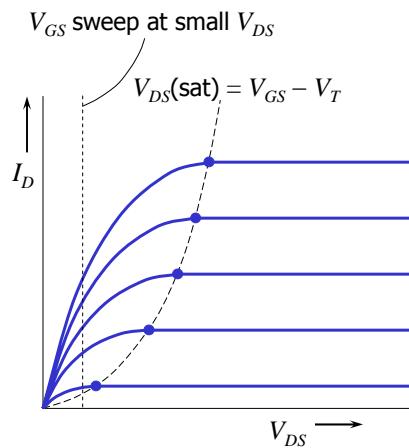


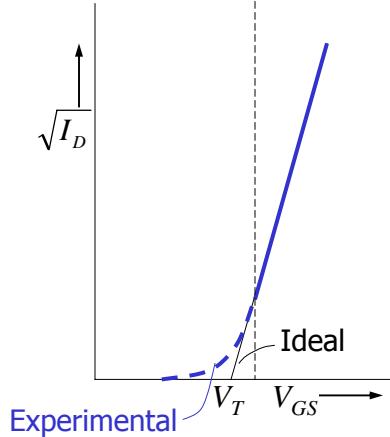
Sub-threshold conduction



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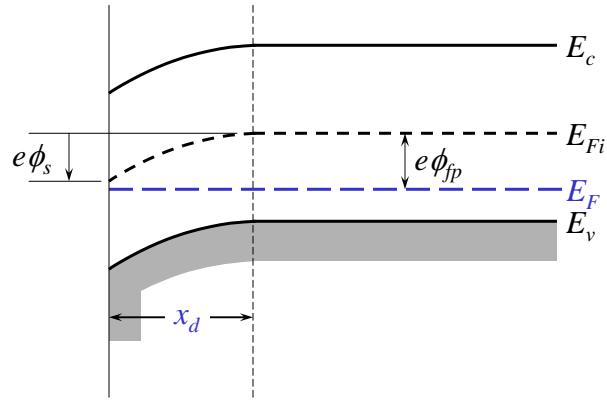
1

Sub-threshold region \longleftrightarrow Saturated region

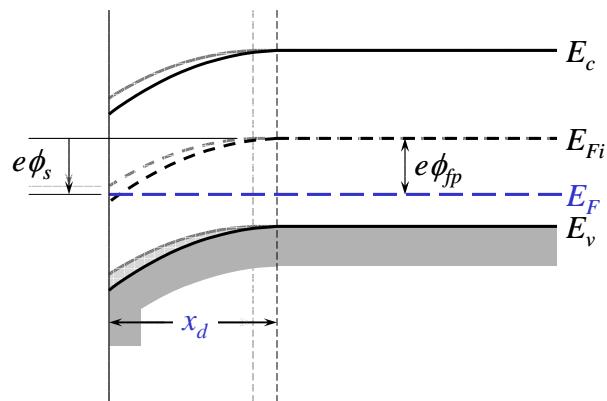


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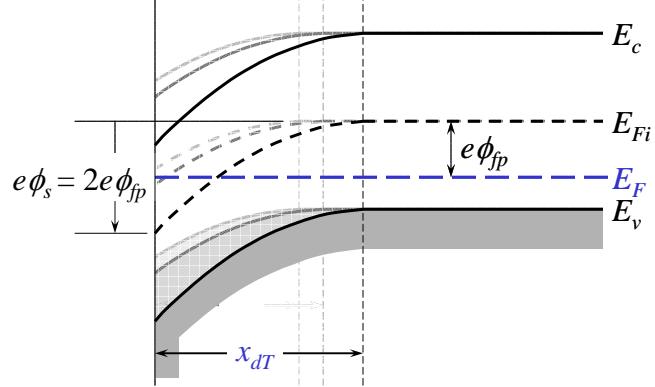
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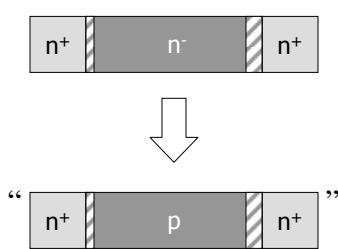
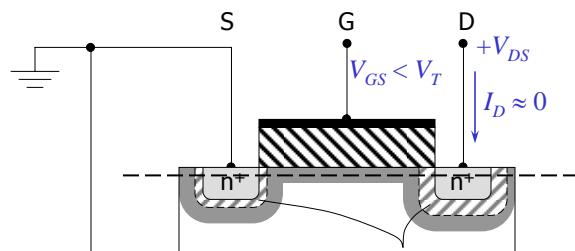
Weak inversion: $\phi_{fp} < \phi_s < 2\phi_{fp}$

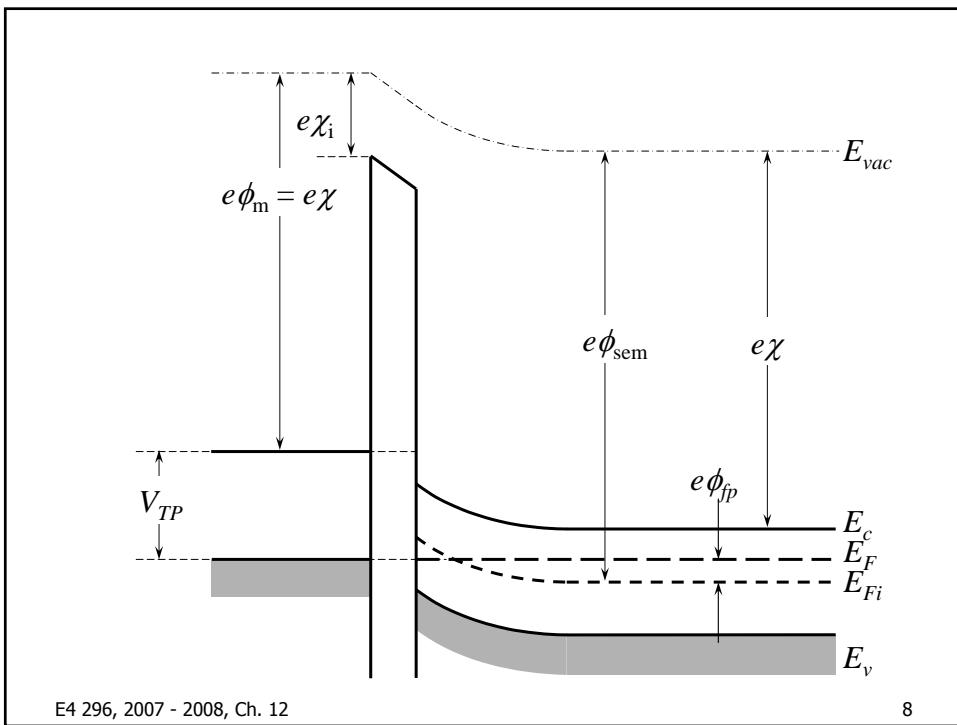
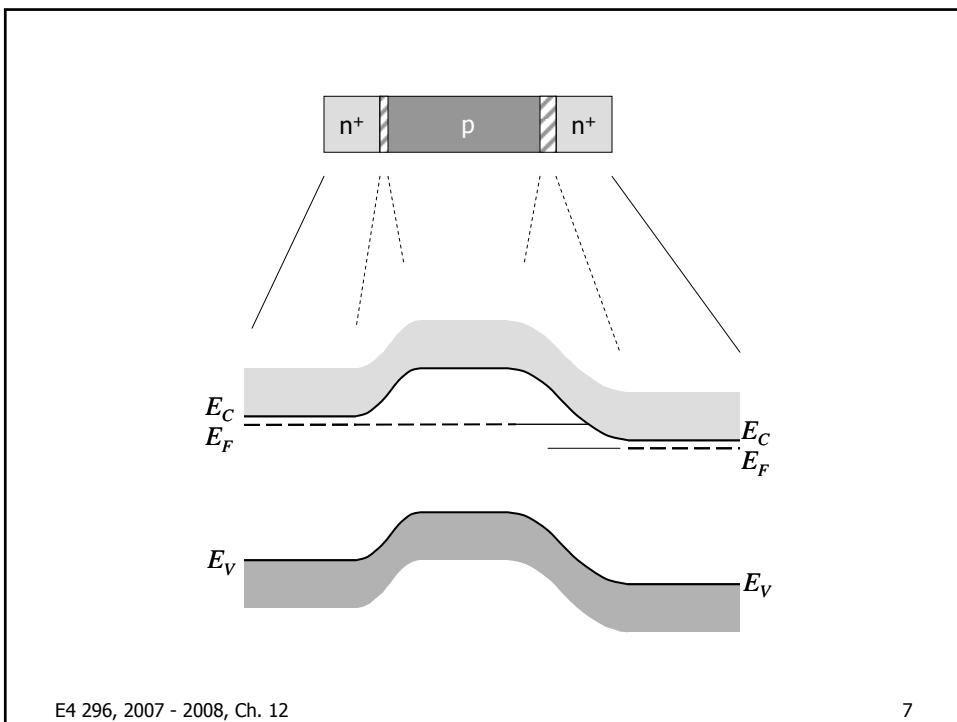


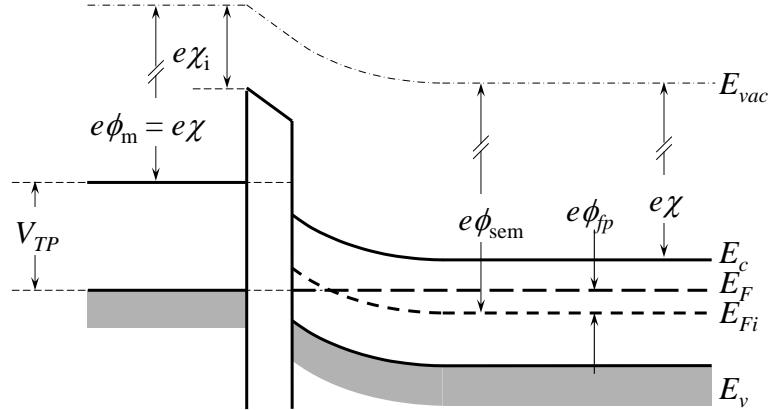
Weak inversion: $\phi_{fp} < \phi_s < 2\phi_{fp}$



Weak inversion: $\phi_{fp} < \phi_s < 2\phi_{fp}$





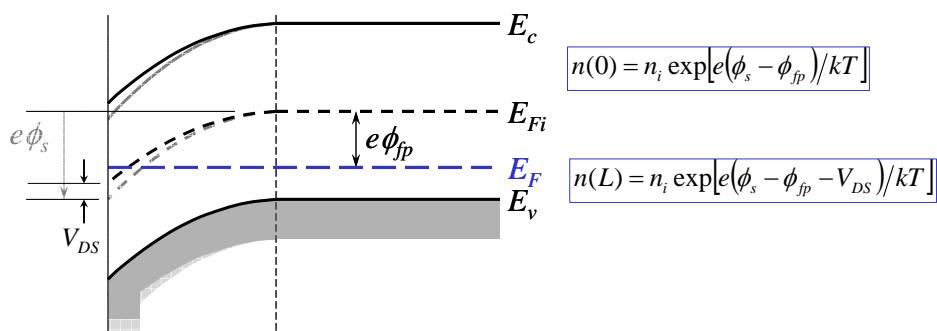


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$$\text{Diffusion current: } I_D = eAD_n \frac{\partial n(x)}{\partial x} = eAD_n \frac{n(L) - n(0)}{L}$$

The electron concentration in the channel depend on the local potential:



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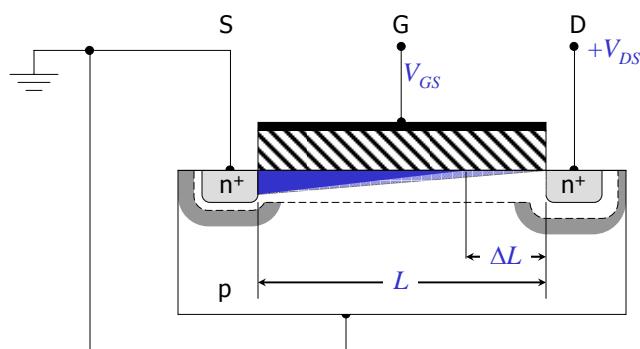
10

We then find for the drain current:

$$I_D = \frac{eAD_n n_i e^{-e\phi_{fp}/kT}}{L} \left(1 - \exp\left(\frac{-eV_{DS}}{kT}\right) \right) \exp\left(\frac{e\phi_s}{kT}\right)$$

$$\approx \exp\left(\frac{e(V_{GS} - V_T)}{kT}\right)$$

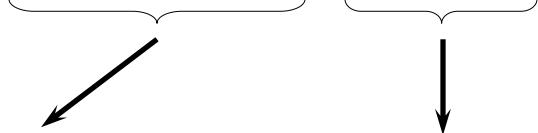
Channel-length modulation



Channel length is modulated as a result of the reverse-bias dependent n⁺-p drain-substrate junction.

...calculating the change in the channel length

$$\Delta L = \sqrt{\frac{2\epsilon_s}{eN_a}} \left[\sqrt{\phi_{fp} + V_{DS}(\text{sat}) + \Delta V_{DS}} - \sqrt{\phi_{fp} + V_{DS}(\text{sat})} \right]$$



Depletion region width
when V_{DS} is higher than
pinch-off.

Depletion region width
at pinch-off.

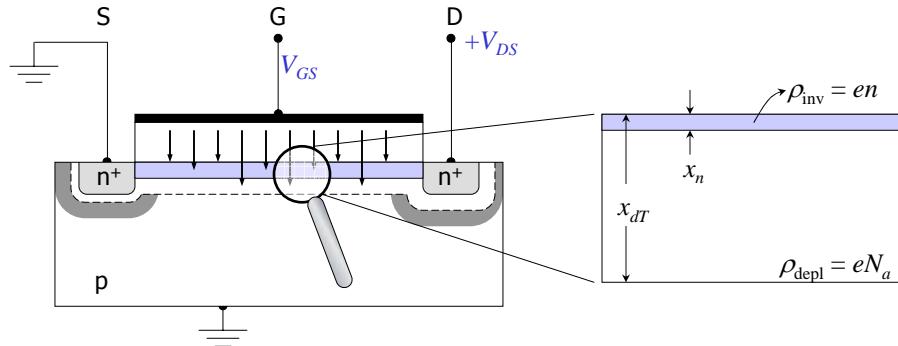
Note: $\Delta V_{DS} = V_{DS} - V_{DS}(\text{sat})$

The drain current then becomes: $I'_D = \left(\frac{L}{L - \Delta L} \right) I_D$

The drain current is now an implicit function of V_{DS} and therefore in saturation the resistance is not infinite

Mobility effects

Mobility variation: $\mu_{\text{eff}} = \mu_0 \left(\frac{E_{\text{eff}}}{E_0} \right)^{-1/3}$ with: $E_{\text{eff}} = \frac{1}{\epsilon_s} \left(|Q'_{SD}(\text{max})| + \frac{1}{2} Q'_n \right)$



Homework: Derive the expression for E_{eff} using Gauss's law?
Assume that width of the inversion-charge layer is much narrower than the width of the depletion layer, $x_n \ll x_{dT}$.

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Velocity saturation

Ideal $I-V$ relationship: $I_D(\text{sat}) = \frac{W\mu_n C_{ox}}{L} (V_{GS} - V_T)^2$

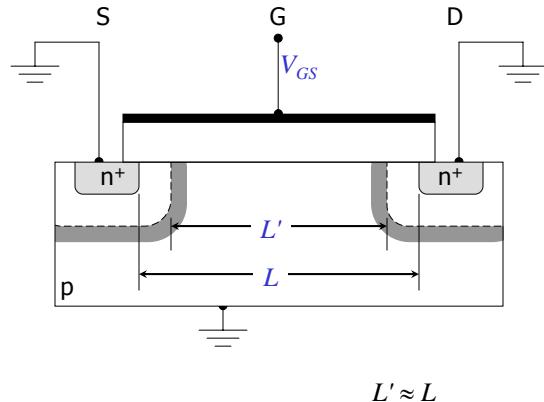
However, when velocity saturation occurs: $\mu_n E = \mu_n \frac{V_{GS} - V_T}{L} \Rightarrow v_{\text{sat}}$

So, the $I-V$ relationship becomes: $I_D(\text{sat}) = W C_{ox} (V_{GS} - V_T) v_{\text{sat}}$

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Threshold-voltage modifications: short-channel effects

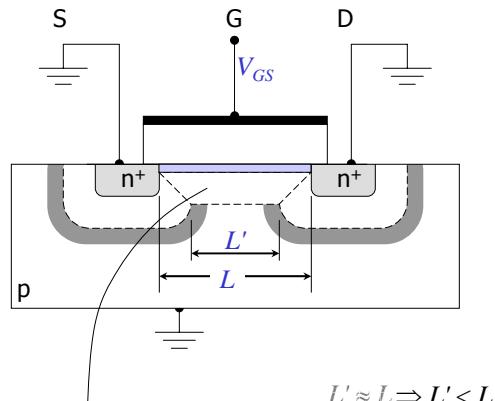


$$L' \approx L$$

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Threshold-voltage modifications: short-channel effects



$$L' \approx L \Rightarrow L' < L$$

Charge in trapezoid controlled by gate voltage

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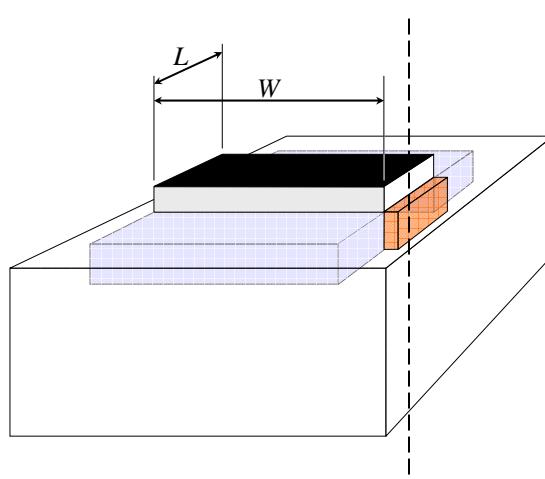
21

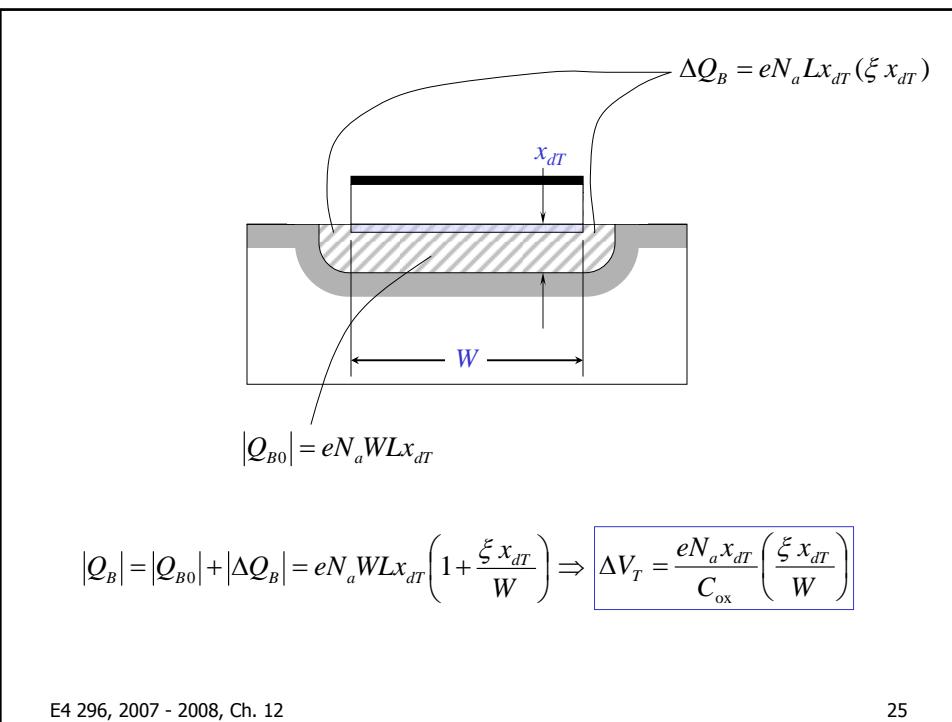
$$\text{From calculation: } |Q_B| = eN_a x_{dT} \left\{ 1 - \frac{r_j}{L} \left[\sqrt{1 + \frac{2x_{dT}}{r_j}} - 1 \right] \right\}$$

$$\Rightarrow \Delta V_T = -\frac{eN_a x_{dT}}{C_{ox}} \left\{ \frac{r_j}{L} \left[\sqrt{1 + \frac{2x_{dT}}{r_j}} - 1 \right] \right\}$$

Homework: The threshold voltage of n-channel MOSFETs is shifted in the negative direction. How will the threshold voltage shift for p-channel MOSFETs?

Threshold-voltage modifications: narrow-channel effects





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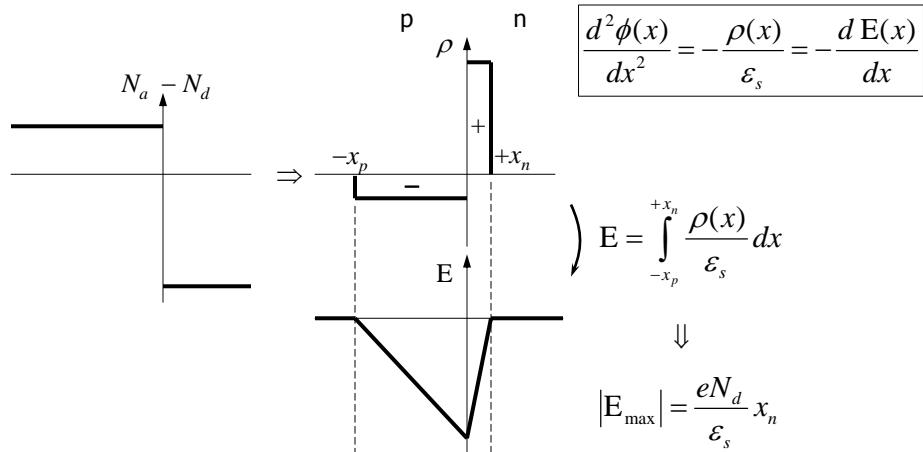
Breakdown mechanisms

- Oxide breakdown: if the electric field across the gate oxide is large enough (for SiO_2 about $6 \times 10^6 \text{ V/cm}$), breakdown can occur.
- Avalanche breakdown: this may occur by impact ionisation in the space charge region near the drain terminal.
- Near avalanche and snapback breakdown: mechanism in which the breakdown of the parasitic bipolar transistor (formed by the n⁺-source, p-substrate, and n⁺-drain) plays a role.
- Near punch-through effects: occurs when the drain-to-substrate space charge region extends completely across the channel region to the source-to-substrate space charge region.

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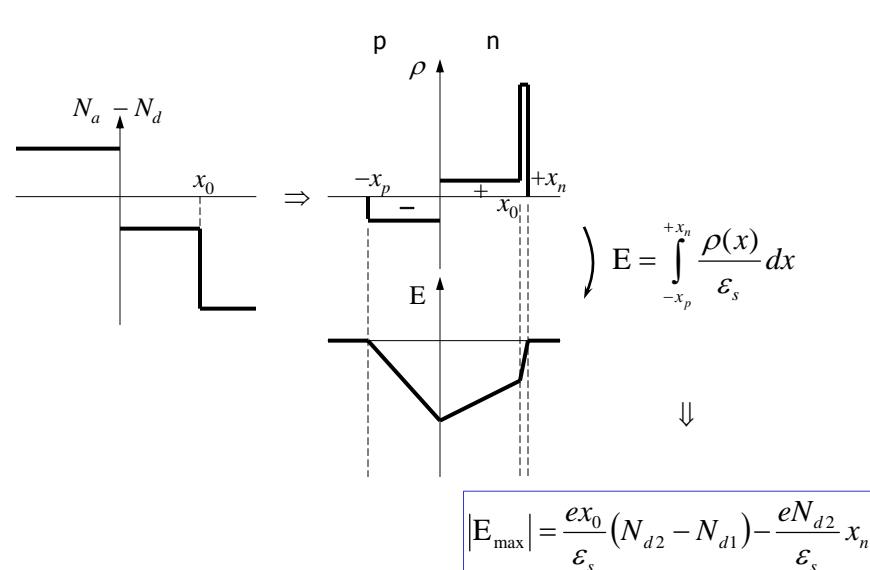
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Lightly-doped drain (LDD) transistor



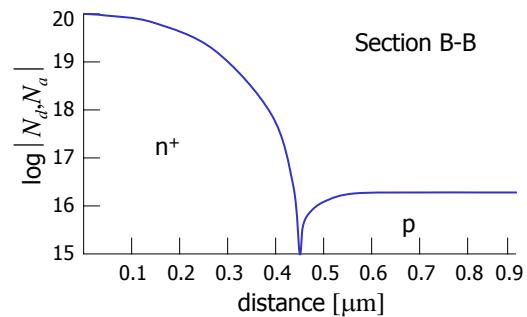
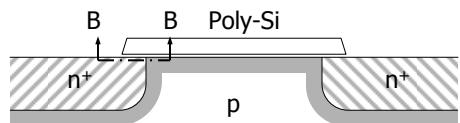
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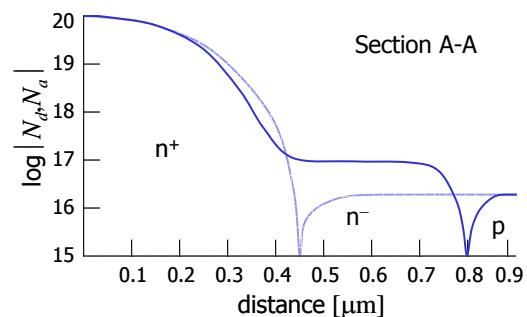
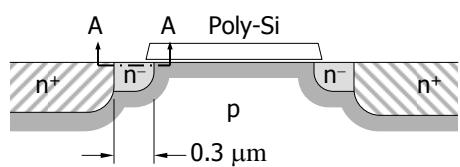
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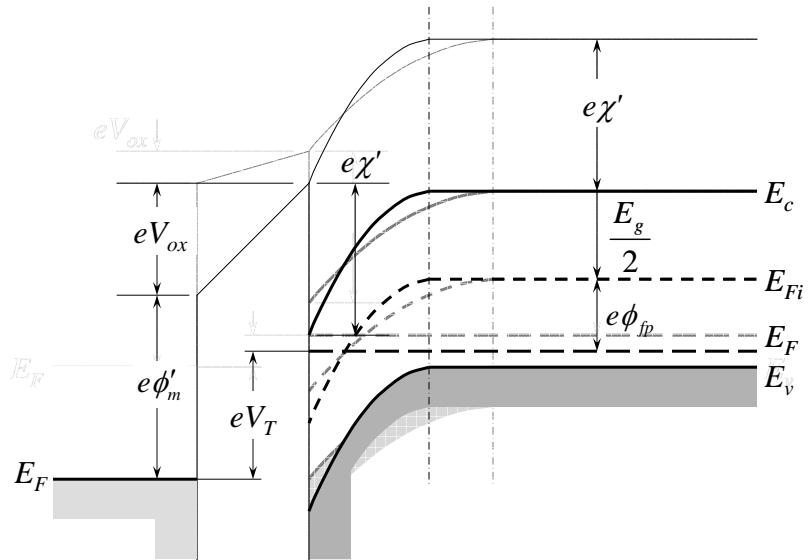
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Threshold-voltage adjustment

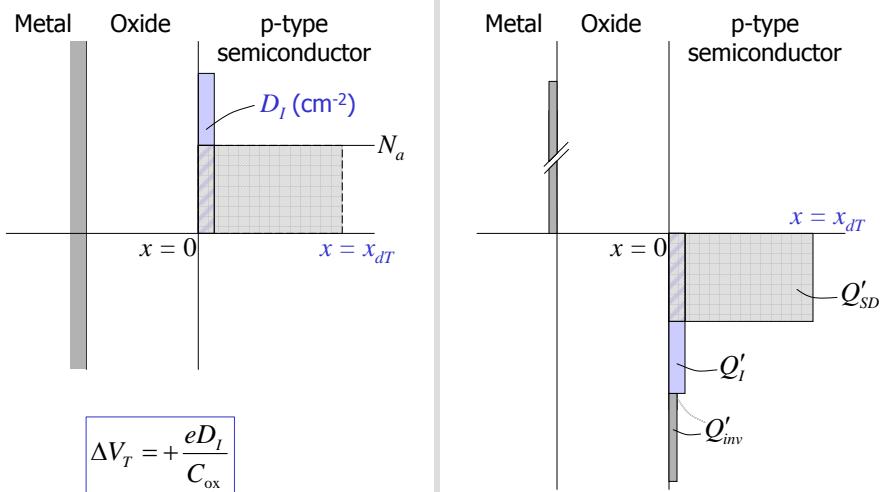


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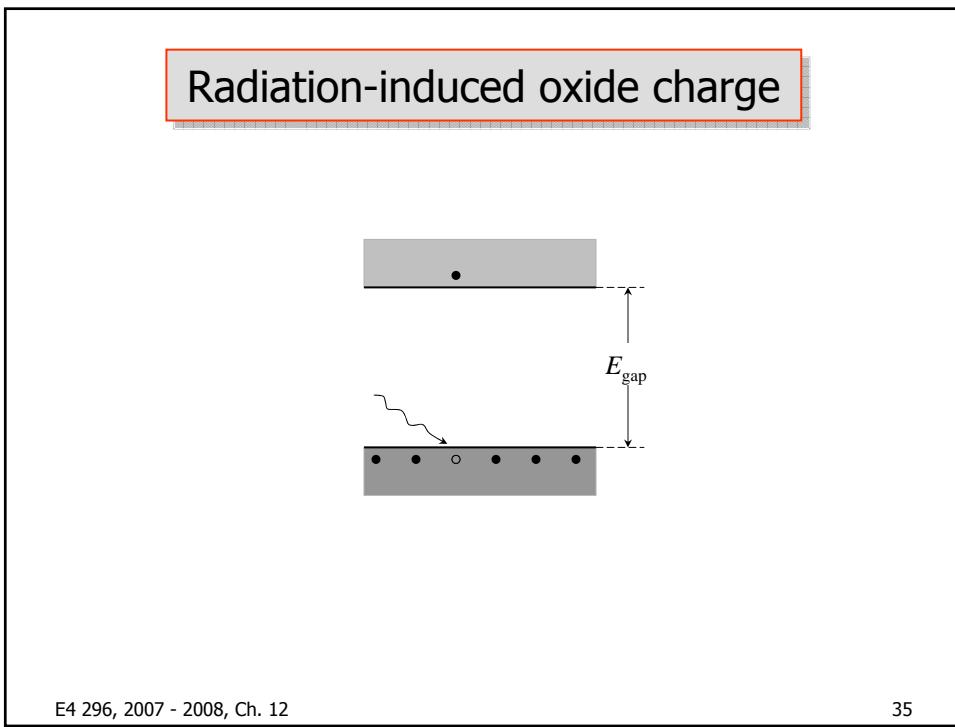
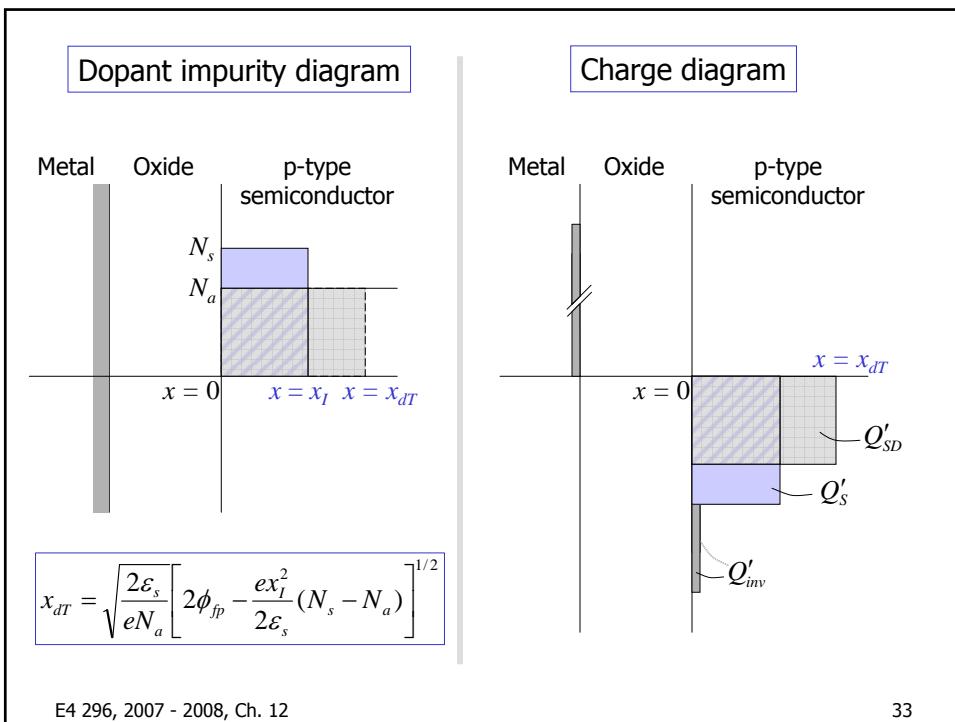
Dopant impurity diagram

Charge diagram

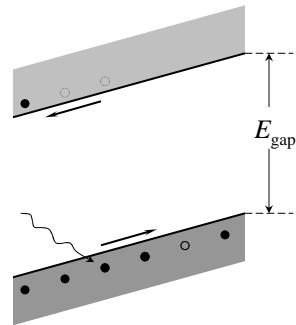


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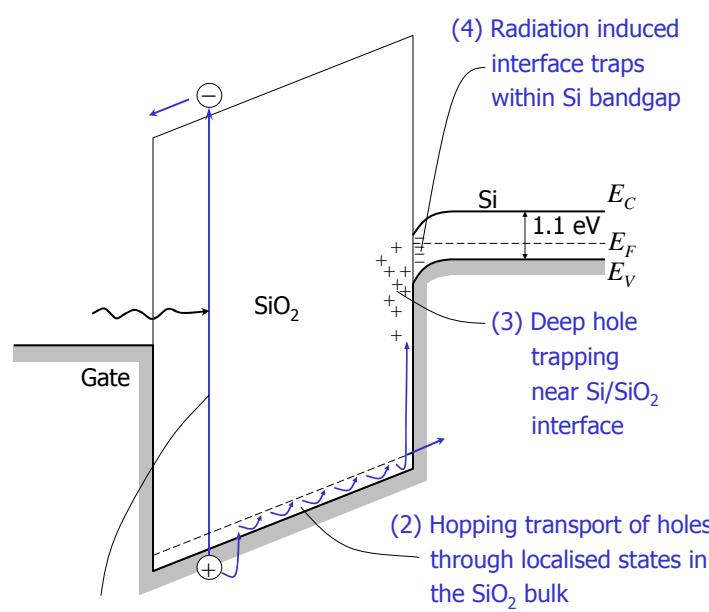


Radiation-induced oxide charge



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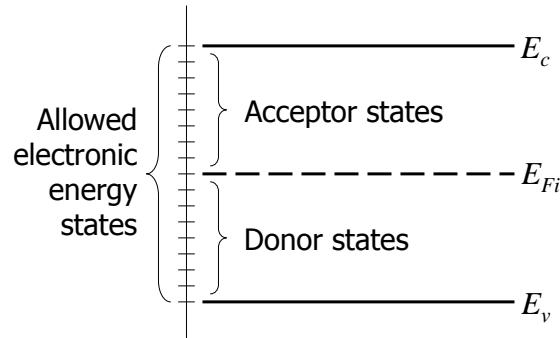
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Radiation-induced interface states



donor $\equiv 0$ or $+e$

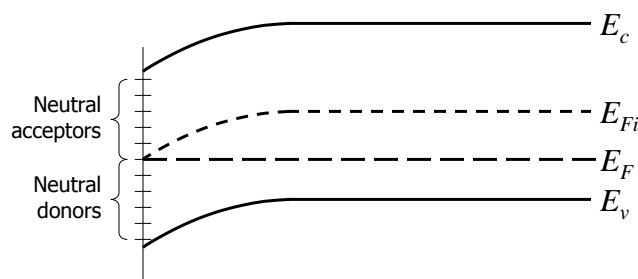
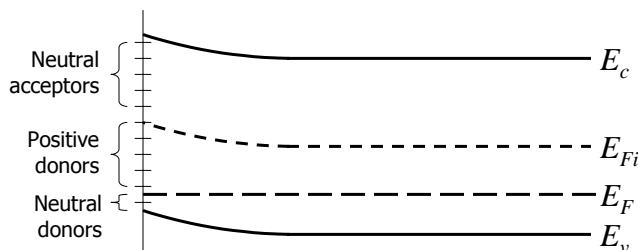
acceptor $\equiv -e$ or 0

above E_F : acceptors 0, donors $+e$

below E_F : acceptors $-e$, donors 0

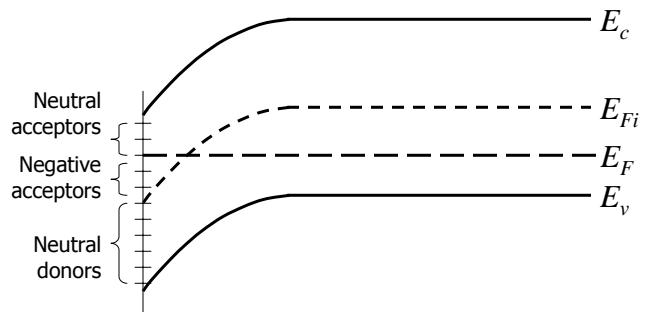
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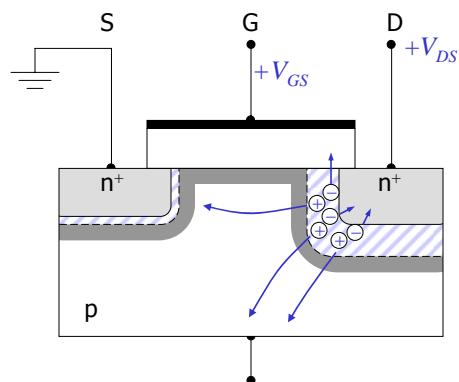
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Hot electron charging effects

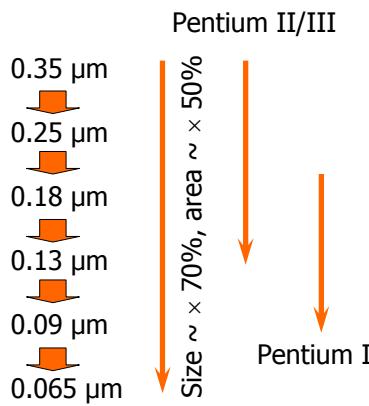


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MOSFET scaling

Moore's law



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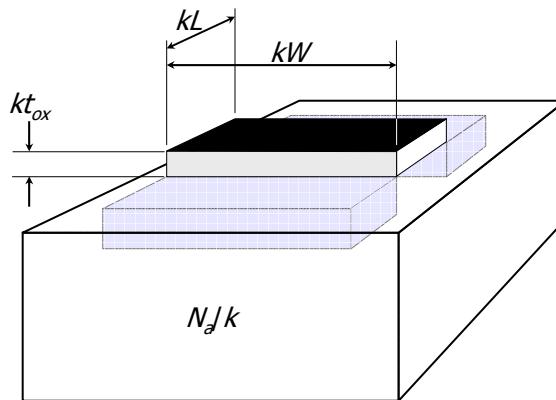
MOSFET scaling

- Constant voltage scaling
- Constant field scaling

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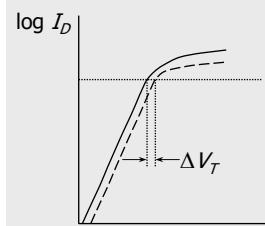
MOSFET scaling: constant field scaling



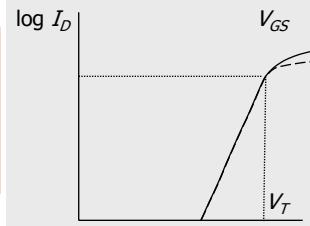
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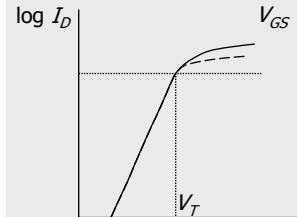
Reducing channel length, L :
 ⇒ short-channel effect
 ⇒ threshold voltage reduction



Increasing dopant concentration, N :
 ⇒ reduced short-channel effect
 ⇒ threshold voltage increase



Reducing oxide thickness, t_{ox} :
 ⇒ Decrease channel width to avoid capacitance increase
 ⇒ threshold voltage 'retuned'



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MOSFET scaling: constant field scaling

- Both lateral and vertical dimensions are decreased by factor of $k < 1$ (i.e., $L \Rightarrow kL$)
- Doping levels are increased by factor $1/k$
- Voltages V_{DS} and V_{GS} are decreased by factor k

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MOSFET scaling: constant field scaling

$$\text{Poisson equation: } \nabla^2 \psi = -\frac{qN_a}{\epsilon_s}$$

This is invariant when: $x \rightarrow kx ; y \rightarrow ky ; z \rightarrow kz ; \psi \rightarrow k\psi ; N_a \rightarrow N_a / k$

$$\text{The electric field: } \mathbf{E} = -\nabla \psi \Rightarrow \left(\vec{i} \frac{\partial(k\psi)}{\partial(kx)} + \vec{j} \frac{\partial(k\psi)}{\partial(ky)} + \vec{z} \frac{\partial(k\psi)}{\partial(kz)} \right)$$

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MOSFET scaling: constant field scaling

	Device and circuit parameters	Scaling factor ($k < 1$)
Scaled parameters	Device dimensions (L, t_{ox}, W, x_j)	k
	Doping concentration (N_a, N_d)	$1/k (1/k^2)^*$
	Voltages	k
Effect on device parameters	Electric field	1
	Carrier velocity	1
	Depletion widths	k
	Capacitance ($C = \epsilon A/t$)	k
	Drift current	k
Effect on circuit parameters	Device density	$1/k^2$
	Power density	1
	Power dissipation per device ($P = VI$)	k^2
	Circuit delay time ($\approx CV/I$)	k
	Power-delay product (P_t)	k^3

*S. Dimitrijev, *Principles of Semiconductor Devices* (Oxford University Press, 2006), p. 321

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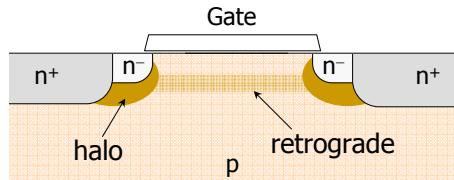
Advanced MOSFETs

- High- k gate dielectric
 - $C = \epsilon_d / t_d$; $\epsilon_d = k\epsilon_0$
 - Allows use of thicker layers \Rightarrow reduced leakage current
 - Big disadvantage: poor interface with Si
- Metal gates
 - $V_T \propto \phi_{ms}$
 - Replace n⁺ polysilicon with small work function metal \Rightarrow parallel negative shift of transfer characteristics
 - Molybdenum (Mo) is attractive, a.o. because of controllable work function

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Advanced MOSFETs



Retrograde substrate doping profiles:

- High doped region prevents extension drain electric field
- Lower doped region prevents threshold voltage increase and channel-mobility reduction

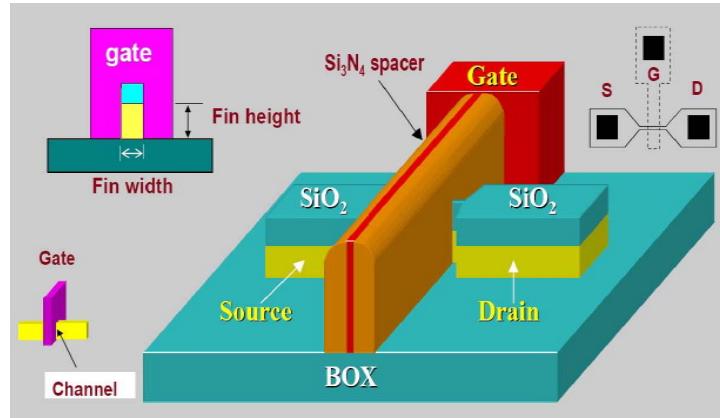
Halo doping profile:

- Increased source-to-substrate barrier for carrier injection

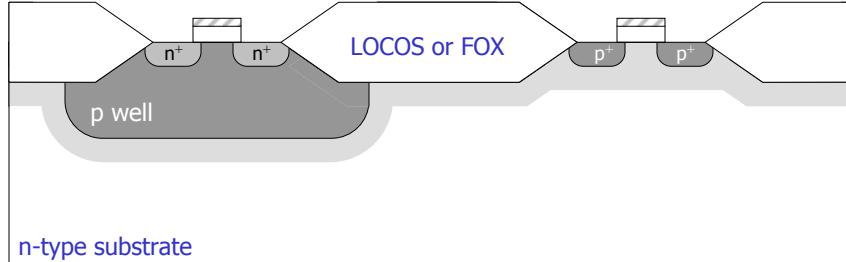
Advanced MOSFETs

Double-gate MOSFETs: FinFET

- Second gate halves the body thickness
- Prevents extension drain electric field under channel



CMOS technology



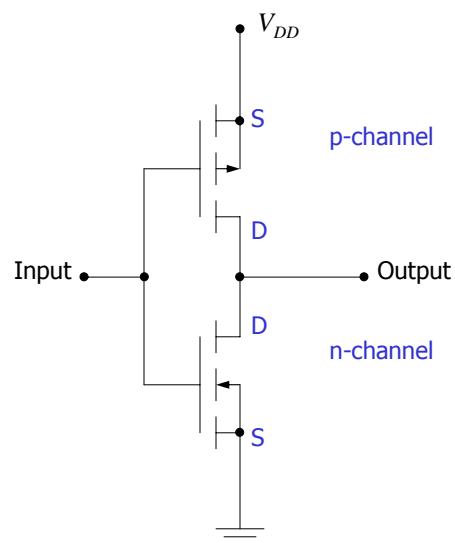
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LOCOS = LOCal Oxidation of Silicon

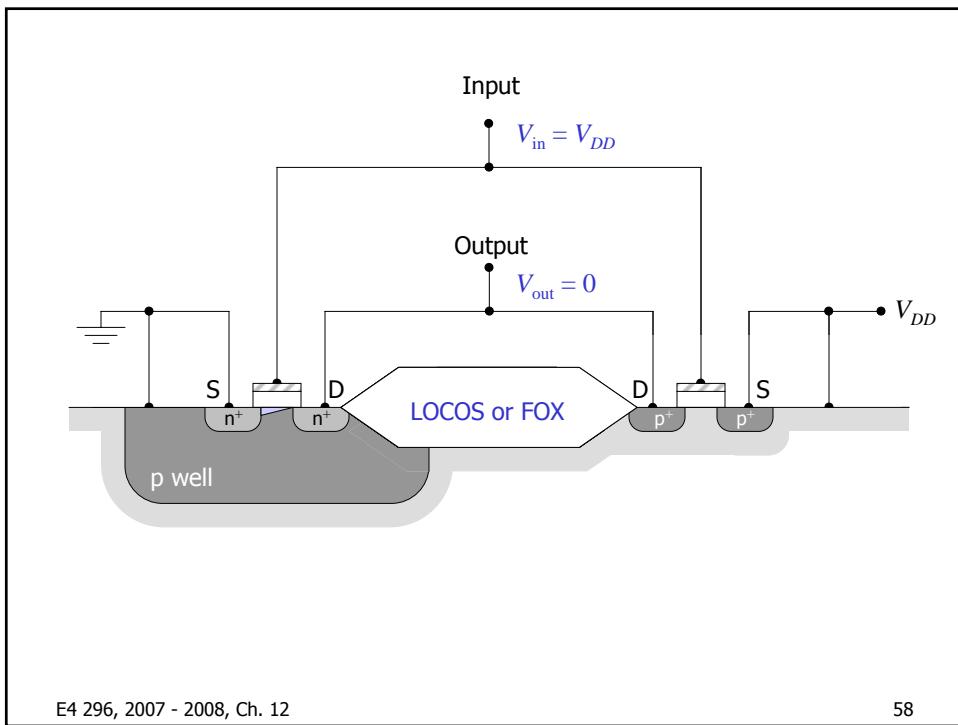
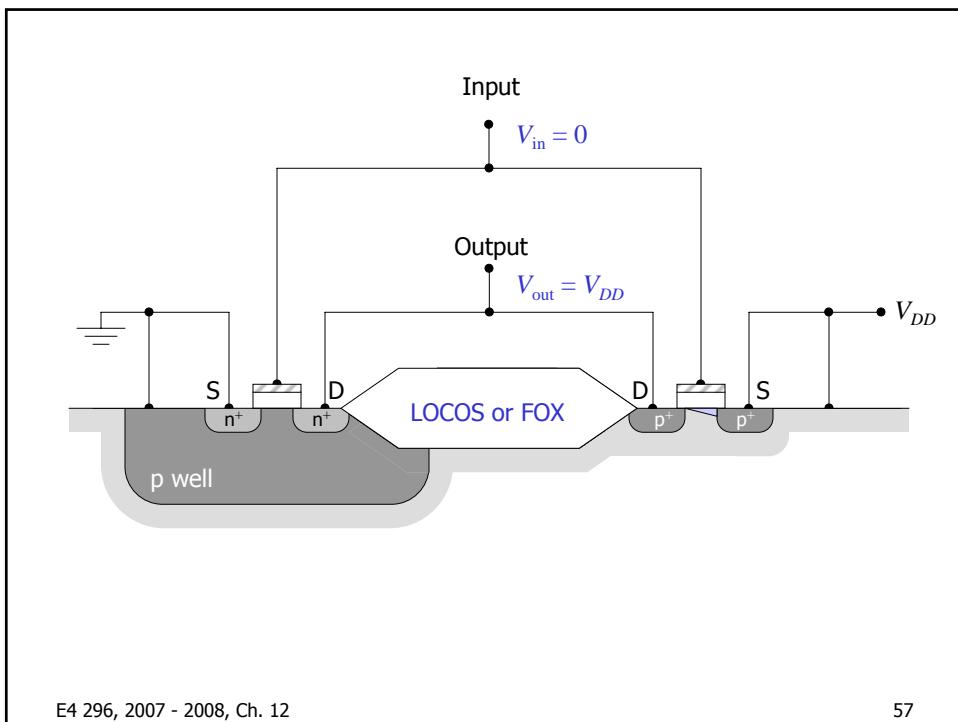
FOX = Field Oxide

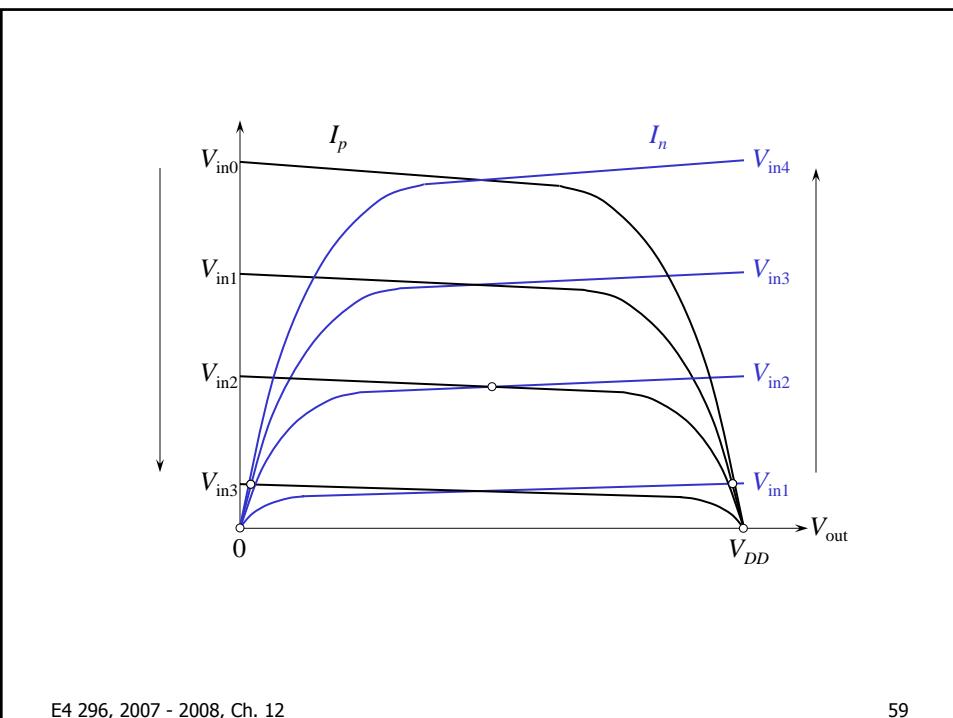
CMOS inverter



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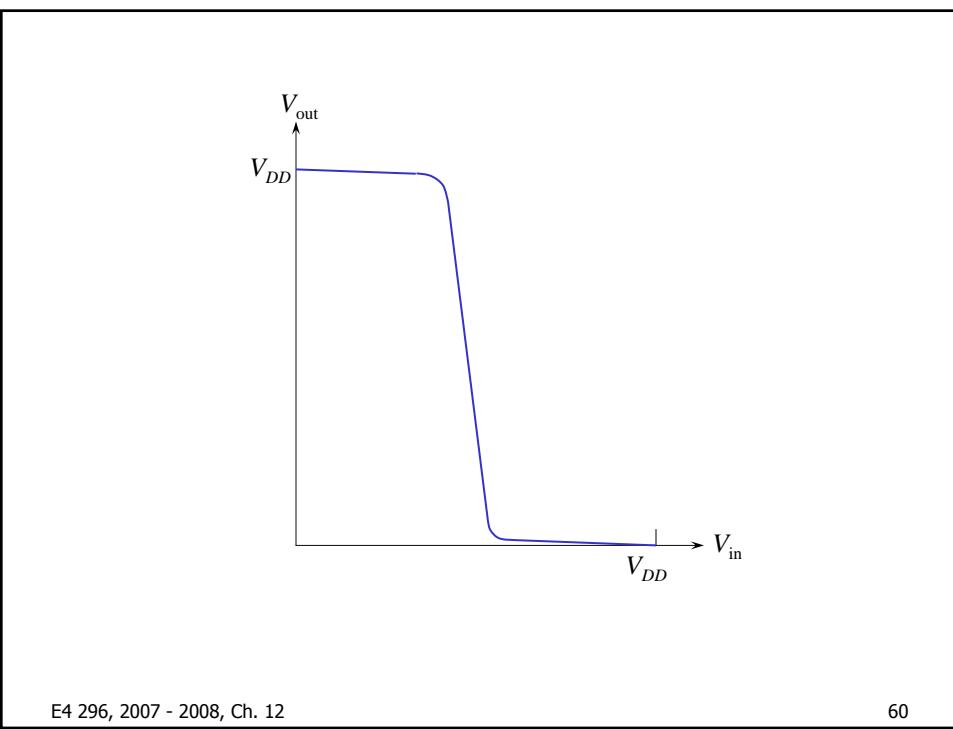
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