Exam Analog Integrated Circuit Design (ET 4252)
August 30, 2007
14:00-17:00h

This exam consists of three main questions. Please start on a new sheet of paper for each main question.

You are allowed to use a calculator and one piece of A4-sized paper with hand-written, non-copied personal notes.

Prefixes:

Giga	(G)	$= 10^{9}$
Mega	(M)	$= 10^{6}$
kilo	(k)	$= 10^{3}$
milli	(m)	$= 10^{-3}$
micro	(μ)	$= 10^{-6}$
nano	(n)	$= 10^{-9}$
pico	(p)	$= 10^{-12}$
femto	(f)	$= 10^{-15}$
atto	(a)	$= 10^{-18}$

$k = 1.38 \cdot 10^{-23}$ J/K (Boltzmann's constant)

$q = 1.60 \cdot 10^{-19}$ C (elementary charge)

$V_T = \frac{kT}{q} = 25.9\text{mV at } T = 300K$

Do not forget to put your name and study number on all material you hand in. And please turn off your mobile phone.

Good luck!

Dr.ir. Wouter A. Serdijn
Dr.ir. Aleksandar Tasic

Question 1: Design of a Voltage-Controlled Oscillator (VCO) for an Impulse-Radio Ultra-Wideband (UWB) Quadrature Downconverter

A negative resistance LC voltage-controlled oscillator is shown in Fig. 1.

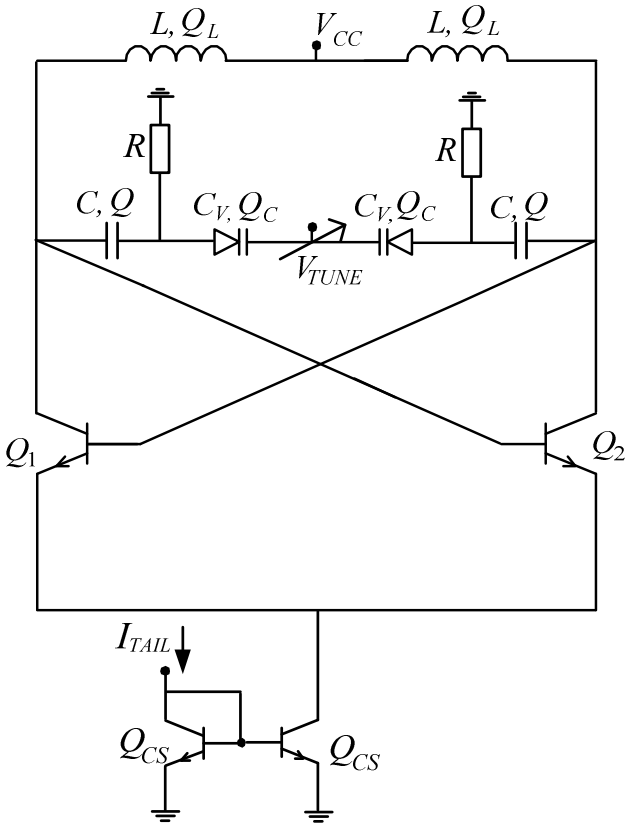


Figure 1: LC voltage-controlled oscillator.

The oscillator consists of a resonating LC tank, a cross-coupled transconductance amplifier (Q_1 and Q_2), and a bias current source (Q_{CS}). L stands for the tank inductance, Q_L for its quality factor, C_V for the varactor capacitance, Q_{CV} for its quality factor, C for the additional tank capacitance (C=C_V at the oscillation central frequency) with a quality factor Q_C=2Q_{CV}, and I_{TAIL} for the bias tail current. For the bias resistor R it holds: R>>1.

Determine the circuit parameter values of this oscillator in order to meet the requirements of the impulse-radio UWB quadrature downconverter.

The oscillator requirements for the impulse-radio UWB quadrature downconverter are:

- oscillation central frequency of 5.7GHz
- phase noise better than –80dBc/Hz at 1MHz offset from the oscillation central frequency
- peak amplitude of a differential oscillation voltage signal across the LC-tank around 400 mV
- power consumption drawn from a supply voltage of V_{CC}=1.8V as low as possible

For a silicon technology chosen, inductors with quality factors of 30 and varactors with quality factors of 40 are available. The noise factor of the oscillator active part equals A=4.

Provide the following:

a) (5%) Derived expression for the LC-tank impedance (Z) at an offset angular frequency ($\Delta\omega$) from the oscillation angular frequency without considering inductor and capacitor losses.

$$C_{eq} = \frac{1}{2} \cdot \frac{C \cdot C_V}{C + C_V}$$

$$L_{eq} = 2L$$

$$Z(\omega_0) = \frac{1}{\frac{1}{j\omega_0 L_{eq}} + j\omega_0 C_{eq}} = \frac{j\omega_0 \cdot 2L}{1 - \omega_0^2 L \frac{C \cdot C_V}{C + C_V}}$$

$$Z(\omega_0 + \Delta\omega) = \frac{j(\omega_0 + \Delta\omega) \cdot 2L}{1 - (\omega_0 + \Delta\omega)^2 L \frac{C \cdot C_V}{C + C_V}}$$

$$\approx \frac{j\omega_0 \cdot 2L}{-2\omega_0 \cdot \Delta\omega \cdot L \frac{C \cdot C_V}{C + C_V}} = -j \frac{\omega_0}{\Delta\omega} \cdot \frac{C + C_V}{C \cdot C_V \cdot \omega_0} = -\frac{j}{2\Delta\omega C_{eq}}$$

where

ω_0 follows from $1 - \omega_0^2 L \frac{C \cdot C_V}{C + C_V} = 0$, hence $\omega_0 = \frac{1}{\sqrt{L \frac{C \cdot C_V}{C + C_V}}}$

b) (15%) Derived expression for the LC-tank conductance (G_{TK}) at the oscillation frequency (f_0).

R_{CV} = series resistance of varactor

R_C = series resistance of capacitor

R_L = series resistance of inductor

$$R_C = \frac{1}{\omega_0 C Q_C} = \frac{1}{\omega_0 C_V Q_C}$$

$$R_{CV} = \frac{1}{\omega_0 C_V Q_{CV}}$$

$$R_L = \frac{\omega_0 L}{Q_L}$$

$$Q_C = 2Q_{CV}$$

$$R_{C,eq} = 2R_C + 2R_{CV} = \frac{2}{\omega_0 C Q_C} + \frac{2}{\omega_0 C_V Q_{CV}} = \frac{3}{\omega_0 C_V Q_{CV}}$$

$$R_{L.eq} = 2R_L = \frac{2\omega_0 L}{Q_L}$$

$$G_{C,eq} = R_{C,eq} \cdot (\omega_0 C_{eq})^2$$

$$G_{L.eq} = \frac{R_L}{(\omega_0 L_{eq})^2}$$

$$G_{TK} = G_{C,eq} + G_{L.eq} = \frac{3}{\omega_0 C_V Q_{CV}} \cdot \left(\frac{\omega_0 C}{4}\right)^2 + \frac{2\omega_0 L}{Q_L (2\omega_0 L)^2}$$

$$= \frac{3}{16}\frac{\omega_0 C}{Q_{CV}} + \frac{1}{2\omega_0 L Q_L}$$

$$= \frac{3}{16}(\omega_0 C_V)^2 R_{CV} + \frac{R_L}{2(\omega_0 L)^2}$$

$$= \omega_0 C\left(\frac{1}{4Q_L} + \frac{3}{16Q_{CV}}\right) = \frac{1}{2\omega_0 L}\left(\frac{1}{Q_L} + \frac{3}{4Q_{CV}}\right)$$

c) (5%) Expression for the oscillation frequency and oscillation condition.

Applying the Barkhausen criteria,

ω_0 follows from $1 - \omega_0^2 L \frac{C \cdot C_V}{C + C_V} = 0$, hence $\omega_0 = \frac{1}{\sqrt{L\frac{C \cdot C_V}{C + C_V}}} = \frac{1}{\sqrt{LC_V/2}}$,

and for the startup of the oscillation,

$|T(\omega_0)| \geq 1$, $T(\omega_0)$ being the loop gain of the oscillator

hence,

$$G_{diffpair} = \frac{g_m}{2} = \frac{I_{tail}}{4V_T} \geq G_{TK}$$

d) (10%) Derived expression for the phase noise of the oscillator. Model the noise contribution of the LC-tank to the phase noise by its loss resistance

(R_{TK}), and the active part noise contribution by a factor AG_{TK}, A being its noise factor.

The noise (voltage) contribution (power spectral density) of the LC-tank, $S_{V,LC}$, equals

$$S_{V,LC} = 4kTG_{TK} \cdot \left|Z(\omega_0 + \Delta\omega)\right|^2 = 4kTG_{TK} \cdot \frac{1}{4G_{TK}^2 Q^2} \cdot \left(\frac{\omega_0}{\Delta\omega}\right)^2 = \frac{kT}{G_{TK} Q^2} \cdot \left(\frac{\omega_0}{\Delta\omega}\right)^2$$

The noise (voltage) contribution of the active part equals

$$S_{V,AP} = A \cdot S_{V,LC} = A \cdot 4kTG_{TK} \cdot \left|Z(\omega_0 + \Delta\omega)\right|^2 = \frac{A \cdot kT}{G_{TK} Q^2} \cdot \left(\frac{\omega_0}{\Delta\omega}\right)^2$$

$A = 4$ (given)

So for the phase noise it follows:

$$L(\Delta\omega) = \frac{1}{2} \frac{S_{V,LC} + S_{V,AP}}{v_s^2 / 2} = \frac{(1+A) \cdot kT}{G_{TK} Q^2 v_s^2} \cdot \left(\frac{\omega_0}{\Delta\omega}\right)^2 = \frac{(1+A) \cdot kTG_{TK}}{(\omega_0 C_{eq})^2 v_s^2} \cdot \left(\frac{\omega_0}{\Delta\omega}\right)^2$$

$$v_s = \frac{2I_{tail}}{\pi G_{TK}}$$

e) (35%) Values of inductance L, varactor capacitance C_V, and tail current I_{TAIL} for the oscillator requirements at the central oscillation frequency, using the results obtained in a)-d).

From the phase noise and signal swing requirements, we get

$L(1\text{MHz}) \le -80\text{dBc/Hz}$ and $v_s = 0.4\text{V}$.

Hence,

$$L(1\text{MHz}) = \frac{1}{2}\frac{S_{V,LC} + S_{V,AP}}{v_s^2/2} = \frac{(1+A)\cdot kT}{G_{TK}Q^2 v_s^2}\cdot\left(\frac{5.7\text{GHz}}{1\text{MHz}}\right)^2 \le 10^{-8}$$

$A = 4$

1) Q follows from a):

$$\frac{1}{Q} = \frac{1}{Q_L} + \frac{3}{4Q_V} = \frac{1}{19.2}$$

$$v_s = \frac{2I_{tail}}{\pi G_{TK}} = 0.4\text{V}$$

2) $$G_{TK} = \frac{1}{2\omega_0 L}\left(\frac{1}{Q_L} + \frac{3}{4Q_{CV}}\right) = \frac{\omega_0 C}{4}\left(\frac{1}{Q_L} + \frac{3}{4Q_{CV}}\right) = \frac{1}{2\omega_0 L}\frac{1}{Q}$$

$$\ge \frac{5kT}{Q^2 v_s^2}\cdot\left(\frac{5.7\text{GHz}}{1\text{MHz}}\right)^2 \cdot 10^8 = 1.14\cdot 10^{-6}$$

3) $$L = \frac{L_{eq}}{2} = \frac{1}{2\omega_0 Q G_{TK}} \le 0.64\mu\text{H}$$

4) $$C = 4C_{eq} = \frac{4QG_{TK}}{\omega_0} \ge 2.4\text{fF}$$

or from: $$f_0 = \frac{1}{2\pi\sqrt{L\frac{C\cdot C_V}{C+C_V}}} \Rightarrow C = C_V = \frac{2}{(2\pi f_0)^2 L} \ge 2.4\text{fF}$$

5) $$I_{tail} = \frac{\pi G_{TK} v_s}{2} = 0.72\mu\text{A}$$

Check whether the loop gain is larger than 1: $$\frac{g_m}{2G_{TK}} = \frac{I_{tail}}{4V_T G_{TK}} = 6.1 \ge 1$$

f) (15%) Values of minimum ($C_{V,MIN}$) and maximum ($C_{V,MAX}$) varactor capacitances to overcome the effects of 10% absolute tolerance on the inductors, varactors and capacitors used.

From a) it follows: $$\omega_0 = \frac{1}{\sqrt{L\frac{C\cdot C_V}{C+C_V}}}$$

So for a 10% change in L, C and C_V while ω_0 remains constant, $L\frac{C\cdot C_V}{C+C_V}$ has to remain constant. This entails:

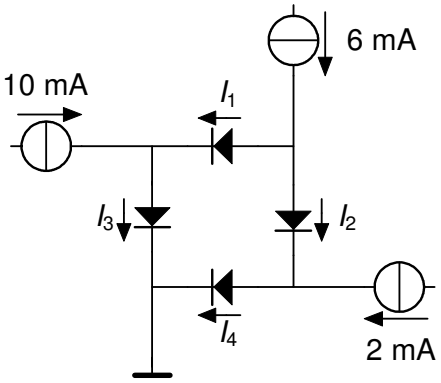
$$L\frac{C\cdot C_V}{C+C_V} = (L \pm \Delta L)\frac{(C\pm\Delta C)\cdot(C_V \pm \Delta C_V)}{C\pm\Delta C + C_V \pm \Delta C_V}$$

g) (15%) Ways to reduce the power consumption (at the expense of phase noise, which is acceptable in this application) by changing the active circuit (not the LC-tank configuration).

Increase the loop gain by connecting stages in cascade instead of increasing the tail current. Two differential pairs in cascade can have a larger transconductance than a single differential pair at the same total bias current.

Question 2: Translinear and biasing circuits

a) A bridge rectifier can be viewed as a translinear loop. Assuming identical diodes, what are the four diode current values I_1, I_2, I_3 and I_4 in the figure below?



First, write down the translinear (TL) loop equation: $I_1 \cdot I_3 = I_2 \cdot I_4$

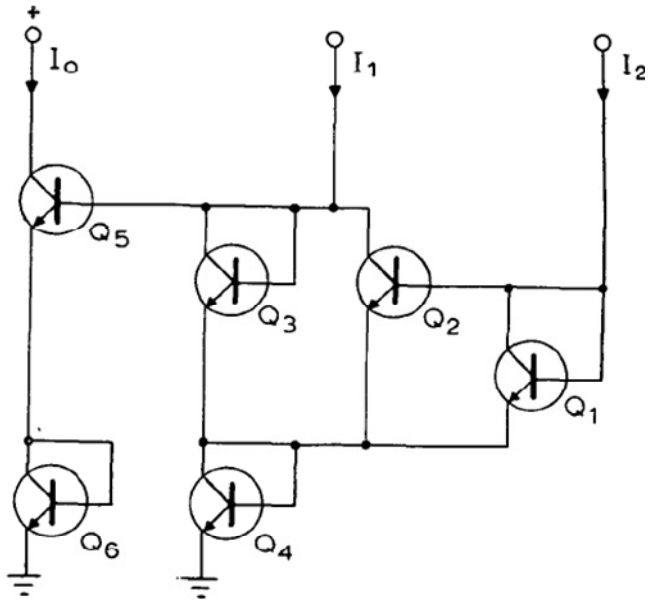
Second, write down the set of nodal equations:

$$I_1 + I_2 = 6 \text{ mA}$$
$$I_1 + 10 \text{ mA} = I_3$$
$$I_2 + 2 \text{ mA} = I_4$$

Third (and finally), the above set of 4 equations yields:

$$I_1 = 2 \text{ mA}$$
$$I_2 = 4 \text{ mA}$$
$$I_3 = 12 \text{ mA}$$
$$I_4 = 6 \text{ mA}$$

b) Analyze the output current I_o in terms of the input currents I_1 and I_2 for the circuit below. All transistors are equivalent.



First (again), write down the translinear loop equations:

$$I_6 \cdot I_5 = I_3 \cdot I_4$$
$$I_1 = I_2$$

Second, write down the nodal equations:

$$I_O = I_{Q5} = I_{Q6}$$
$$I_2 = I_{Q1} = I_{Q2}$$
$$I_4 = I_{Q1} + I_{Q2} + I_{Q3} = I_1 + I_2$$

Third (and finally), solve the set of equations:

$$I_O^2 = (I_1 - I_2)(I_1 + I_2)$$
$$I_O = \sqrt{I_1^2 - I_2^2}$$

c) What restrictions hold for the magnitudes of the input currents I_1, I_2 and I_o in the above circuit? Write them in the form of inequalities, such as $I_y > 0$.

TL circuits can be functional as long as the collector current of all transistors are nonnegative. This yields:

$$I_O \geq 0$$
$$I_2 \geq 0$$
$$I_1 \geq I_2$$

We will now concentrate on the design of a current source that delivers I_1. Assume its output current to be constant and equal to 2mA. Also, assume I_2 to be equal to 1mA.

d) What is the load impedance of the current source, i.e., what is the value of the (low-frequency) impedance seen by the current source that delivers I_1?

The load impedance (resistance) of the current source, R_L, mentioned is the input impedance of the combination of Q5 and Q6, in parallel with {[the resistance of diode connected transistor Q3 ($1/g_m$) in parallel with the output impedance of Q2 (r_o)], in series with the resistance of diode connected transistor Q4 ($1/g_m$)}. Neglecting r_o, as it is much greater than both r_{pi} and $1/g_m$, we get:

$$\begin{aligned} R_L &= [r_{\pi 5} + (\beta+1)/(g_{m6} + 1/r_{\pi 6})] // [1/g_{m3} + 1/g_{m4}] \\ &= [r_{\pi 5} + r_{\pi 6}] // [1/g_{m3} + 1/g_{m4}] \\ &\approx 1/g_{m3} + 1/g_{m4} \end{aligned}$$

e) Design a single-transistor (i.e., having one transistor only and possibly a few passive components, such as resistors, capacitors, etc.) current source to implement I_1.

There are a few alternatives here. They all employ a PNP transistor (possibly with an emitter series resistor or diode to the positive supply and some kind of (possibly nonlinear) voltage divider between the positive and negative rail to deliver an appropriate voltage at the base of the transistor. Possible elements of the voltage divider are resistors and/or diodes.

f) What is the value of its (low-frequency) output impedance?

If the emitter of the PNP transistor is connected to the positive supply, the output resistance equals $r_o = V_{AF}/I_C$, V_{AF} being the forward Early voltage (usually between 10 and 100 volt), I_C being the transistor collector current of 2 mA.

If the emitter of the PNP transistor is connected in series with a resistor and/or diode(s), the output impedance may (depending on the loop gain) increase to approximately $(\beta+1)r_o$.

g) Give two possible ways to improve the power-supply rejection (PSRR) of your current source implementation.

There are many possible ways to enhance the PSRR. They can be divided into two categories: one is based on the suppression of supply voltage variations before they reach the current source; the other is based on improving the current-source behavior of the current source.

In the first category we find: filtering the supply lines and having the supply regulated by a voltage source.

In the second category we find: stabilizing the resistive voltage divider by either making it nonlinear or by filtering the voltage across the upper resistor and increasing the resistance in the emitter lead or by applying a cascode.

As said, there are many possible ways.

h) Now redesign the above translinear circuit, having the same input-output relation, employing PNP ánd NPN (thus not only NPN or only PNP) transistors, for operation from a 2-V supply. The parameters $I_{S,PNP}$ and $I_{S,NPN}$ are different and subject to absolute tolerances. The transistor's current-gain factor BF is large, but finite (i.e., not infinite).

i. First choose a correct translinear loop topology.
ii. Subsequently assign the correct collector currents (i.e., choose which current flows through which transistor).
iii. Finally, take care of appropriate biasing. Assume ideal biasing and input sources.

A straightforward approach would be to just replace diode connected transistors Q6 and Q4 by diode connected (and forward biased) PNP transistors.

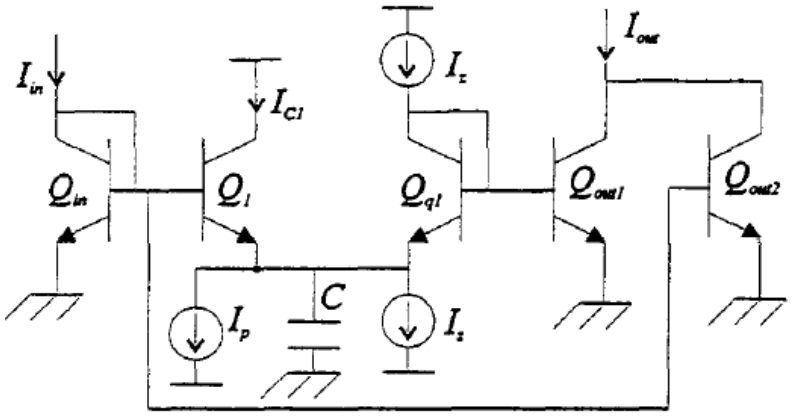
A more structured approach would be to re-use the translinear loop equations derived above and map them onto an NPN-PNP topology (for the 2^{nd}-order loop) and a PNP or an NPN topology (for the current mirror, the 1^{st}-order loop).

Many alternative circuits exist.

Question 3: Dynamic translinear and biasing circuits

Consider the dynamic translinear circuit (DTL) below. The circuit behaves as a non-ideal integrator.

a) Analyze its input-output relation in terms of I_z, I_p, C, I_{in} and I_{out}. All NPN transistors are identical.



First, analyze the DTL loop equation:

$$I_{cap} = CU_T\left(\frac{\dot{I}_{out1}}{I_{out1}} - \frac{\dot{I}_z}{I_z}\right) = CU_T\frac{\dot{I}_{out1}}{I_{out1}}$$

Second, analyze the STL loop equations:

$$I_{Qin}\cdot I_{Qq1} = I_{Q1}\cdot I_{out1}$$
$$I_{Qin} = I_{out2}$$

Third, write down the nodal equations (i.e, substitute the applied current into the (expressions for the) collector currents):

$$I_{in} = I_{Qin}$$
$$I_{C1} = I_{Q1} = I_p + I_{cap}$$
$$I_z = I_{Qq1}$$
$$I_{out1} = I_{Qout1}$$
$$I_{out2} = I_{Qout2}$$
$$I_{out} = I_{out1} + I_{out2}$$

Fourth, and finally, solve the above derived set of equations:

$$I_{in}\cdot I_z = \left(I_p + CU_T\frac{\dot{I}_{out1}}{I_{out1}}\right)\cdot I_{out1}$$
$$= I_p\cdot(I_{out} - I_{in}) + CU_T(\dot{I}_{out} - \dot{I}_{in})$$
$$I_{in}\cdot(I_z + I_p) + CU_T\dot{I}_{in} = I_p\cdot I_{out} + CU_T\dot{I}_{out}$$
$$H(s) = \frac{I_{out}(s)}{I_{in}(s)} = \frac{I_z + I_p + sCU_T}{I_p + sCU_T}$$
$$= \frac{1 + \frac{I_z}{I_p} + s\tau}{1 + s\tau}$$

The transfer function $H(s)$ (in the s-domain) thus has a pole and a zero.

b) Now redesign the above non-ideal integrator in such a way that its input-output relation becomes that of an ideal integrator:

$$I_{in} = \frac{CU_T}{I_z}\frac{dI_{out}}{dt}, \text{ or } I_{out} = \frac{I_z}{CU_T}\int I_{in}dt$$

NB. The (quiescent) current through Q_1 should be always positive.

There are two possible approaches.

1. If we first remove Qqout2, we obtain a lossy integrator, i.e., a low-pass filter, its input-output relation equal to:

$$I_{in} \cdot I_z = I_p \cdot I_{out} + CU_T \dot{I}_{out}$$

Subsequently, we can turn the above equation into that of an ideal integrator by addition of a fraction of I_{out} to the left term as follows.

$$\begin{aligned} I_{in} \cdot I_z &= CU_T \dot{I}_{out} \\ I_{in} \cdot I_z + I_p \cdot I_{out} &= I_p \cdot I_{out} + CU_T \dot{I}_{out} \\ \left(I_{in} + \tfrac{I_p}{I_z} \cdot I_{out}\right) \cdot I_z &= I_p \cdot I_{out} + CU_T \dot{I}_{out} \end{aligned}$$

To the circuit, this means that we add a fraction ($\frac{I_p}{I_z}$) of I_{out} to the input current in order to obtain the input-output relation of an ideal integrator.

2. Alternatively, we can start by the transfer function of an ideal integrator and do DTL synthesis as follows.

$$\begin{aligned} I_{in} \cdot I_z &= CU_T \dot{I}_{out} \\ I_{in} \cdot I_z + I_z \cdot I_{out} &= I_z \cdot I_{out} + CU_T \dot{I}_{out} \\ \left(I_{in} + I_{out}\right) \cdot I_z &= I_z \cdot I_{out} + CU_T \dot{I}_{out} \\ I_{cap} &= CU_T \frac{\dot{I}_{out}}{I_{out}} \\ \left(I_{in} + I_{out}\right) \cdot I_z &= I_z \cdot I_{out} + I_{cap} \cdot I_{out} \\ &= (I_z + I_{cap}) \cdot I_{out} \end{aligned}$$

The last equation is a correct translinear loop equation and can be mapped on a TL loop topology. The circuit design is completed by proper biasing.

c) If we wish to make the above integrator temperature independent what type of current source I_z do we need?

- A resistor
- A peaking current source
- A proportional-to-absolute-temperature current source
- A bandgap current reference

Give also a motivation for this.

As the time constant in the circuit equals CU_T/I_z, and U_T (= kT/q) is proportional to the absolute temperature (PTAT), we need to make I_z PTAT as well.

d) Design the chosen current source at transistor level, using BJT (NPN and/or PNP) transistors and resistors, operating from a 2-V supply and delivering 1mA at room temperature.

See the various circuit topologies in the reader and the answer to question 2.e)

e) **Bonus question.** If the output resistance (due to the Early effect) of the transistors in the current source designed above is low, give ways (the more the better) to reduce the dependence of I_z on the supply voltage.

We can apply (matched) resistors in the emitter lead of every transistor. We can apply circuit techniques (such as cascodes) to ensure that the collector voltages of transistors become constant (and equal for matched transistors). We can apply filtering on the supply lines. We can apply filtering on the current output. We can employ a voltage regulator between the supply voltage and the current source.