Exam Analog Integrated Circuit Design (ET 4252)
January 23, 2008
14:00-17:00h

This exam consists of three main questions. Please start on a new sheet of paper for each main question.

You are allowed to use a calculator and one piece of A4-sized paper with hand-written, non-copied personal notes.

Prefixes:

Giga	(G)	$= 10^{9}$
Mega	(M)	$= 10^{6}$
kilo	(k)	$= 10^{3}$
milli	(m)	$= 10^{-3}$
micro	(μ)	$= 10^{-6}$
nano	(n)	$= 10^{-9}$
pico	(p)	$= 10^{-12}$
femto	(f)	$= 10^{-15}$
atto	(a)	$= 10^{-18}$

$k = 1.38 \cdot 10^{-23}$ J/K (Boltzmann's constant)

$q = 1.60 \cdot 10^{-19}$ C (elementary charge)

$V_T = \frac{kT}{q} = 25.9\text{mV at } T = 300K$

Do not forget to put your name and study number on all material you hand in. And please turn off your mobile phone.

Good luck!

Dr.ir. Wouter A. Serdijn

Question 1: Design of a Voltage-Controlled Oscillator (VCO) for an Impulse-Radio Ultra-Wideband (UWB) Quadrature Downconverter

A negative resistance LC voltage-controlled oscillator is shown in Fig. 1.

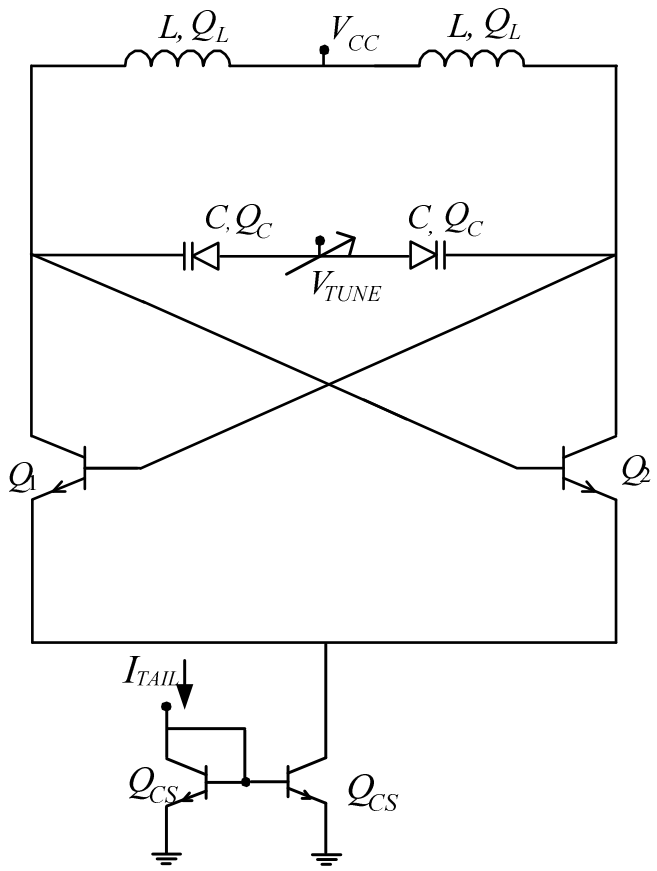


Figure 1: (simple) LC voltage-controlled oscillator.

The oscillator consists of a resonating LC tank, a cross-coupled transconductance amplifier (Q_1 and Q_2), and a bias current source (Q_{CS}). L stands for the tank inductance, Q_L for its quality factor, C for the varactor capacitance, Q_C for its quality factor, and I_{TAIL} for the bias tail current.

Determine the circuit parameter values of this oscillator in order to meet the requirements of the impulse-radio UWB quadrature downconverter.

The oscillator requirements for the impulse-radio UWB quadrature downconverter are:

- oscillation central frequency of 7.2 GHz
- phase noise better than –100 dBc/Hz at 1MHz offset from the oscillation central frequency
- peak amplitude of a differential oscillation voltage signal across the LC-tank around 400 mV
- power consumption drawn from a supply voltage of V_{CC} = 1.2V as low as possible

For a silicon technology chosen, inductors with quality factors of 20 and varactors with quality factors of 30 are available. The noise factor of the oscillator active part equals A=5.

Provide the following:

a) (5%) Derived expression for the LC-tank impedance (Z) at an offset angular frequency ($\Delta\omega$) from the oscillation angular frequency without considering inductor and capacitor losses.

$$C_{eq} = C/2$$

$$L_{eq} = 2L$$

$$Z(\omega_0) = \frac{1}{\frac{1}{j\omega_0 L_{eq}} + j\omega_0 C_{eq}} = \frac{j\omega_0 \cdot 2L}{1-\omega_0^2 LC}$$

$$Z(\omega_0 + \Delta\omega) = \frac{j(\omega_0 + \Delta\omega)\cdot 2L}{1-(\omega_0 + \Delta\omega)^2 LC}$$

$$\approx \frac{j\omega_0 \cdot 2L}{-2\omega_0 \cdot \Delta\omega \cdot LC} = -j\frac{\omega_0}{\Delta\omega}\cdot\frac{1}{C\cdot\omega_0} = -\frac{j}{\Delta\omega C} = -\frac{j\omega_0^2 L}{\Delta\omega}$$

where

ω_0 follows from $1-\omega_0^2 LC = 0$, hence $\omega_0 = \frac{1}{\sqrt{LC}}$

b) (15%) Derived expression for the LC-tank conductance (G_{TK}) at the oscillation frequency (f_0).

$R_C =$ series resistance of varactor

$R_L =$ series resistance of inductor

$$R_C = \frac{1}{\omega_0 C Q_C}$$

$$R_L = \frac{\omega_0 L}{Q_L}$$

$$R_{C,eq} = 2R_C = \frac{2}{\omega_0 C Q_C}$$

$$R_{L.eq} = 2R_L = \frac{2\omega_0 L}{Q_L}$$

$$G_{C,eq} = R_{C,eq} \cdot (\omega_0 C_{eq})^2$$

$$G_{L.eq} = \frac{R_L}{(\omega_0 L_{eq})^2}$$

$$G_{TK} = G_{C,eq} + G_{L.eq} = \frac{2}{\omega_0 C Q_C} \cdot \left(\frac{\omega_0 C}{2}\right)^2 + \frac{2\omega_0 L}{Q_L (2\omega_0 L)^2}$$

$$= \frac{\omega_0 C}{2Q_C} + \frac{1}{2\omega_0 L Q_L}$$

$$= \frac{1}{2}(\omega_0 C)^2 R_C + \frac{R_L}{2(\omega_0 L)^2}$$

$$= \omega_0 C\left(\frac{1}{2Q_L} + \frac{1}{2Q_C}\right) = \frac{1}{\omega_0 L}\left(\frac{1}{2Q_L} + \frac{1}{2Q_C}\right)$$

c) (5%) Expression for the oscillation frequency and oscillation condition.

Applying the Barkhausen criteria,

ω_0 follows from $1 - \omega_0^2 L_{eq} C_{eq} = 0$, hence $\omega_0 = \frac{1}{\sqrt{L_{eq} C_{eq}}} = \frac{1}{\sqrt{LC}}$,

and for the startup of the oscillation,

$|T(\omega_0)| \geq 1$, $T(\omega_0)$ being the loop gain of the oscillator

hence,

$$G_{diffpair} = \frac{g_m}{2} = \frac{I_{tail}}{4V_T} \geq G_{TK}$$

d) (10%) Derived expression for the phase noise of the oscillator. Model the noise contribution of the LC-tank to the phase noise by its loss resistance (R_{TK}), and the active part noise contribution by a factor AG_{TK}, A being its noise factor.

The noise (voltage) contribution (power spectral density) of the LC-tank, $S_{V,LC}$, equals

$$S_{V,LC} = 4kTG_{TK} \cdot \left|Z(\omega_0 + \Delta\omega)\right|^2 = 4kTG_{TK} \cdot \frac{1}{4G_{TK}^2 Q^2} \cdot \left(\frac{\omega_0}{\Delta\omega}\right)^2 = \frac{kT}{G_{TK}Q^2} \cdot \left(\frac{\omega_0}{\Delta\omega}\right)^2$$

The noise (voltage) contribution of the active part equals

$$S_{V,AP} = A \cdot S_{V,LC} = A \cdot 4kTG_{TK} \cdot \left|Z(\omega_0 + \Delta\omega)\right|^2 = \frac{A \cdot kT}{G_{TK}Q^2} \cdot \left(\frac{\omega_0}{\Delta\omega}\right)^2$$

$A = 5$ (given)

So for the phase noise it follows:

$$L(\Delta\omega) = \frac{1}{2} \frac{S_{V,LC} + S_{V,AP}}{v_s^2 / 2} = \frac{(1+A) \cdot kT}{G_{TK}Q^2 v_s^2} \cdot \left(\frac{\omega_0}{\Delta\omega}\right)^2 = \frac{(1+A) \cdot kTG_{TK}}{(\omega_0 C_{eq})^2 v_s^2} \cdot \left(\frac{\omega_0}{\Delta\omega}\right)^2$$

$$v_s = \frac{2I_{tail}}{\pi G_{TK}}$$

e) (35%) Possible values of inductance L, varactor capacitance C, and tail current I_{TAIL} for the oscillator requirements at the central oscillation frequency, using the results obtained in a)-d).

From the phase noise and signal swing requirements, we get

$L(1\text{MHz}) \le -100\text{dBc/Hz}$ and $v_s = 0.4\text{V}$.

Hence,

$$L(1\text{MHz}) = \frac{1}{2}\frac{S_{V,LC} + S_{V,AP}}{v_s^2/2} = \frac{(1+A)\cdot kT}{G_{TK}Q^2 v_s^2}\cdot\left(\frac{7.2\text{GHz}}{1\text{MHz}}\right)^2 \le 10^{-10}$$

$A = 5$

1) Q follows from a):

$$\frac{1}{Q} = \frac{1}{Q_L} + \frac{1}{Q_C} = \frac{1}{12}$$

$$v_s = \frac{2I_{tail}}{\pi G_{TK}} = 0.4\text{V}$$

2) $$G_{TK} = \frac{1}{\omega_0 L}\left(\frac{1}{2Q_L} + \frac{1}{2Q_C}\right) = \frac{\omega_0 C}{2}\left(\frac{1}{Q_L} + \frac{1}{Q_C}\right) = \frac{1}{2\omega_0 L}\frac{1}{Q}$$

$$\ge \frac{6kT}{Q^2 v_s^2}\cdot\left(\frac{7.2\text{GHz}}{1\text{MHz}}\right)^2 \cdot 10^{10} = 5.6\cdot 10^{-4}$$

3) $$L = \frac{L_{eq}}{2} = \frac{1}{2\omega_0 Q G_{TK}} \le 1.6\text{nH}$$

4) $$C = 2C_{eq} = \frac{2QG_{TK}}{\omega_0} \ge 0.30\text{pF}$$

or from: $$f_0 = \frac{1}{2\pi\sqrt{LC}} \Rightarrow C = \frac{1}{(2\pi f_0)^2 L} \ge 0.30\text{pF}$$

5) $$I_{tail} = \frac{\pi G_{TK} v_s}{2} = 0.35\text{mA}$$

Check whether the loop gain is larger than 1: $$\frac{g_m}{2G_{TK}} = \frac{I_{tail}}{4V_T G_{TK}} = 6.0 \ge 1$$

f) (15%) Values of minimum (C_{MIN}) and maximum (C_{MAX}) varactor capacitances to overcome the effects of 10% absolute tolerance on the inductors, varactors and transistors used.

From a) it follows: $$\omega_0 = \frac{1}{\sqrt{LC}}$$

So for a 10% change in L and C while ω_0 remains constant, LC has to remain constant. This entails:

$$LC = (L \pm \Delta L)(C \pm \Delta C)$$

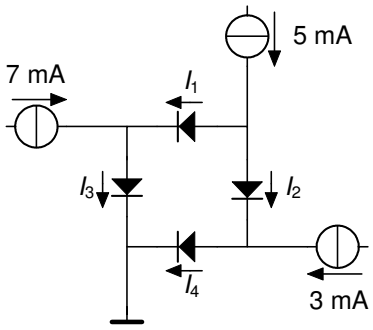
In the worst case condition, both the varactors and the inductors have been affected by the technology such that their values have altered in the same direction. In order to keep the product of L and C constant, we thus need to tune C in the opposite direction by 20% of its nominal value. For both negative and positive changes, the varactor values can be calculated, defining the entire tuning range.

g) (15%) Ways to reduce the power consumption (at the expense of phase noise, which is acceptable in this application) by *changing the LC-tank configuration* (not the active circuit).

Of course we can lower the tail current. This will give us a current (and thus power) saving of a little over 80%. For lower currents, the oscillator will shut off as there is not enough loop gain to sustain the oscillations. To reduce the current even further we need to reduce the tank conductance G_{TK}. This can be done by increasing the inductance L (and thus decreasing the capacitance C), by inserting components with larger quality factors (in place or in series/parallel), or by simply putting a number of identical LC tanks in series.

Question 2: Translinear and biasing circuits

a) A bridge rectifier can be viewed as a translinear loop. Assuming identical diodes, what are the four diode current values I_1, I_2, I_3 and I_4 in the figure below?



First, write down the translinear (TL) loop equation: $I_1 \cdot I_3 = I_2 \cdot I_4$

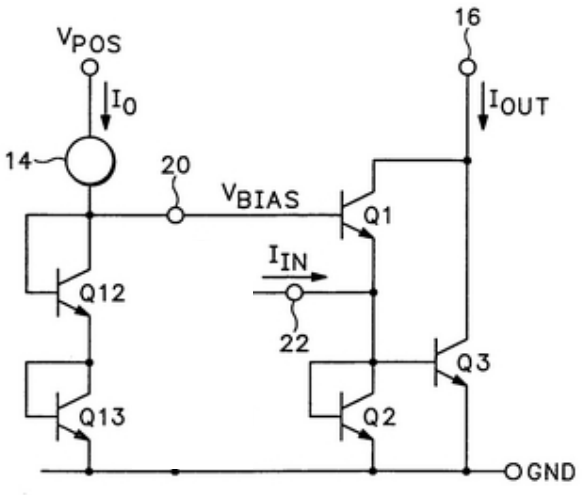
Second, write down the set of nodal equations:

$$I_1 + I_2 = 5 \text{ mA}$$
$$I_1 + 7 \text{ mA} = I_3$$
$$I_2 + 3 \text{ mA} = I_4$$

Third (and finally), the above set of 4 equations yields:

$$I_1 = 2 \text{ mA}$$
$$I_2 = 3 \text{ mA}$$
$$I_3 = 9 \text{ mA}$$
$$I_4 = 6 \text{ mA}$$

b) Analyze the output current I_{OUT} in terms of the input currents I_{IN} and I_O for the circuit below. All transistors are identical.



First (again), write down the translinear loop equations:

$$I_{12} \cdot I_{13} = I_1 \cdot I_2$$
$$I_3 = I_2$$

Second, write down the nodal equations:

$$I_O = I_{12} = I_{13}$$
$$I_2 = I_1 + I_{in}$$
$$I_{out} = I_1 + I_3 = I_1 + I_2$$

Third (and finally), solve the set of equations:

$$I_O^2 = \frac{I_{out} - I_{in}}{2} \frac{I_{out} + I_{in}}{2}$$
$$I_O^2 + \frac{I_{in}^2}{4} = \frac{I_{out}^2}{4}$$
$$I_{out} = \sqrt{4I_O^2 + I_{in}^2}$$

c) What restrictions hold for the magnitudes of currents I_O, I_{IN} and I_{OUT} in the above circuit? Write them in the form of inequalities, such as $I_x > 0$.

TL circuits will be functional as long as the collector current of all transistors are nonnegative. This yields:

$$I_O \geq 0$$
$$I_{out} \geq 0$$
$$I_{in} \in \mathbb{R}$$

We will now concentrate on the design of a current source that delivers I_{IN}. Assume its output current to be constant and equal to 3mA. Also assume I_O to be equal to 2mA.

d) What is the load impedance of the current source, i.e., what is the value of the (low-frequency) impedance seen by the current source that delivers I_{IN}?

The load impedance (resistance) of the current source, R_L, mentioned is the input impedance seen into the emitter of Q1, in parallel with the resistance of diode connected transistor Q2 ($1/g_m$), in parallel with the input resistance of Q3 (r_{pi}). The input resistance seen into the emitter of Q1 equals the effective emitter resistance of Q1 + the beta-reduced series resistances of diode connected transistors Q12 and Q13.

Neglecting r_{pi}, as it is much greater than $1/g_m$, we get:

$$\begin{aligned} R_L &= \frac{1}{g_{m2}} // \left(\frac{1}{g_{m1}} + \frac{1}{(\beta+1)g_{m12}} + \frac{1}{(\beta+1)g_{m13}} \right) \\ &\approx \frac{1}{g_{m2}} // \frac{1}{g_{m1}} \\ &= \frac{1}{g_{m2} + g_{m1}} \end{aligned}$$

which equals 5 ohm for I_1 = 1 mA and I_1 = 4 mA, respectively.

e) Design a single-transistor (i.e., having one transistor only and possibly a few passive components, such as resistors, capacitors, etc.) current source to implement I_{IN}. Make sure the current source is compliant with the voltage at node 22. Assume I_{IN} to be positive and that the supply voltage V_{pos} equals 2V.

There are a few alternatives here. They all employ a PNP transistor (possibly with an emitter series resistor or diode to the positive supply and some kind of (possibly nonlinear) voltage divider between the positive and negative rail to deliver an appropriate voltage at the base of the transistor. Possible elements of the voltage divider are resistors and/or diodes.

f) What is the value of its (low-frequency) output impedance?

If the emitter of the PNP transistor is connected to the positive supply, the output resistance equals $r_o = V_{AF}/I_C$, V_{AF} being the forward Early voltage (usually between 10 and 100 volt), I_C being the transistor collector current of 2 mA.

If the emitter of the PNP transistor is connected in series with a resistor and/or diode(s), the output impedance may (depending on the loop gain) increase to approximately $(\beta+1)r_o$.

g) Give two possible ways to improve the power-supply rejection of your current source implementation.

There are many possible ways to enhance the PSRR. They can be divided into two categories: one is based on the suppression of supply voltage variations before they reach the current source; the other is based on improving the current-source behavior of the current source.

In the first category we find: filtering the supply lines and having the supply regulated by a voltage source.

In the second category we find: stabilizing the resistive voltage divider by either making it nonlinear or by filtering the voltage across the upper resistor and increasing the resistance in the emitter lead or by applying a cascode, or by replacing the current source by a better version, e.g., the peaking current source.

As said, there are many possible ways.

h) Now redesign the above translinear circuit, having the same input-output relation, employing PNP ánd NPN (thus not only NPN or only PNP) transistors, for operation from a 1-V supply. The parameters $I_{S,PNP}$ and $I_{S,NPN}$ are different and subject to absolute tolerances. The transistor's current-gain factor BF is large, but finite (i.e., not infinite).

i. First choose a correct translinear loop topology.
ii. Subsequently assign the correct collector currents (i.e., choose which current flows through which transistor).
iii. Finally, take care of appropriate biasing. Assume ideal biasing and input sources.

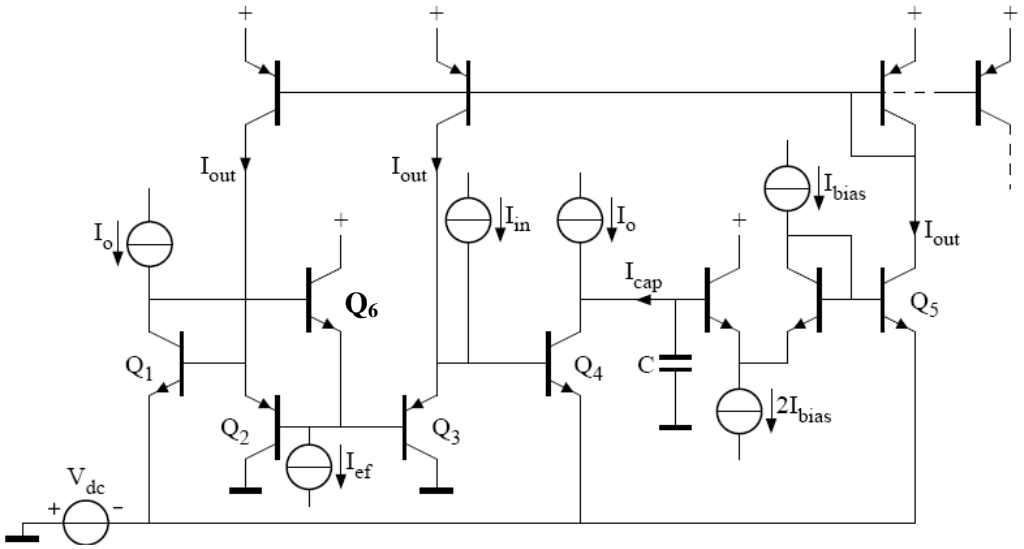
A structured approach involves re-using (or, if you are ambitious, redefining/ rewriting) the translinear loop equations derived above and map them onto an up-down (alternating) NPN-PNP topology (for the 2^{nd}-order loop) and an up-down PNP or an NPN topology (for the current mirror, the 1^{st}-order loop). It must be ensured that the correct (collector) currents flow through the transistors.

Many alternative circuits exist.

Question 3: Dynamic translinear and biasing circuits

Consider the 1-V dynamic translinear circuit (DTL) for hearing instruments below, designed by Serdijn, Broest, Mulder, van der Woerd and van Roermund.

a) Analyze its input-output relation in terms of I_o, I_{bias}, C, I_{in} and I_{out}. All NPN transistors are identical and all PNP transistors are identical.



First, analyze the DTL loop equation:

$$I_{cap} = -CU_T\left(\frac{\dot{I}_{out}}{I_{out}} - \frac{\dot{I}_{bias}}{I_{bias}} + \frac{\dot{I}_{bias}}{I_{bias}}\right) = -CU_T\frac{\dot{I}_{out}}{I_{out}}$$

Second, analyze the STL loop equation:

$$I_{Q1}\cdot I_{Q3} = I_{Q2}\cdot I_4$$

Third, write down the nodal equations (i.e, substitute the applied current into the (expressions for the) collector currents):

$$\begin{aligned} I_{Q1} &= I_o \\ I_{Q2} &= I_{out} \\ I_{Q3} &= I_{out} + I_{in} \\ I_{Q4} &= I_o + I_{cap} \end{aligned}$$

Fourth, and finally, solve the above derived set of equations:

$$\begin{aligned} I_o\cdot\left(I_{out} + I_{in}\right) &= I_{out}\cdot\left(I_o + I_{cap}\right) \\ &= I_{out}\cdot\left(I_o - CU_T\frac{\dot{I}_{out}}{I_{out}}\right) \\ &= I_{out}\cdot I_o - CU_T\dot{I}_{out} \\ I_o\cdot I_{in} &= -CU_T\dot{I}_{out} \\ H(s) &= \frac{I_{out}(s)}{I_{in}(s)} = -\frac{I_o}{sCU_T} \end{aligned}$$

The transfer function $H(s)$ (in the s-domain) thus has a pole in the origin and describes the transfer function of an ideal integrator.

b) What do you think is the purpose of Q_6 in the circuit?

Q_6 serves to provide the base currents of both Q_1 and Q_2 (together with I_{ef}) ánd serves as a voltage shift, so that the base-emitter voltage of Q_1 is close to zero. This reduces the Early effect for this transistor.

c) How would you choose the value of I_{bias} with respect to I_o and I_{out}? Write this in the form of inequalities.

First, an important observation is that I_{bias} does not appear in any of the above equations. The differential pair implements a voltage follower and as such thus reduces the influence of the base current (and its fluctuations) of Q_5. From inspection we can see that I_{bias} should be much larger than the base current of Q_5 but at the same time the base current of the transistors in the differential pair should be much smaller than the collector current of Q_4. A convenient value is that I_{bias} equals twice (two transistors!) times the geometric mean of the collector currents of Q_4 and Q_5, which both equal I_o. $Ibias = 2\ I_o$.

d) Now redesign the above circuit in such a way that its input-output relation becomes that of a lossy integrator:

$$I_{in} = \frac{CU_T}{I_O}\frac{dI_{out}}{dt} + I_{out}$$

NB. The (quiescent) current through *all the transistors* should be always positive (> 0).

There are two possible approaches.

1. We take the equation the above circuit implements.

$$\begin{aligned} I_o \cdot (I_{out} + I_{in}) &= I_{out} \cdot (I_o + I_{cap}) \\ &= I_{out} \cdot \left(I_o - CU_T \frac{\dot{I}_{out}}{I_{out}} \right) \\ &= I_{out} \cdot I_o - CU_T \dot{I}_{out} \end{aligned}$$

By removing the term $I_o \cdot I_{out}$ from the left hand side of this equation, we obtain the desired input-output relation of a lossy integrator.

2. Alternatively, we can start by the transfer function of an ideal integrator and do DTL synthesis as follows.

$$I_{in} = I_{out} + \frac{CU_T}{I_o}\dot{I}_{out}$$
$$I_o \cdot I_{in} = I_o \cdot I_{out} + CU_T \dot{I}_{out}$$
$$I_{cap} = CU_T \frac{\dot{I}_{out}}{I_{out}}$$
$$I_o \cdot I_{in} = I_{out} \cdot \left(I_o + I_{cap}\right)$$

The last equation is a correct translinear loop equation and can be mapped on a TL loop topology. The circuit design is completed by proper biasing.

e) If we wish to make the above integrator temperature independent what type of current source I_o do we need?
- A resistor
- A peaking current source
- A proportional-to-absolute-temperature current source
- A bandgap current reference

Give also a motivation for this.

As the time constant in the circuit equals CU_T/I_o, and U_T (= kT/q) is proportional to the absolute temperature (PTAT), we need to make I_o PTAT as well.

f) **Bonus question.** If the output resistance (due to the Early effect) of the transistors in the dynamic translinear circuit above is low, give ways (the more the better) to reduce the dependence of its input-output relation on the supply voltage.

We cannot apply (matched) resistors in the emitter lead of every transistor as this will influence the STL or DTL loop equations. We can apply circuit techniques (such as cascodes) to ensure that the collector voltages of transistors become constant (and equal for matched transistors). We can apply filtering on the supply lines. We can employ a voltage regulator between the supply voltage and the current source.