# Answers Exam Analog Integrated Circuit Design (ET 4252)
# August 28, 2008
# 14:00-17:00h

Delft University of Technology
Faculty of Electrical Engineering, M&CS
Dept. of Microelectronics
Section Electronic Circuit Design

This exam consists of three main questions. Please start on a new sheet of paper for each main question.

You are allowed to use a calculator and one piece of A4-sized paper with hand-written, non-copied personal notes.

Prefixes:

| | | |
|---|---|---|
| Giga | (G) | $= 10^{9}$ |
| Mega | (M) | $= 10^{6}$ |
| kilo | (k) | $= 10^{3}$ |
| milli | (m) | $= 10^{-3}$ |
| micro | (μ) | $= 10^{-6}$ |
| nano | (n) | $= 10^{-9}$ |
| pico | (p) | $= 10^{-12}$ |
| femto | (f) | $= 10^{-15}$ |
| atto | (a) | $= 10^{-18}$ |

$k = 1.38 \cdot 10^{-23}$ J/K (Boltzmann's constant)

$q = 1.60 \cdot 10^{-19}$ C (elementary charge)

$V_T = \frac{kT}{q} = 25.9\text{mV at } T = 300K$

Do not forget to put your name and study number on all material you hand in. And please turn off your mobile phone.

Good luck!

Dr.ir. Wouter A. Serdijn

# Question 1: Design of a Voltage-Controlled Oscillator (VCO) for an Impulse-Radio Ultra-Wideband (UWB) Quadrature Downconverter in CMOS technology

A MOS negative resistance LC voltage-controlled oscillator is shown in Fig. 1.

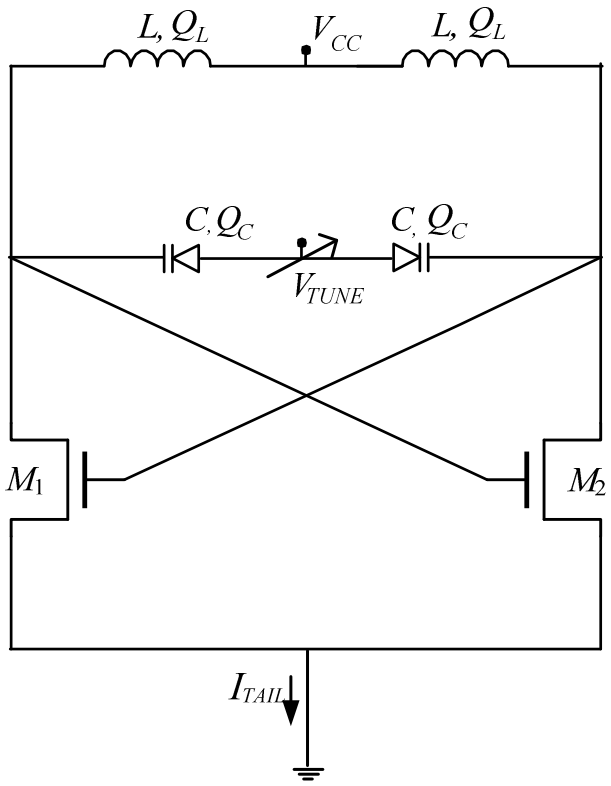



Figure 1: (simple) MOS LC voltage-controlled oscillator.

The oscillator consists of a resonating LC tank and a cross-coupled MOS transconductance amplifier ($M_1$ and $M_2$). $L$ stands for the tank inductance, $Q_L$ for its quality factor, $C$ for the varactor capacitance, $Q_C$ for its quality factor, and $I_{TAIL}$ for the tail current.

Determine the circuit parameter values of this oscillator in order to meet the requirements of the impulse-radio UWB quadrature downconverter.

The oscillator requirements for the impulse-radio UWB quadrature downconverter are:

- oscillation central frequency of 7.2 GHz
- phase noise better than –120 dBc/Hz at 10MHz offset from the oscillation central frequency
- peak amplitude of a differential oscillation voltage signal across the LC-tank around 400 mV
- power consumption drawn from a supply voltage of $V_{CC}$ = 1.2V as low as possible

For a silicon technology chosen, inductors with quality factors of 15 and varactors with quality factors of 30 are available. The noise factor of the oscillator active part equals $A$=7.

Provide the following:

a) Derived expression for the LC-tank impedance ($Z$) at an offset angular frequency ($\Delta\omega$) from the oscillation angular frequency without considering inductor and capacitor losses.

$$C_{eq} = C/2$$

$$L_{eq} = 2L$$

$$Z(\omega_0) = \frac{1}{\frac{1}{j\omega_0 L_{eq}} + j\omega_0 C_{eq}} = \frac{j\omega_0 \cdot 2L}{1-\omega_0^2 LC}$$

$$Z(\omega_0+\Delta\omega) = \frac{j(\omega_0+\Delta\omega)\cdot 2L}{1-(\omega_0+\Delta\omega)^2 LC}$$

$$\approx \frac{j\omega_0 \cdot 2L}{-2\omega_0 \cdot \Delta\omega \cdot LC} = -j\frac{\omega_0}{\Delta\omega}\cdot\frac{1}{C\cdot\omega_0} = -\frac{j}{\Delta\omega C} = -\frac{j\omega_0^2 L}{\Delta\omega}$$

where

$\omega_0$ follows from $1-\omega_0^2 LC = 0$, hence $\omega_0 = \frac{1}{\sqrt{LC}}$

b) Derived expression for the LC-tank conductance ($G_{TK}$) at the oscillation frequency ($f_0$).

$R_C =$ series resistance of varactor

$R_L =$ series resistance of inductor

$$R_C = \frac{1}{\omega_0 C Q_C}$$

$$R_L = \frac{\omega_0 L}{Q_L}$$

$$R_{C,eq} = 2R_C = \frac{2}{\omega_0 C Q_C}$$

$$R_{L.eq} = 2R_L = \frac{2\omega_0 L}{Q_L}$$

$$G_{C,eq} = R_{C,eq} \cdot (\omega_0 C_{eq})^2$$

$$G_{L.eq} = \frac{R_L}{(\omega_0 L_{eq})^2}$$

$$G_{TK} = G_{C,eq} + G_{L.eq} = \frac{2}{\omega_0 C Q_C} \cdot \left(\frac{\omega_0 C}{2}\right)^2 + \frac{2\omega_0 L}{Q_L (2\omega_0 L)^2}$$

$$= \frac{\omega_0 C}{2Q_C} + \frac{1}{2\omega_0 L Q_L}$$

$$= \frac{1}{2}(\omega_0 C)^2 R_C + \frac{R_L}{2(\omega_0 L)^2}$$

$$= \omega_0 C\left(\frac{1}{2Q_L} + \frac{1}{2Q_C}\right) = \frac{1}{\omega_0 L}\left(\frac{1}{2Q_L} + \frac{1}{2Q_C}\right)$$

c) Expression for the oscillation frequency and oscillation condition.

Applying the Barkhausen criteria,

$\omega_0$ follows from $1 - \omega_0^2 L_{eq} C_{eq} = 0$, hence $\omega_0 = \frac{1}{\sqrt{L_{eq} C_{eq}}} = \frac{1}{\sqrt{LC}}$,

and for the startup of the oscillation,

$|T(\omega_0)| \geq 1$, $T(\omega_0)$ being the loop gain of the oscillator

hence,

$$G_{diffpair} = \frac{g_m}{2} \geq G_{TK}$$

d) Derived expression for the phase noise of the oscillator. Model the noise contribution of the LC-tank to the phase noise by its loss resistance ($R_{TK}$), and the active part noise contribution by a factor $AG_{TK}$, $A$ being its noise factor.

The noise (voltage) contribution (power spectral density) of the LC-tank, $S_{V,LC}$, equals

$$S_{V,LC} = 4kTG_{TK} \cdot \left|Z(\omega_0 + \Delta\omega)\right|^2 = 4kTG_{TK} \cdot \frac{1}{4G_{TK}^2 Q^2} \cdot \left(\frac{\omega_0}{\Delta\omega}\right)^2 = \frac{kT}{G_{TK}Q^2} \cdot \left(\frac{\omega_0}{\Delta\omega}\right)^2$$

The noise (voltage) contribution of the active part equals

$$S_{V,AP} = A \cdot S_{V,LC} = A \cdot 4kTG_{TK} \cdot \left|Z(\omega_0 + \Delta\omega)\right|^2 = \frac{A \cdot kT}{G_{TK}Q^2} \cdot \left(\frac{\omega_0}{\Delta\omega}\right)^2$$

$A = 7$ (given)

So for the phase noise it follows:

$$L(\Delta\omega) = \frac{1}{2}\frac{S_{V,LC} + S_{V,AP}}{v_s^2/2} = \frac{(1+A) \cdot kT}{G_{TK}Q^2 v_s^2} \cdot \left(\frac{\omega_0}{\Delta\omega}\right)^2 = \frac{(1+A) \cdot kTG_{TK}}{(\omega_0 C_{eq})^2 v_s^2} \cdot \left(\frac{\omega_0}{\Delta\omega}\right)^2$$

$$v_s = \frac{2I_{tail}}{\pi G_{TK}}$$

e) Possible values of inductance $L$, varactor capacitance $C$, and tail current $I_{TAIL}$ for the oscillator requirements at the central oscillation frequency, using the results obtained in a)-d).

From the phase noise and signal swing requirements, we get $L(10\text{MHz}) \le -120\text{dBc/Hz}$ and $v_s = 0.4\text{V}$.

Hence,

$$L(10\text{MHz}) = \frac{1}{2}\frac{S_{V,LC} + S_{V,AP}}{v_s^2/2} = \frac{(1+A)\cdot kT}{G_{TK}Q^2 v_s^2}\cdot\left(\frac{7.2\text{GHz}}{10\text{MHz}}\right)^2 \le 10^{-12}$$

$A = 7$

1) $Q$ follows from a):

$$\frac{1}{Q} = \frac{1}{Q_L} + \frac{1}{Q_C} = \frac{1}{10}$$

$$v_s = \frac{2I_{tail}}{\pi G_{TK}} = 0.4\text{V}$$

2) $$G_{TK} = \frac{1}{\omega_0 L}\left(\frac{1}{2Q_L} + \frac{1}{2Q_C}\right) = \frac{\omega_0 C}{2}\left(\frac{1}{Q_L} + \frac{1}{Q_C}\right) = \frac{1}{2\omega_0 L}\frac{1}{Q}$$

$$\ge \frac{8kT}{Q^2 v_s^2}\cdot\left(\frac{7.2\text{GHz}}{10\text{MHz}}\right)^2 \cdot 10^{12} = 1.1\cdot 10^{-3}$$

3) $$L = \frac{L_{eq}}{2} = \frac{1}{2\omega_0 Q G_{TK}} \le 1.0\text{nH}$$

4) $$C = 2C_{eq} = \frac{2QG_{TK}}{\omega_0} \ge 0.47\text{pF}$$

or from: $$f_0 = \frac{1}{2\pi\sqrt{LC}} \Rightarrow C = \frac{1}{(2\pi f_0)^2 L} \ge 0.47\text{pF}$$

5) $$I_{tail} = \frac{\pi G_{TK} v_s}{2} = 0.67\text{mA}$$

NB: additionally, the loop gain should be larger than 1: $\frac{g_m}{2G_{TK}} \ge 1$

f) Values of minimum ($C_{MIN}$) and maximum ($C_{MAX}$) varactor capacitances to overcome the effects of 10% absolute tolerance on the inductors, varactors and transistors used.

From a) it follows: $\omega_0 = \frac{1}{\sqrt{LC}}$

So for a 10% change in $L$ and $C$ while $\omega_0$ remains constant, $LC$ has to remain constant. This entails:

$LC = (L \pm \Delta L)(C \pm \Delta C)$

In the worst case condition, both the varactors and the inductors have been affected by the technology such that their values have altered in the same direction. In order to keep the product of $L$ and $C$ constant, we thus need to tune $C$ in the opposite direction by 20% of its nominal value. For both negative and

positive changes, the varactor values can be calculated, defining the entire tuning range.

g) Ways to reduce the power consumption (at the expense of phase noise, which is acceptable in this application) by *changing the LC-tank configuration* (not the active circuit).

Of course we can lower the tail current. This will give us a current (and thus power) saving. For lower currents however, the oscillator will shut off as there is not enough loop gain to sustain the oscillations. To reduce the current even further we need to reduce the tank conductance $G_{TK}$. This can be done by increasing the inductance $L$ (and thus decreasing the capacitance $C$), by inserting components with larger quality factors (in place or in series/parallel), or by simply putting a number of identical LC tanks in series.

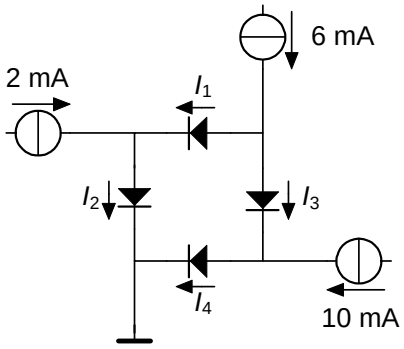
h) Ways to reduce the noise factor of the oscillator active part, while keeping the bias current the same, *by changing the size of M1 and M2* (not the LC tank). Also explain how the minimum noise factor is restricted by the supply voltage.

The noise factor is proportional to the transconductance factor $g_m$ of the MOS transistors used. Lowering $g_m$ while still fulfilling the oscillation conditions is thus the way to reduce the noise factor of the entire oscillator. This can be done by, e.g., reducing the tail current. This, first of all, is not allowed, as the question clearly mentions “while keeping the bias current the same”, but is not of much help either, as it will also reduce the voltage swing across the LC tank, thereby deteriorating the phase noise. The correct answer here is **to reduce the W/L of the MOS transistor**, as this will also lower the $g_m$.

As the gate-source voltage increases for increasing lengths, the supply voltage will set an upper limit to the gate-source voltage and thus a lower limit to the $g_m$.

# Question 2: Translinear and biasing circuits

a) A bridge rectifier can be viewed as a translinear loop. Assuming identical diodes, what are the four diode current values $I_1$, $I_2$, $I_3$ and $I_4$ in the figure below?




First, write down the translinear (TL) loop equation: $I_1 \cdot I_2 = I_3 \cdot I_4$

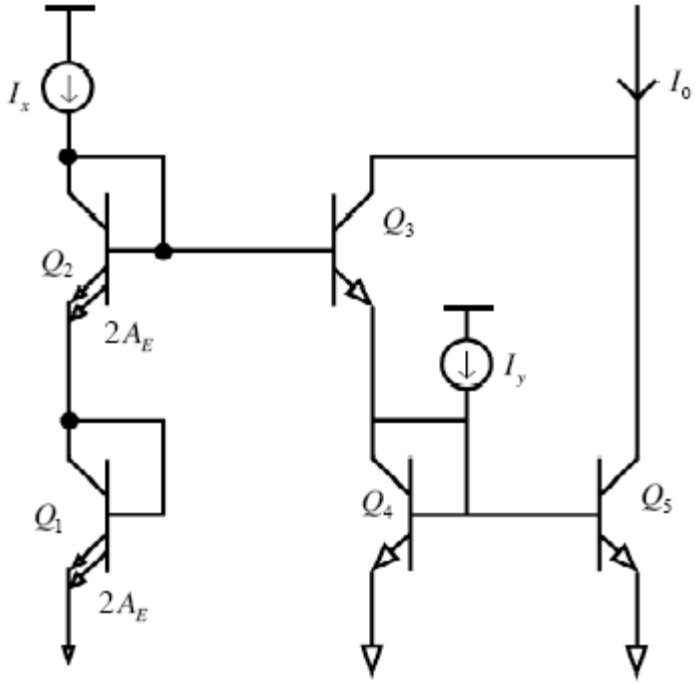
Second, write down the set of nodal equations:

$$I_1 + I_3 = 6\ \text{mA}$$
$$I_1 + 2\ \text{mA} = I_2$$
$$I_3 + 10\ \text{mA} = I_4$$

Third (and finally), the above set of 4 equations yields:

$$I_1 = 4\ \text{mA}$$
$$I_2 = 6\ \text{mA}$$
$$I_3 = 2\ \text{mA}$$
$$I_4 = 12\ \text{mA}$$

b) Analyze the output current $I_o$ in terms of the input currents $I_x$ and $I_y$ for the circuit below. All transistors are equivalent; only $Q_1$ and $Q_2$ have a doubled emitter area.




First (again), write down the translinear loop equations:

$$\frac{I_1}{2}\cdot\frac{I_2}{2} = I_3 \cdot I_4$$
$$I_4 = I_5$$

Second, write down the nodal equations:

$$I_x = I_1 = I_2$$
$$I_4 = I_3 + I_y$$
$$I_{out} = I_3 + I_5 = I_3 + I_4$$

Third (and finally), solve the set of equations:

$$\frac{I_x^2}{4} = \frac{I_{out} - I_y}{2}\frac{I_{out} + I_y}{2}$$
$$\frac{I_x^2}{4} + \frac{I_y^2}{4} = \frac{I_{out}^2}{4}$$
$$I_{out} = \sqrt{I_x^2 + I_y^2}$$

c) What restrictions hold for the magnitudes of the input currents $I_x$ and $I_y$ in the above circuit? Write them in the form of inequalities, such as $I_y > 0$.

TL circuits will be functional as long as the collector current of all transistors are nonnegative. This yields:

$$I_x \geq 0$$
$$I_{out} \geq 0$$
$$I_y \in \square$$

We will now concentrate on the design of the lower current source $I_y$. Assume its output current to be constant and equal to 1 mA. Also assume $I_x$ to be equal to 1 mA.

d) What is the load impedance of the current source, i.e., what is the value of the (low-frequency) impedance seen by current source $I_y$?

The load impedance (resistance) of the current source, $R_L$, mentioned is the input impedance seen into the emitter of Q3, in parallel with the resistance of diode connected transistor Q4 ($1/g_m$), in parallel with the input resistance of Q5 ($r_{pi}$). The input resistance seen into the emitter of Q3 equals the effective emitter resistance of Q3 + the beta-reduced series resistances of diode connected transistors Q1 and Q2.

Neglecting $r_{pi}$, as it is much greater than $1/g_m$, we get:

$$R_L = \frac{1}{g_{m4}} // \left( \frac{1}{g_{m3}} + \frac{1}{(\beta+1)g_{m2}} + \frac{1}{(\beta+1)g_{m1}} \right)$$
$$\approx \frac{1}{g_{m4}} // \frac{1}{g_{m3}}$$
$$= \frac{1}{g_{m4} + g_{m3}}$$

which equals 18 ohm for $I_x$ = 1 mA and $I_y$ = 1 mA, respectively.

e) Design a single-transistor (i.e., having one transistor only and possibly a few passive components, such as resistors, capacitors, etc.) current source to implement $I_y$.

There are a few alternatives here. They all employ a PNP transistor (possibly with an emitter series resistor or diode to the positive supply and some kind of (possibly nonlinear) voltage divider between the positive and negative rail to deliver an appropriate voltage at the base of the transistor. Possible elements of the voltage divider are resistors and/or diodes.

f) What is the value of its (low-frequency) output impedance?

If the emitter of the PNP transistor is connected to the positive supply, the output resistance equals $r_o = V_{AF}/I_C$, $V_{AF}$ being the forward Early voltage (usually between 10 and 100 volt), $I_C$ being the transistor collector current of 1 mA.

If the emitter of the PNP transistor is connected in series with a resistor and/or diode(s), the output impedance may (depending on the loop gain) increase to approximately $(\beta+1)r_o$.

g) Give two possible ways to improve the power-supply rejection of your current source implementation.

There are many possible ways to enhance the PSRR. They can be divided into two categories: one is based on the suppression of supply voltage variations before

they reach the current source; the other is based on improving the current-source behavior of the current source.

In the first category we find: filtering the supply lines and having the supply regulated by a voltage source.

In the second category we find: stabilizing the resistive voltage divider by either making it nonlinear or by filtering the voltage across the upper resistor and increasing the resistance in the emitter lead or by applying a cascode, or by replacing the current source by a better version, e.g., the peaking current source.

As said, there are many possible ways.

h) Now redesign the above translinear circuit, having the same input-output relation, employing PNP and NPN transistors, for operation from a 1-V supply. The parameters $I_{S,PNP}$ and $I_{S,NPN}$ are different and subject to absolute tolerances. The transistor's current-gain factor *BF* is large, but finite (i.e., not infinite).
    i. First choose a correct translinear loop topology.
    ii. Subsequently assign the correct collector currents (i.e., choose which current flows through which transistor).
    iii. Finally, take care of appropriate biasing. Assume ideal biasing and input sources.

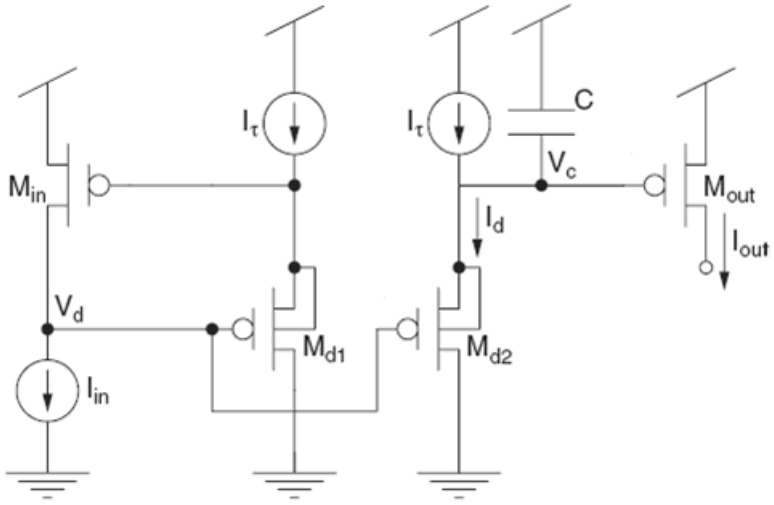
A structured approach involves re-using (or, if you are ambitious, redefining/ rewriting) the translinear loop equations derived above and map them onto an up-down (alternating) NPN-PNP topology (for the $2^{nd}$-order loop) and an up-down PNP or an NPN topology (for the current mirror, the $1^{st}$-order loop). It must be ensured that the correct (collector) currents flow through the transistors.

Many alternative circuits exist.

# Question 3: Dynamic translinear and biasing circuits

Consider the dynamic translinear circuit (DTL) below. The circuit behaves as a non-ideal integrator.

a) Analyze its input-output relation in terms of $I_\tau$, $C$, $I_{in}$ and $I_{out}$. All PMOS transistors are identical and operate in weak inversion (i.e., follow an exponential input-output relation: $I_d = I_s \exp(V_{gs}/V_T)$, $I_d$ being the drain current, $I_s$ being a technology and size dependent specific current, $V_{gs}$ being the gate-source voltage and $V_T$ being the thermal voltage $kT/q$, approximately 26 mV at room temperature).




First, analyze the DTL loop equation:

$$I_{cap} = CU_T \frac{\dot{I}_{Mout}}{I_{Mout}}$$

Second, analyze the STL loop equation:

$$I_{Min} \cdot I_{Md1} = I_{Md2} \cdot I_{Mout}$$

Third, write down the nodal equations (i.e, substitute the applied current into the (expressions for the) collector currents):

$$I_{Min} = I_{in}$$
$$I_{Md1} = I_\tau$$
$$I_{Md2} = I_\tau + I_{cap}$$
$$I_{Mout} = I_{out}$$

Fourth, and finally, solve the above derived set of equations:

$$
\begin{aligned}
I_{in} \cdot I_\tau &= I_{out}\left(I_\tau + I_{cap}\right) \\
&= I_{out} \cdot \left(I_\tau + CU_T \frac{\dot{I}_{out}}{I_{out}}\right) \\
&= I_{out} \cdot I_\tau + CU_T \dot{I}_{out} \\
I_{in} &= I_{out} + \frac{CU_T}{I_\tau}\dot{I}_{out} \\
H(s) &= \frac{I_{out}(s)}{I_{in}(s)} = \frac{1}{1 + sCU_T / I_\tau}
\end{aligned}
$$

The transfer function $H(s)$ (in the $s$-domain) thus has a pole in the left half-plane and describes the transfer function of a lossy integrator.

b) Now redesign the above non-ideal integrator in such a way that its input-output relation becomes that of an ideal integrator:

$$I_{in} = \frac{CU_T}{I_\tau}\frac{dI_{out}}{dt}, \text{ or } I_{out} = \frac{I_\tau}{CU_T}\int I_{in}dt$$

NB: the drain currents should always remain positive. Capacitance currents are bipolar, i.e., positive and negative, as the average current equals zero.

One way is to introduce an additional term, a current, in the translinear loop equation, such that the above analysis becomes:

$$
\begin{aligned}
\left(I_{in} + I_{out}\right) \cdot I_\tau &= I_{out}\left(I_\tau + I_{cap}\right) \\
&= I_{out} \cdot \left(I_\tau + CU_T \frac{\dot{I}_{out}}{I_{out}}\right) \\
&= I_{out} \cdot I_\tau + CU_T \dot{I}_{out} \\
I_{in} &= \frac{CU_T}{I_\tau}\dot{I}_{out} \\
H(s) &= \frac{I_{out}(s)}{I_{in}(s)} = \frac{I_\tau}{sCU_T}
\end{aligned}
$$

This can be done, for instance, by feeding back the output current $I_{out}$ to the input via a current mirror. A couple of alternative solutions exist.

c) If we wish to make the above integrator temperature independent what type of current source $I_\tau$ do we need and why?

- A resistor
- A peaking current source
- **A proportional-to-absolute-temperature current source**
- A bandgap current reference

As the time constant in the circuit equals $CU_T/I_\tau$, and $U_T$ (= $kT/q$) is proportional to the absolute temperature (PTAT), we need to make $I_\tau$ PTAT as well.

d) Design the chosen current source at transistor level, using MOS (NMOS and/or PMOS) transistors and resistors, operating from a 2-V supply and delivering 1mA at room temperature.

The simplest circuits comprise a linear current mirror (employing only two transistors) and a nonlinear current mirror, the output transistor having a resistor in its source lead and a larger aspect (W/L) ratio. See the reader for the basic principle of PTAT current sources. The current mirrors can be improved (at the expense of voltage headroom) by applying common-gate stages (cascodes).

Alternatively, peaking current sources can be used *as part of* the nonlinear current mirror in the PTAT current source. The basic idea of all PTAT current sources is that a difference in gate-source voltages (in weak inversion) that arises from different current densities, appears across a resistor, thus producing a current that is proportional to the absolute temperature.

e) **Bonus question.** If the output resistance (due to channel length modulation) of the transistors in the current source designed above is low, give ways (the more the better) to reduce the dependence of $I_\tau$ on the supply voltage.

We cannot apply (matched) resistors in the source lead of every transistor as this will influence the STL or DTL loop equations. We can apply circuit techniques (such as cascodes) to ensure that the collector voltages of transistors become constant (and equal for matched transistors). We can apply filtering on the supply lines. We can employ a voltage regulator between the supply voltage and the current source.