

Answers Exam Analog Integrated Circuit Design (ET 4252)
January 21, 2009
14:00-17:00h

This exam consists of three main questions. Please start on a new sheet of paper for each main question.

You are allowed to use a calculator and one piece of A4-sized paper with handwritten, non-copied personal notes.

Prefixes:

| | | |
|-----------------|---|------------|
| Giga (G) | = | 10^9 |
| Mega (M) | = | 10^6 |
| kilo (k) | = | 10^3 |
| milli (m) | = | 10^{-3} |
| micro (μ) | = | 10^{-6} |
| nano (n) | = | 10^{-9} |
| pico (p) | = | 10^{-12} |
| femto (f) | = | 10^{-15} |
| atto (a) | = | 10^{-18} |

$$k = 1.38 \cdot 10^{-23} \text{ J/K (Boltzmann's constant)}$$

$$q = 1.60 \cdot 10^{-19} \text{ C (elementary charge)}$$

$$V_T = \frac{kT}{q} = 25.9 \text{ mV at } T = 300 \text{ K}$$

Do not forget to put your name and study number on all material you hand in. And please turn off your mobile phone.

Good luck!

Dr.ir. Wouter A. Serdijn

Question 1: Design of a Voltage-Controlled Oscillator (VCO) for an Impulse-Radio Ultra-Wideband (UWB) Quadrature Downconverter

A negative resistance LC voltage-controlled oscillator is shown in Fig. 1.

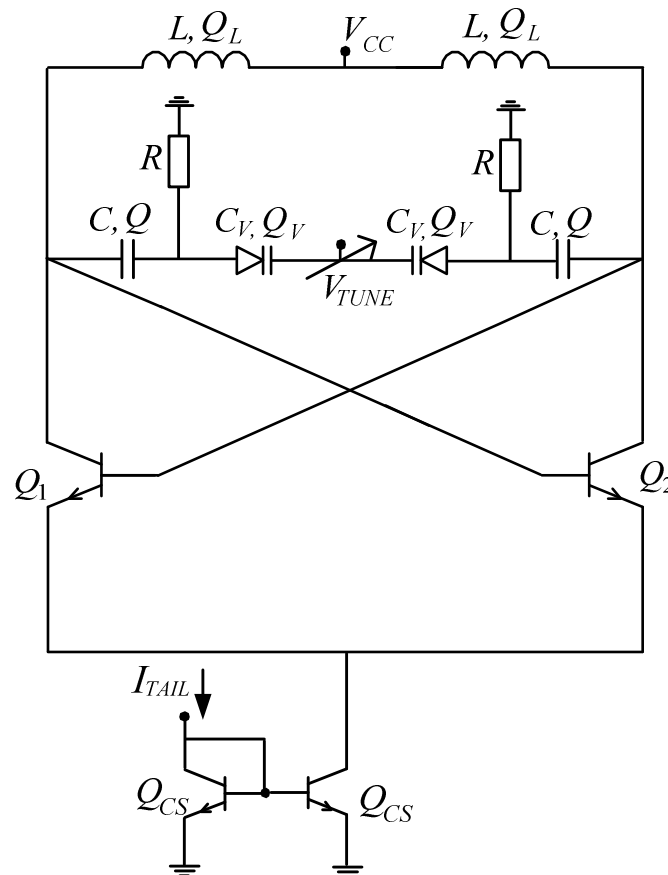


Figure 1: (simple) LC voltage-controlled oscillator.

The oscillator consists of a resonating LC tank, a cross-coupled transconductance amplifier (Q_1 and Q_2), and a bias current source (Q_{CS}). L stands for the tank inductance, Q_L for its quality factor, C for the additional tank capacitance, Q_C for its quality factor, C_V for the varactor capacitance ($C=C_V$ at the oscillation central frequency), Q_{CV} for its quality factor, and I_{TAIL} for the bias tail current. The resistors R are for biasing purposes only, are very large and thus negligible.

Determine the circuit parameter values of this oscillator in order to meet the requirements of the impulse-radio UWB quadrature downconverter.

The oscillator requirements for the impulse-radio UWB quadrature downconverter are:

- oscillation central frequency of 1.8 GHz
- phase noise better than -120 dBc/Hz at 10MHz offset from the oscillation central frequency
- peak amplitude of a differential oscillation voltage signal across the LC-tank around 400 mV
- power consumption drawn from a supply voltage of $V_{CC} = 1.2V$ as low as possible

For a silicon technology chosen, inductors with quality factors of 15, varactors with quality factors of 30 and capacitors with quality factors 40 are available. The noise factor of the oscillator active part equals $A=5$.

Provide the following:

- a) (5%) Derived expression for the LC-tank impedance (Z) at an offset angular frequency ($\Delta\omega$) from the oscillation angular frequency without considering inductor and capacitor losses.

$$C_{eq} = \frac{1}{2} \cdot \frac{C \cdot C_V}{C + C_V} = \frac{C}{4}$$

$$L_{eq} = 2L$$

$$Z(\omega_0) = \frac{1}{\frac{1}{j\omega_0 L_{eq}} + j\omega_0 C_{eq}} = \frac{j\omega_0 \cdot 2L}{1 - \omega_0^2 LC/2}$$

$$Z(\omega_0 + \Delta\omega) = \frac{j(\omega_0 + \Delta\omega) \cdot 2L}{1 - (\omega_0 + \Delta\omega)^2 LC/2}$$

$$\approx \frac{j\omega_0 \cdot 2L}{-2\omega_0 \cdot \Delta\omega \cdot LC/2} = -j \frac{\omega_0}{\Delta\omega} \cdot \frac{2}{C \cdot \omega_0} = -\frac{2j}{\Delta\omega C} = -\frac{j\omega_0^2 L}{\Delta\omega}$$

where

$$\omega_0 \text{ follows from } 1 - \omega_0^2 LC/2 = 0, \text{ hence } \omega_0 = \frac{1}{\sqrt{LC/2}}$$

- b) (15%) Derived expression for the LC-tank conductance (G_{TK}) at the oscillation frequency (f_0).

R_{CV} = series resistance of varactor

R_C = series resistance of capacitor

R_L = series resistance of inductor

$$R_C = \frac{1}{\omega_0 C Q_C} = \frac{1}{\omega_0 C_V Q_C}$$

$$R_{CV} = \frac{1}{\omega_0 C_V Q_{CV}}$$

$$R_L = \frac{\omega_0 L}{Q_L}$$

$$Q_C = \frac{4}{3} Q_{CV}$$

$$R_{C,eq} = 2R_C + 2R_{CV} = \frac{2}{\omega_0 C Q_C} + \frac{2}{\omega_0 C_V Q_{CV}} = \frac{7}{2\omega_0 C_V Q_{CV}}$$

$$R_{L,eq} = 2R_L = \frac{2\omega_0 L}{Q_L}$$

$$G_{C,eq} = R_{C,eq} \cdot (\omega_0 C_{eq})^2$$

$$G_{L,eq} = \frac{R_{L,eq}}{(\omega_0 L_{eq})^2}$$

$$G_{TK} = G_{C,eq} + G_{L,eq} = \frac{7}{2\omega_0 C Q_{CV}} \cdot \left(\frac{\omega_0 C}{4}\right)^2 + \frac{2\omega_0 L}{Q_L (2\omega_0 L)^2}$$

$$= \frac{7\omega_0 C}{32Q_{CV}} + \frac{1}{2\omega_0 L Q_L}$$

$$= \frac{7}{32} (\omega_0 C)^2 R_{CV} + \frac{R_L}{2(\omega_0 L)^2}$$

$$= \omega_0 C \left(\frac{1}{4Q_L} + \frac{7}{32Q_{CV}} \right) = \frac{1}{2\omega_0 L} \left(\frac{1}{Q_L} + \frac{7}{8Q_{CV}} \right) = \frac{1}{2\omega_0 L} \frac{1}{Q_{TK}}$$

- c) (5%) Expression for the oscillation frequency and oscillation condition.

Applying the Barkhausen criteria,

$$\omega_0 \text{ follows from } 1 - \omega_0^2 L_{eq} C_{eq} = 0, \text{ hence } \omega_0 = \frac{1}{\sqrt{L_{eq} C_{eq}}} = \frac{1}{\sqrt{LC/2}},$$

and for the startup of the oscillation,

$$|T(\omega_0)| \geq 1, T(\omega_0) \text{ being the loop gain of the oscillator}$$

hence,

$$G_{diffpair} = \frac{g_m}{2} = \frac{I_{tail}}{4V_T} \geq G_{TK}$$

- d) (10%) Derived expression for the phase noise of the oscillator. Model the noise contribution of the LC-tank to the phase noise by its loss resistance (R_{TK}), and the active part noise contribution by a factor AG_{TK} , A being its noise factor.

The noise (voltage) contribution (power spectral density) of the LC-tank, $S_{V,LC}$, equals

$$S_{V,LC} = 4kTG_{TK} \cdot |Z(\omega_0 + \Delta\omega)|^2 = 4kTG_{TK} \cdot \frac{1}{4G_{TK}^2 Q_{TK}^2} \cdot \left(\frac{\omega_0}{\Delta\omega}\right)^2 = \frac{kT}{G_{TK} Q_{TK}^2} \cdot \left(\frac{\omega_0}{\Delta\omega}\right)^2$$

The noise (voltage) contribution of the active part equals

$$S_{V,AP} = A \cdot S_{V,LC} = A \cdot 4kTG_{TK} \cdot |Z(\omega_0 + \Delta\omega)|^2 = \frac{A \cdot kT}{G_{TK} Q_{TK}^2} \cdot \left(\frac{\omega_0}{\Delta\omega}\right)^2$$

$A = 5$ (given)

So for the phase noise it follows:

$$L(\Delta\omega) = \frac{1}{2} \frac{S_{V,LC} + S_{V,AP}}{v_s^2 / 2} = \frac{(1+A) \cdot kT}{G_{TK} Q_{TK}^2 v_s^2} \cdot \left(\frac{\omega_0}{\Delta\omega}\right)^2 = \frac{(1+A) \cdot kTG_{TK}}{(\omega_0 C_{eq})^2 v_s^2} \cdot \left(\frac{\omega_0}{\Delta\omega}\right)^2$$

$$v_s = \frac{2I_{tail}}{\pi G_{TK}}$$

- e) (35%) Possible values of inductance L , capacitance C , varactor capacitance C_V , and tail current I_{TAIL} for the oscillator requirements at the central oscillation frequency, using the results obtained in a)-d).

From the phase noise and signal swing requirements, we get

$$L(10\text{MHz}) \leq -120\text{dBc/Hz and } v_s = 0.4\text{V.}$$

Hence,

$$L(10\text{MHz}) = \frac{1}{2} \frac{S_{V,LC} + S_{V,AP}}{v_s^2/2} = \frac{(1+A) \cdot kT}{G_{TK} Q_{TK}^2 v_s^2} \cdot \left(\frac{1.8\text{GHz}}{10\text{MHz}} \right)^2 \leq 10^{-12}$$

$$A = 5$$

1) Q_{TK} follows from b):

$$\frac{1}{Q_{TK}} = \frac{1}{Q_L} + \frac{7}{8Q_{CV}} = \frac{1}{15} + \frac{7}{240} = \frac{23}{240} \approx \frac{1}{10}$$

$$v_s = \frac{2I_{tail}}{\pi G_{TK}} = 0.4\text{V}$$

$$2) G_{TK} = \frac{1}{2\omega_0 L} \left(\frac{1}{Q_L} + \frac{7}{8Q_{CV}} \right) = \omega_0 C \left(\frac{1}{4Q_L} + \frac{7}{32Q_{CV}} \right) = \frac{1}{2\omega_0 L} \frac{1}{Q_{TK}}$$

$$\leq \frac{6kT}{Q_{TK}^2 v_s^2} \cdot \left(\frac{1.8\text{GHz}}{10\text{MHz}} \right)^2 \cdot 10^{12} = 5.0 \cdot 10^{-5}$$

$$3) L = \frac{L_{eq}}{2} = \frac{1}{2\omega_0 Q_{TK} G_{TK}} \leq 88\text{nH}$$

$$4) C = 4C_{eq} = \frac{4Q_{TK} G_{TK}}{\omega_0} \geq 0.18\text{pF}$$

$$\text{or from: } f_0 = \frac{1}{2\pi\sqrt{LC/2}} \Rightarrow C = \frac{2}{(2\pi f_0)^2 L} \geq 0.18\text{pF}$$

$$5) I_{tail} = \frac{\pi G_{TK} v_s}{2} = 31\mu\text{A}$$

NB: additionally, the loop gain should be larger than 1: $\frac{g_m}{2G_{TK}} = \frac{I_{tail}}{4V_T G_{TK}} = 6 \geq 1$

- f) (15%) Values of minimum (C_{MIN}) and maximum (C_{MAX}) varactor capacitances to overcome the effects of 10% absolute tolerance on the inductors, capacitors, varactors and transistors used.

From a) it follows: $\omega_0 = \frac{1}{\sqrt{L \frac{C \cdot C_V}{C+C_V}}}$

So for a 10% change in L , C and C_V while ω_0 remains constant,

$L \frac{C \cdot C_V}{C+C_V}$ has to remain constant. This entails:

$$L \frac{C \cdot C_V}{C+C_V} = (L \pm \Delta L) \frac{(C \pm \Delta C) \cdot (C_V \pm \Delta C_V \mp \delta C_V)}{C \pm \Delta C + C_V \pm \Delta C_V \mp \delta C_V}$$

if $\Delta = +10\%$

$$\frac{1}{2} = 1.1 \cdot \frac{1.1 \cdot (1.1 - \delta)}{2.2 - \delta}$$

$$\delta = \frac{2 \cdot 1.1^3 - 2.2}{2 \cdot 1.1^2 - 1} = 0.33 = 33\%$$

if $\Delta = -10\%$

$$\frac{1}{2} = 0.9 \cdot \frac{0.9 \cdot (0.9 - \delta)}{1.8 - \delta}$$

$$\delta = \frac{2 \cdot 0.9^3 - 1.8}{2 \cdot 0.9^2 - 1} = -0.55 = -55\%$$

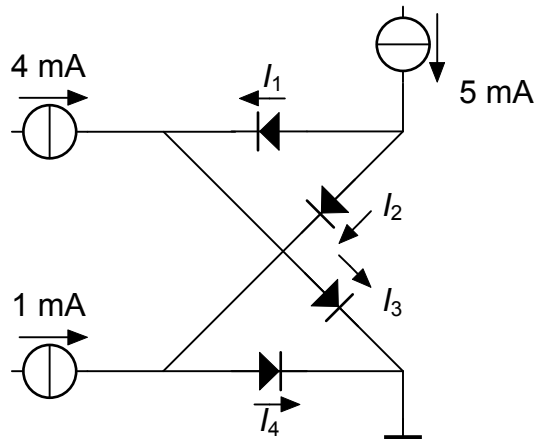
In the worst case condition, the capacitor, the varactors and the inductors have been affected by the technology such that their values have altered in the same direction (sign of Δ). In order to keep the product of L and C constant, we thus need to tune C_{eq} in the opposite direction by approximately 20% of its nominal value. Since $C = C_V$, we thus need to tune C_V by approximately 40%. For both negative and positive changes, the varactor values can be calculated, defining the entire tuning range.

- g) (15%) Ways to reduce the power consumption (at the expense of phase noise, which is acceptable in this application) by *changing the LC-tank configuration* (not the active circuit).

Of course we can lower the tail current. This will give us a current (and thus power) saving. For lower currents however, the oscillator will shut off as there is not enough loop gain to sustain the oscillations. To reduce the current even further we need to reduce the tank conductance G_{TK} . This can be done by increasing the inductance L (and thus decreasing the capacitance C_{eq}), by inserting components with larger quality factors (in place or in series/parallel), or by simply putting a number of identical LC tanks in series.

Question 2: Translinear and biasing circuits

- a) A double-sided rectifier can be viewed as a translinear loop. Assuming identical diodes, what are the four diode current values I_1 , I_2 , I_3 and I_4 in the figure below?



First, write down the translinear (TL) loop equation: $I_1 \cdot I_3 = I_2 \cdot I_4$

Second, write down the set of nodal equations:

$$I_1 + I_2 = 5 \text{ mA}$$

$$I_1 + 4 \text{ mA} = I_3$$

$$I_2 + 1 \text{ mA} = I_4$$

Third (and finally), the above set of 4 equations yields:

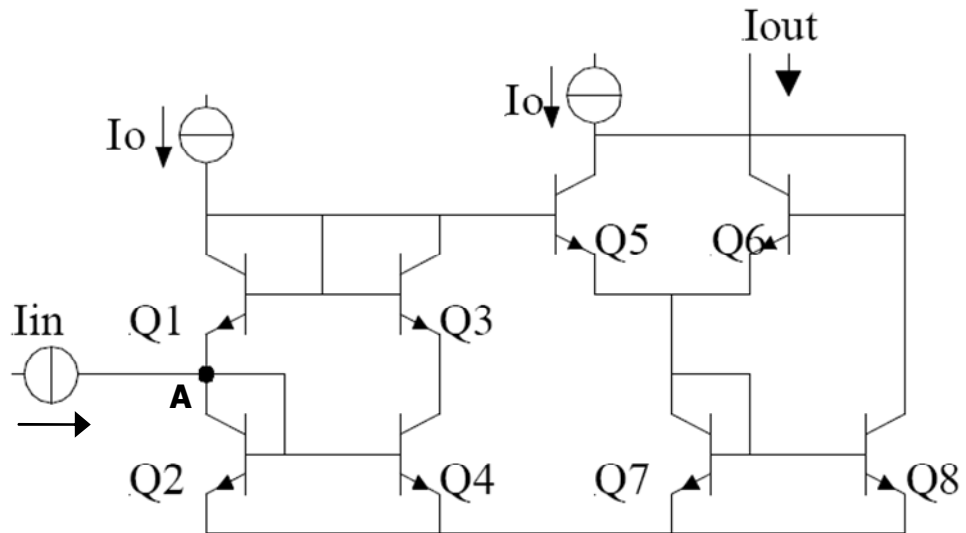
$$I_1 = 2 \text{ mA}$$

$$I_2 = 3 \text{ mA}$$

$$I_3 = 6 \text{ mA}$$

$$I_4 = 4 \text{ mA}$$

- b) Analyze the output current I_{out} in terms of the input currents I_{in} and I_O for the circuit below. All transistors are identical.
1. Write down the translinear loop equation(s)
 2. Write down the nodal equations
 3. Solve the (set of) equation(s)



First (again), write down the translinear loop equations:

$$I_1 \cdot I_2 = I_5 \cdot I_7$$

$$I_2 = I_4$$

$$I_7 = I_8$$

NB: there are only 3 translinear loops.

Second, write down the nodal equations:

$$I_o = I_1 + I_3 = I_1 + I_4$$

$$I_o = I_5 + I_8$$

$$I_7 = I_5 + I_6$$

$$I_{out} = I_6$$

$$I_2 = I_1 + I_{in}$$

Third (and finally), solve the set of equations:

$$I_1 = \frac{I_o - I_{in}}{2}$$

$$I_2 = \frac{I_o + I_{in}}{2}$$

$$I_5 = \frac{I_o - I_{out}}{2}$$

$$I_7 = \frac{I_o + I_{out}}{2}$$

$$\frac{I_o - I_{in}}{2} \cdot \frac{I_o + I_{in}}{2} = \frac{I_o - I_{out}}{2} \cdot \frac{I_o + I_{out}}{2}$$

$$I_o^2 - I_{in}^2 = I_o^2 - I_{out}^2$$

$$I_{in}^2 = I_{out}^2$$

$$I_{out} = |I_{in}|$$

- c) What restrictions hold for the magnitudes of currents I_O , I_{in} and I_{OUT} in the above circuit? Write them in the form of inequalities, such as $I_x > 0$.

TL circuits will be functional as long as the collector current of all transistors are nonnegative. This yields:

$$\begin{aligned} I_o &\geq 0 \\ I_o &\geq I_{out} \geq 0 \\ I_o &\geq I_{in} \geq -I_o \end{aligned}$$

- d) What do you think is the role of transistor Q3?

Q3 does **not** appear in any of the translinear loops. It is diode-connected and just relays the current of Q4. The effect of Q3 is that the potential at the collector of Q4 now is more or less equal to the potential at node A. As a consequence, the current mirror Q3-Q4 does not suffer from the Early effect (if any).

We will now concentrate on the design of a current source that delivers I_{in} . Assume its output current to be constant and equal to 2mA. Also assume I_O to be equal to 4mA.

- e) What is the load impedance of the current source, i.e., what is the value of the (low-frequency) impedance seen by the current source that delivers I_{in} ?

The load impedance (resistance) of the current source, R_L , mentioned is the input impedance seen into the emitter of Q1, in parallel with the resistance of diode connected transistor Q2 ($1/g_m$), in parallel with the input resistance of Q4 (r_{pi}). The input resistance seen into the emitter of Q1 equals the effective emitter resistance of Q3 + the input resistance of Q5 + the beta-enhanced (i.e., times beta) resistance of diode connected transistor Q7 ($1/g_m$). Note that (diode connected) Q3 hardly affects this value as it appears in series with r_o of Q4.

Neglecting r_{pi} , as it is much greater than $1/g_m$, we get:

$$\begin{aligned} R_L &= \frac{1}{g_{m2}} // \left(\frac{1}{g_{m1}} + r_{\pi 5} + \frac{\beta + 1}{g_{m7}(\beta + 1)} \right) // r_{\pi 4} \\ &\approx \frac{1}{g_{m2}} \end{aligned}$$

which equals 8.6 ohm for $I_2 = 3$ mA.

- f) Design a single-transistor (i.e., having one transistor only and possibly a few passive components, such as resistors, capacitors, etc.) current source to implement I_{in} . Make sure the current source is compliant with the voltage at node A. Assume I_{in} to be positive and that the (positive) supply voltage equals 2V.

There are a few alternatives here. They all employ a PNP transistor (possibly with an emitter series resistor or diode to the positive supply and some kind of (possibly nonlinear) voltage divider between the positive and negative rail to deliver an appropriate voltage at the base of the transistor. Possible elements of the voltage divider are resistors and/or diodes.

NB. You should also calculate the values of the components used in the current source.

g) What is the value of its (low-frequency) output impedance?

If the emitter of the PNP transistor is connected to the positive supply, the output resistance equals $r_o = V_{AF}/I_C$, V_{AF} being the forward Early voltage (usually between 10 and 100 volt), I_C being the transistor collector current of 1 mA.

If the emitter of the PNP transistor is connected in series with a resistor and/or diode(s), the output impedance may (depending on the loop gain) increase to approximately $(\beta + 1)r_o$.

h) Give two possible ways to improve the power-supply rejection of your current source implementation.

There are many possible ways to enhance the PSRR. They can be divided into two categories: one is based on the suppression of supply voltage variations before they reach the current source; the other is based on improving the current-source behavior of the current source.

In the first category we find: filtering the supply lines and having the supply regulated by a voltage source.

In the second category we find: stabilizing the resistive voltage divider by either making it nonlinear or by filtering the voltage across the upper resistor and increasing the resistance in the emitter lead or by applying a cascode, or by replacing the current source by a better version, e.g., the peaking current source.

As said, there are many possible ways.

Redesign of the entire translinear circuit.

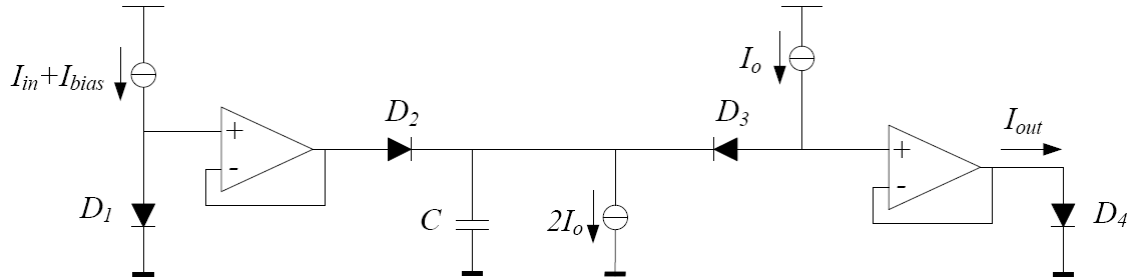
i) Now redesign the above translinear circuit, having the same input-output relation, employing (more than one) PNP and (multiple) NPN (thus not only NPN or only PNP) transistors, for operation from the same 2V supply. The parameters $I_{S,PNP}$ and $I_{S,NPN}$ are different and subject to absolute tolerances. The transistor's current-gain factor BF is large, but finite (i.e., not infinite).

A structured approach involves re-using (or, if you are ambitious, redefining/rewriting) the translinear loop equations derived above and map them onto an up-down (alternating) NPN-PNP topology (for the 2nd-order loop, Q1-Q2-Q5-Q7) and an up-down PNP or an NPN topology for any required current mirrors, realizing 1st-order loops. It must be ensured that the correct (collector) currents flow through the transistors.

Many alternative circuits exist.

Question 3: Dynamic translinear and biasing circuits

Consider the 1-V dynamic translinear circuit (DTL) for high-frequency operation below, designed by Haddad and Serdijn, in line with the original idea of Adams (Picture taken from the upcoming book of Haddad and Serdijn, to appear with Springer, March 2009).



- a) Analyze its input-output relation in terms of I_o , I_{bias} , C , I_{in} and I_{out} . All diodes are identical.

First, analyze the DTL loop equation:

$$I_{cap} = CU_T \left(\frac{\dot{I}_{d4}}{I_{d4}} - \frac{\dot{I}_{d3}}{I_{d3}} \right)$$

Second, analyze the STL loop equation:

$$I_{d1} \cdot I_{d3} = I_{d2} \cdot I_{d4}$$

Third, write down the nodal equations (i.e, substitute the applied current into the (expressions for the) collector currents):

$$I_{d1} = I_{in} + I_{bias}$$

$$I_{d2} = I_o + I_{cap}$$

$$I_{d3} = I_o$$

$$I_{d4} = I_{out}$$

Fourth, and finally, solve the above derived set of equations:

$$\begin{aligned} (I_{in} + I_{bias}) \cdot I_o &= I_{out} (I_o + I_{cap}) \\ &= I_{out} \cdot \left(I_o + CU_T \frac{\dot{I}_{out}}{I_{out}} \right) \\ &= I_{out} \cdot I_o + CU_T \dot{I}_{out} \\ I_{in} + I_{bias} &= I_{out} + \frac{CU_T}{I_o} \dot{I}_{out} \\ &= I'_{in} \\ H(s) &= \frac{I_{out}(s)}{I'_{in}(s)} = \frac{1}{1 + sCU_T/I_o} \end{aligned}$$

The transfer function $H(s)$ (in the s -domain) thus has a pole in the left half-plane and describes the transfer function of a lossy integrator.

- b) 1. In what configuration are the operational amplifiers connected in the circuit? 2. What do you think is the purpose of the operational amplifiers in the circuit?

The operation amplifiers are connected in *voltage-follower* configuration. Their purpose is to implement a correct translinear loop of diode voltages, without loading (taking away additional current from) diodes $D1$ and $D3$.

- c) How would you choose the value of I_{bias} with respect to I_{in} , I_o and I_{out} ? Write this in the form of inequalities.

First, it is important to realize that all diode currents should be always positive in order for the circuit to work correctly. I_{bias} thus determines the maximum peak current of I_{in} , as I_{d1} equals the sum of I_{bias} and I_{in} . As I_{out} is the low-pass filtered version of the sum of I_{bias} and I_{in} , viz. I_{d1} , I_{bias} thus also defines the maximum signal (current) swing the filter delivers. Needless to say that I_{bias} must be positive. I_o is not related to the choice of I_{bias} in any way.

- d) Now redesign the above circuit in such a way that its input-output relation becomes that of an ideal integrator:

$$I_{in} = \frac{CU_T}{I_o} \frac{dI_{out}}{dt}$$

NB1. The (quiescent) current through *all the diodes* should be always positive (> 0).

NB2. Assume that, apart from the diodes, also NPN transistors are present that exhibit an identical exponential input-output relation. These may be included in the design.

One way is to introduce an additional term, a current, in the translinear loop equation, such that the above analysis becomes:

$$\begin{aligned} (I_{in} + I_{out}) \cdot I_o &= I_{out} (I_o + I_{cap}) \\ &= I_{out} \cdot \left(I_o + CU_T \frac{\dot{I}_{out}}{I_{out}} \right) \\ &= I_{out} \cdot I_o + CU_T \dot{I}_{out} \\ I_{in} &= \frac{CU_T}{I_o} \dot{I}_{out} \\ H(s) &= \frac{I_{out}(s)}{I_{in}(s)} = \frac{I_o}{sCU_T} \end{aligned}$$

This can be done, for instance, by feeding back the output current I_{out} to the input via a current mirror and use this current to replace I_{bias} .

A couple of alternative solutions exist.

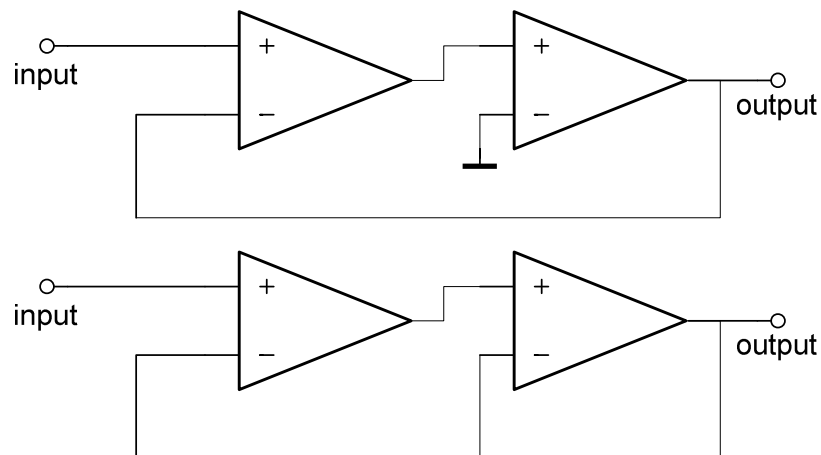
- e) If we wish to make the above integrator temperature independent what type of current source I_o do we need?
- A resistor
 - A peaking current source
 - **A proportional-to-absolute-temperature current source**
 - A bandgap current reference

Give also a motivation for this.

As the time constant in the circuit equals CU_T/I_o , and $U_T (= kT/q)$ is proportional to the absolute temperature (PTAT), we need to make I_o PTAT as well.

- f) **Bonus question.** If the output resistance of (closed-loop) operational amplifiers in the dynamic translinear circuit above is too high for correct circuit operation, give ways (the more the better) to reduce it.

One way is to connect another opamp in cascade in the active part of the voltage follower. Two possible topologies are depicted below (the first one being the best).



Voltage followers employing two operational amplifiers to reduce the output impedance

Another way is to enhance the loop gain of the opamps being used by increasing the bias current, using cascode stages, adding gain stages, etc.