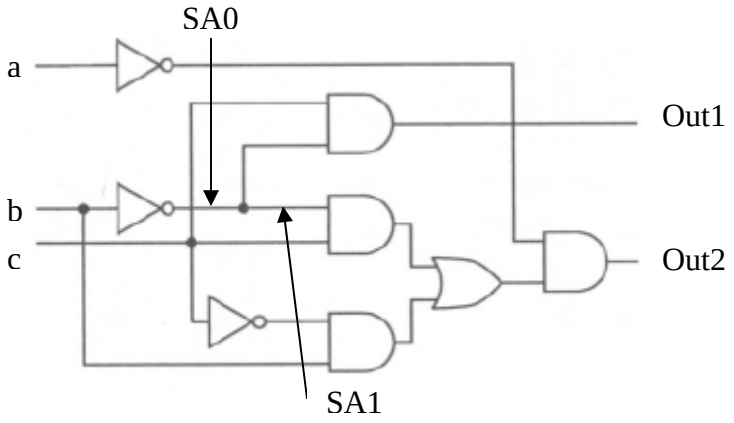
VLSI Test Technology and Reliability ET4076
Assignment 1
Deadline: Feb 24, 2010

Given the following circuit.



1. What is the difference between a defect and a fault model? Give an example.
2. How many test vectors will be needed if functional testing will be used to test the above circuit?
3. What is the number of potential fault sites in the above circuit?
4. Derive the equivalence collapsed set. What is the collapsed ratio? (optional: you may also use dominant fault collapsing)
5. Enumerate the minimal set of single SAF that must be tested according to Checkpoint Theorem. Notice that a single input gate (inverter) has to be treated as continuation of its input line. Use also the concept of equivalence faults to further reduce the number of faults that have to be tested?
6. Compute the combinational SCOAP testability measures (both controllability and observability).
7. Use D algorithm to generate a test pattern for SA0 shown in the circuit? If applicable, how does D algorithm use testability measurements for decision-making?
8. Use D algorithm to generate a test pattern for SA1 shown in the circuit? If applicable, how does D algorithm use testability measurements for decision-making?
9. Use now PODEM algorithm to generate the test pattern for the SA1.
10. *(Optional). Given the minimal fault set of question 5, determine (e.g., using the fault simulator concept or ATPG) the required test set for such fault set.*

Q	1	2	3	4	5	6	7	8	9	10
pt	5	5	5	10	15	15	15	15	15	Can increase you score with 20