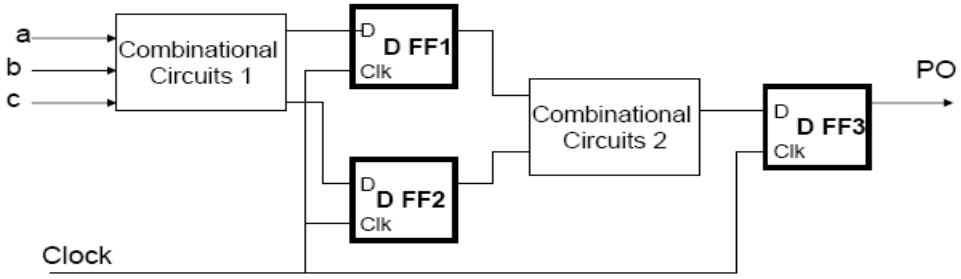
VLSI Test Technology and Reliability ET4076
Assignment 2
Deadline: April 1, 2010

1. **Delay Testing.**
   Given the following circuit.

   Consider the path C – F – G in the circuit above.
   a. Derive a test for a rising transition at C.
   b. Will the above test work if a falling transition is applied at B?
   c. Sketch all signal waveforms for the situation in (b) when all gates have one unit of delay. Assuming that the permitted delay for the circuit is 2.5 units; interpret the result of the test. Can you locate the faulty path?
   d. What is the difference between testing of a delay fault (e.g., rising transition at C) and testing of stuck at fault (e.g., C stuck at 1)?

2. **Scan design**
   Given the following circuit which consists of two combinational blocks and three D flip-flops. The Combinational circuit 1 consists of 150 gates while combinational circuit 2 consists of 200 gates.



   a. Convert the circuit above into full scan circuit. Redraw the circuit with the scan design and show all the signals and modifications done in the original circuit. Describe clearly the steps you followed to realize the scan design.
   b. Explain how you can test the original circuit using the developed scan design
   c. Assume that we want to test SAF in combinational circuit 2. Describe how you can do this.
   d. What is the benefit of your Scan design? And what are the costs? How much is the area overhead?

Q	1				2			
	a	b	c	d	a	b	c	d
pt	10	5	10	5	30	10	15	15