DC reference sources

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Electronics

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DIMES

Overview

- Voltage sources (Main part) ⇨ Basics and Implementations
- Current sources ⇨ Basics and Implementations

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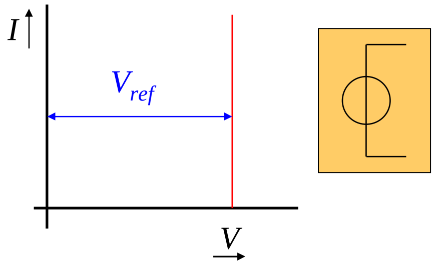
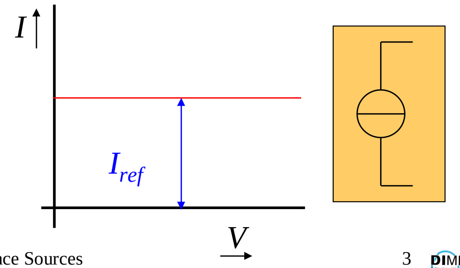
Ideal voltage source

- Output voltage *independent* of I, T, ……..



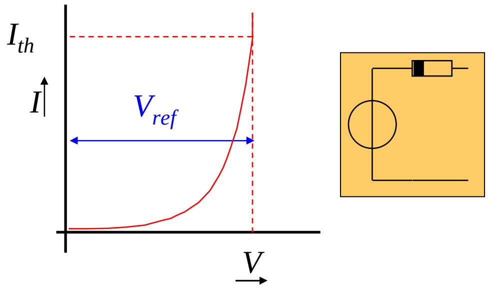
Ideal current source

- Output current *independent* of V, T, ……..



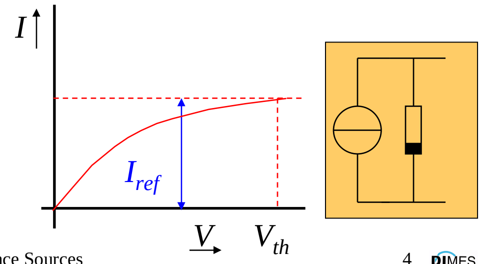
Practical voltage source

- Beyond I_{th} a voltage source
- Output voltage *depends on* external parameters



Practical current source

- Beyond V_{th} a current source
- Output current *depends on* external parameters



Quality Aspects V,I Source

- Output impedance
- Noise level

→ Power

- Temperature dependency

→ Circuit design

Power Supply Rejection Ratio

- V,I source powered by a *power source*

PSRR is a measure for the *sensitivity* of the output quantity (V,I) for *power supply variations*

$$PSRR = 20 \cdot {}^{10}\log\left(\frac{dV_{\text{supply}}}{dV_{\text{ref}}}\frac{V_{\text{ref}}}{V_{\text{supply}}}\right)$$

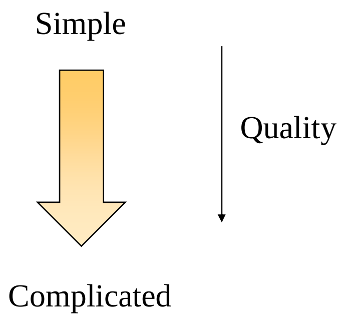
unit: dB

$$PSRR = 20 \cdot {}^{10}\log\left(\frac{dV_{\text{supply}}}{dI_{\text{ref}}}\frac{I_{\text{ref}}}{V_{\text{supply}}}\right)$$

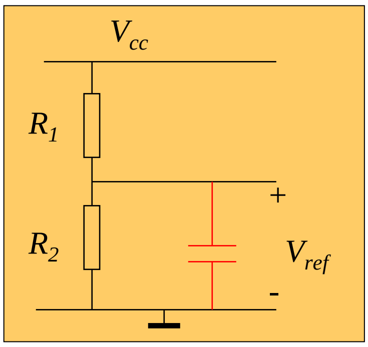
unit: dB

- The larger the better

Voltage sources



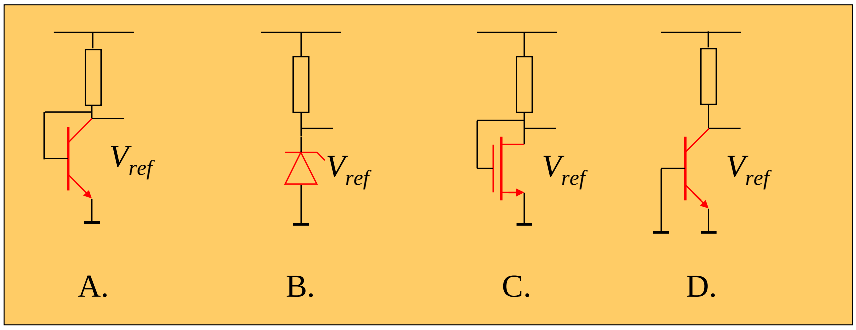
Most simple voltage source



- Accuracy depends on V_{cc} and matching of R_1 and R_2
- Low output impedance and low noise costs *power* or a *capacitor*
- *PSRR* = 1
  Can also be improved by *capacitor*

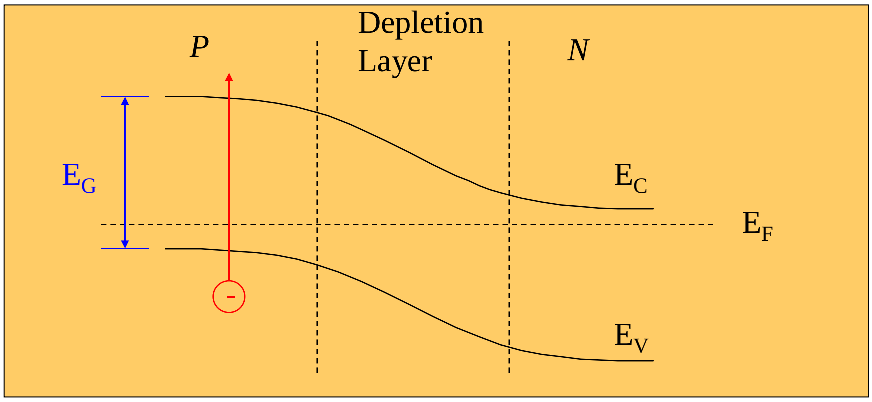
$$V_{ref} = V_{cc} \frac{R_2}{R_1 + R_2}$$

Non-linear voltage divider

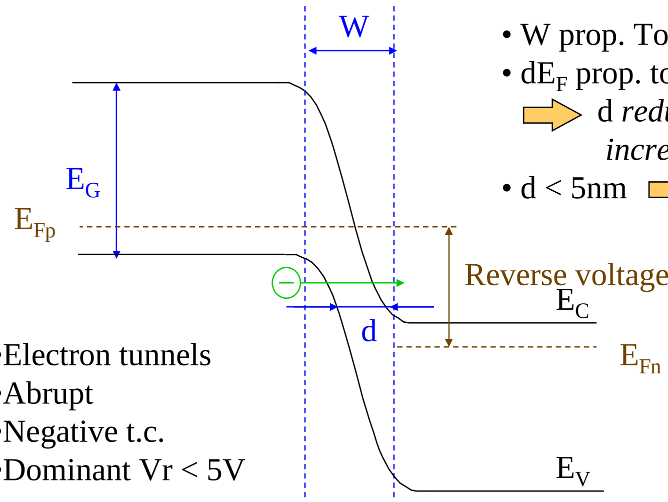


A. Diode-connected transistor
B. Zener diode ⇨ Zener and Avalanche breakdown
C. Normally-off FET (NMOS)
D. Bipolar transistor at punch-through

Zener breakdown



Electron must gain energy equal to E_G for a transition from valence band to conduction band

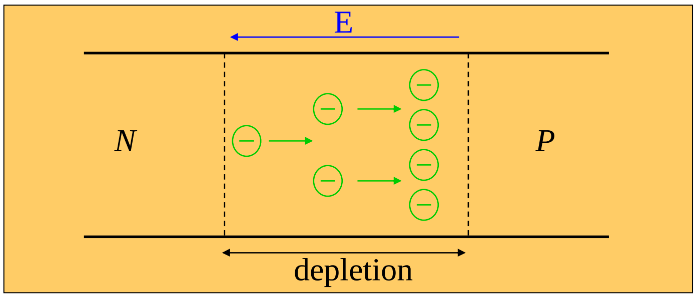


- W prop. To $\sqrt{|V_r|}$
- dE$_F$ prop. to $|V_r|$

  ⇨ d *reduces* for *increasing* V_r
- d < 5nm ⇨ tunneling

- Electron tunnels
- Abrupt
- Negative t.c.
- Dominant Vr < 5V

Avalanche breakdown



- Electrons are accelerated by E-field
- Speed high enough ⇨ other electrons are made free

Requirements:

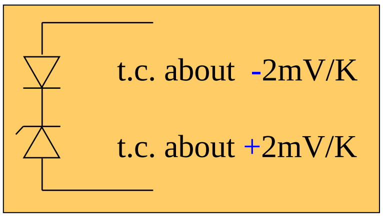
- E-field must be high enough
- Free path length must be high enough

Positive t.c.
Dominant Vr > 6V

Temperature compensation Zener diode

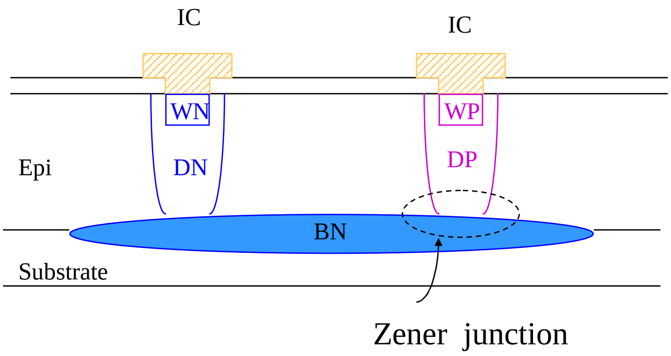
•Use a Zener diode with V_{br} = 5 .. 6V (5.6V)
⇨ Both Avalanche and Zener breakdown occur
⇨ Temperature behavior reduced

•Zener diode with avalanche in series with a forward biased junction



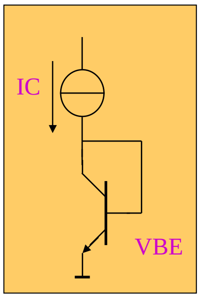
Requires 6..7V

Buried Zener diode



•No degradation due to surface effects
⇨ less 1/f - noise
⇨ less sensitive to stress

Forward biased junction



$$I_C = I_S \exp(qV_{BE}/kT)$$

$$I_S = \frac{qAn_i^2\overline{D}}{N_B}$$

$$n_i^2 \rightarrow CT^3\exp[-E_G(T)/kT] \qquad \overline{D} \rightarrow \frac{kT}{q}\cdot\mu \qquad \mu \rightarrow BT^n$$

(η = XTI = 4-n)

$$I_{C0}(T/T_0)^\theta = C'(T/T_0)^\eta \ \exp\left[\frac{qV_{BE}-E_G(T)}{kT}\right]$$

$$V_{BE}(T) = \frac{E_G(T)}{q} - \left[\frac{E_G(T_0)}{q} - V_{BE}(T_0)\right]\frac{T}{T_0} + (\theta-\eta)\cdot\frac{kT}{q}\ln\left(\frac{T}{T_0}\right)$$

First-order approximation around T_0

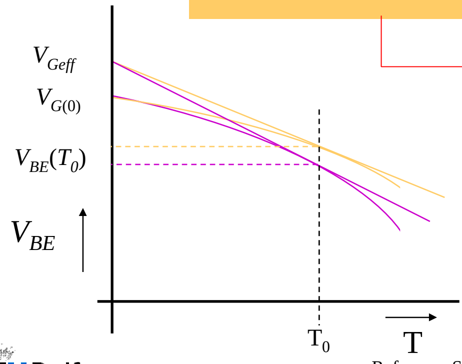
$$V_{BE}(T) = \frac{E_G(T)}{q} - \left[\frac{E_G(T_0)}{q} - V_{BE}(T_0)\right]\frac{T}{T_0} + (\theta-\eta)\cdot\frac{kT}{q}\ln\left(\frac{T}{T_0}\right)$$

Taylor

$$V_{BE}(T)_1 = \frac{E_G(T)}{q} - \left[\frac{E_G(T_0)}{q} - V_{BE}(T_0)\right]\frac{T}{T_0} + (\eta-\theta)\cdot\frac{kT}{q}\frac{T_0-T}{T_0}$$

$$V_{BE}(T)_1 = V_{Geff} - \left[V_{Geff} - V_{BE}(T_0)\right]\frac{T}{T_0}$$

$$V_{Geff} = V_{G(0)} + (\eta-\theta)kT_0/q$$



- V_{BE} has negative t.c.
- V_{BE} ↓ |t.c.| ↑
- V_{Geff} independent of V_{BE}

Example

Assume a transistor is biased at a constant current of 1 μA.
For the transistor the following parameters apply: I_S=18 aA ,
XTI = 3 and $V_{G(0)}$ = 1.2V.

What is the first-order temperature coefficient at T_0 = 300K?

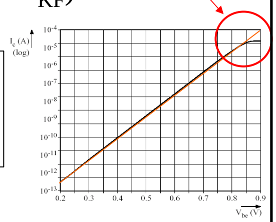
V_{BE}(300K) = 640 mV
V_{Geff} = 1.2V + (3-0) · 25.8mV = 1.28V ($V_{Geff} = V_{G(0)} + (\eta - \theta)kT/q$)

t.c. = -2.1 mV/K

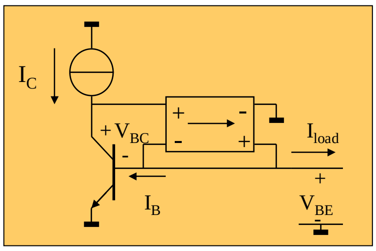
($t.c. = -[V_{Geff} - V_{BE}(T_0)]/T_0$)

Biasing a BE-junction

- Bias current far below high-level injection (I_C<<I_{KF})
- Bulk resistances (made) negligible

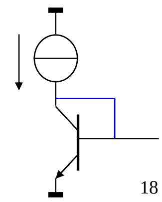


$$I_C = I_S\left[\exp(V_{BE}/V_T) - 1\right]\left[1 - \frac{V_{BC}}{V_{AF}} - \frac{V_{BE}}{V_{AR}}\right]$$

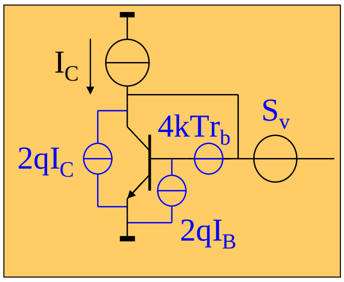


- Nullor makes V_{BC}=0 ⇨ ~~VAF~~
- Nullor supplies I_B and I_{load}
  - ⇨ Low beta no problem
  - ⇨ V_{BE} is buffered
- VAR remains

Simplest implementation nullor ?



Noise of a BE junction



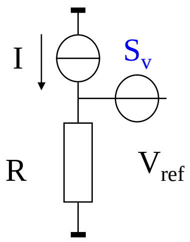
- S_v noise-power density spectrum [V^2/Hz]

$$S_v = 4kT\left(r_b + \frac{1}{2g_m}\right)$$

- Collector shot noise and thermal noise of the base resistance dominate

- Assume r_b=150, I_C=100 μA and V_{BE}=600 mV → $\frac{1}{2g_m} = 130$ → $S_v = 4kT \cdot 280\Omega$

Comparison



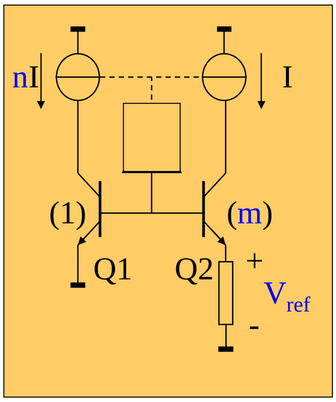
$$R = \frac{600\text{ mV}}{100\ \mu\text{A}} = 6000\ \Omega$$

⇒ $S_v = 4kT\ 6000\ \Omega$

- Noise of a BE-junction is 20 times lower
- Output impedance is 25 times lower

Proportional To Absolute Temperature

- Difference of two junction voltages



$V_{ref} = V_{BE1} - V_{BE2}$

$= \frac{kT}{q} \ln(n\,m)$

Example:

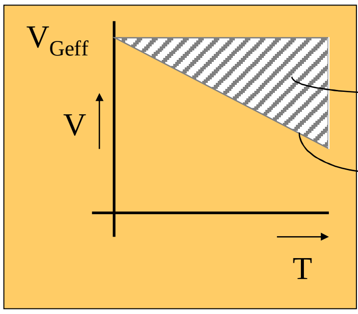
$n = 10 \Rightarrow V_{ref} = \frac{kT}{q} \ln(10)$
$m = 1$

$= T \cdot 198\ \mu V/K$

$= 59.58\ mV@300K$

Use as temperature sensor

Combination of a V_{BE} and V_{PTAT}



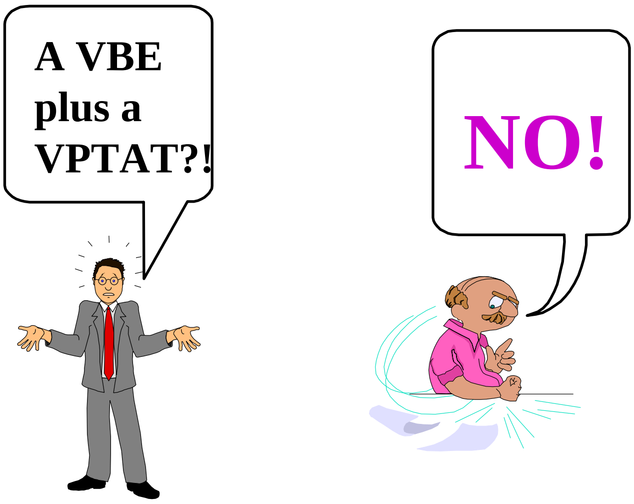
V_{PTAT}
$+ \longrightarrow V_{Geff}$
V_{BE}

V_{BE} has a *negative* t.c.
V_{PTAT} has a *positive* t.c. +
Sum can have *zero* t.c.

⇓

The Bandgap Reference

Question : What is a bandgap reference ?



The bandgap reference

Relates output voltage to the bandgap voltage at 0K

$$V_{ref} = x \cdot \frac{E_G(0)}{q}$$

- Describe base-emitter voltage as:

$$V_{BE}(T) = V_{Geff} - \left[V_{Geff} - V_{BE}(T_0)\right]\frac{T}{T_0}$$

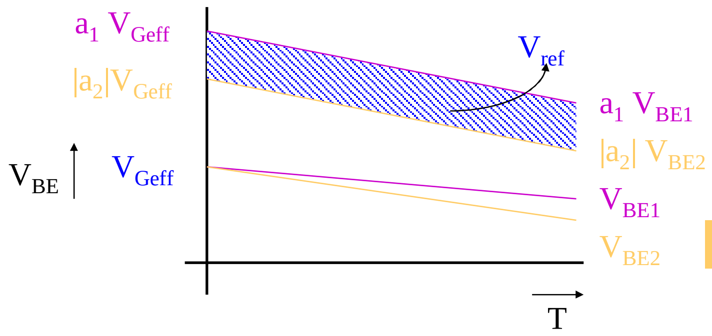
Use linear combination of base-emitter voltages

Linear combination of V_{BE}s

$$a_1 V_{BE1} = a_1 V_{Geff} - a_1\left[V_{Geff} - V_{BE1}(T_0)\right]T/T_0$$

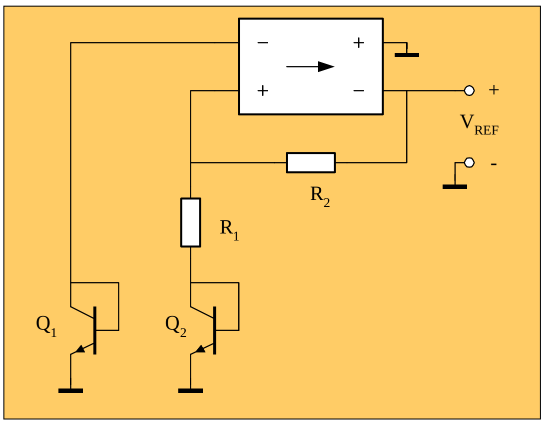
$$a_2 V_{BE2} = a_2 V_{Geff} - a_2\left[V_{Geff} - V_{BE2}(T_0)\right]T/T_0 \quad +$$

$$= (a_1 + a_2)V_{Geff} + 0 \cdot T/T_0$$



NB: $a_2 < 0$

Bandgap Reference Example



$$V_{REF} = a_1 V_{BE1} + a_2 V_{BE2}$$

$$a_1 = 1 + \frac{R_2}{R_1}, \quad a_2 = -\frac{R_2}{R_1} \quad \Big\} \quad a_1 + a_2 = 1$$

$$V_{REF} = (a_1 + a_2)V_{Geff} = V_{Geff}$$

But also: $V_{R1} = V_{BE2} - V_{BE1} = V_{PTAT}$ ➡ $V_{REF} = V_{BE2} + A_U V_{PTAT}$

Accuracy of V_{ref}

a_1, a_2 : rely on matching

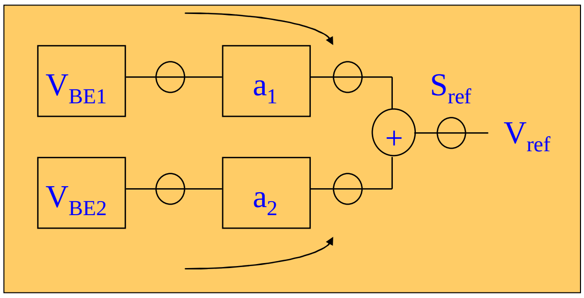
V_{BE1}, V_{BE2} : several parameters are important

- I_{S1}, I_{S2} : matching and absolute accuracy
- I_{C1}, I_{C2} : use accurate bias techniques
  θ_1, θ_2
- E_G, η, V_{AR} : given by process, good characterization required

Key parameters of device : E_G, V_{AR}, I_S, η

For accurate design these should be well-known !

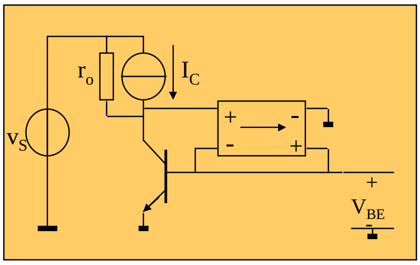
Noise performance of Bandgap Reference



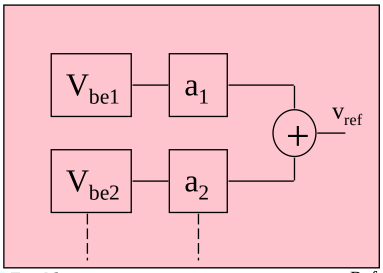
- Noise of the bandgap reference is a weighted sum of the noise contributions of the V_{BE}s

S_{ref} is inversely proportional to the current consumption

Power-Supply Rejection Ratio



r_o due to Early effect



$$PSRR = 20 \cdot {}^{10}\log\left(\frac{V_T}{V_{AF}}\frac{V_{ref}}{V_S}\right)$$

unit: dB

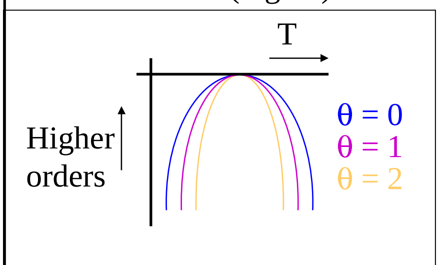
Design example 1V, 100 μA, BGR

(Second-order compensated)

- Describe V_{BE}s with a second-order polynomial

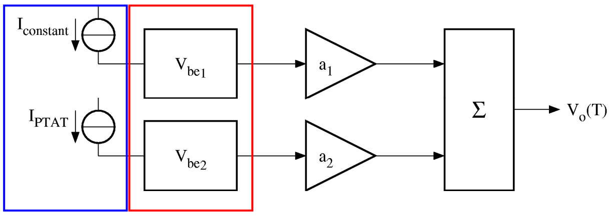
$$V_{BE}(T) = V_{BE}(T_0) + x_1\,(T-T_0) + x_2(T-T_0)^2$$

- Second (higher) order terms can only be changed by θ



- Again use linear combination
- Two V_{BE}s for second-order compensation
- Different V_{BE}s (1 order)
- Different θ's (1 order)

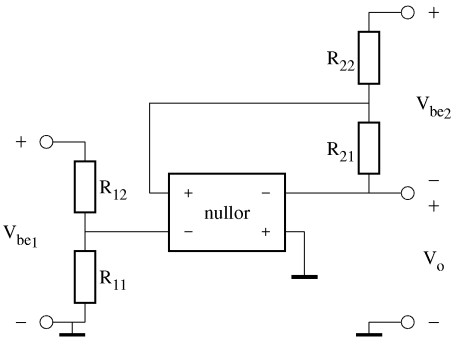
Block Schematic



Different V_{BE}s (1 order)
Different θ's (1 order)

Vref = 200 mV

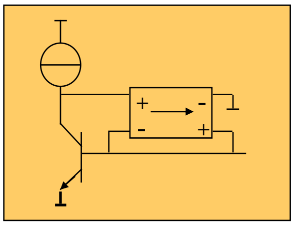
First implementation step

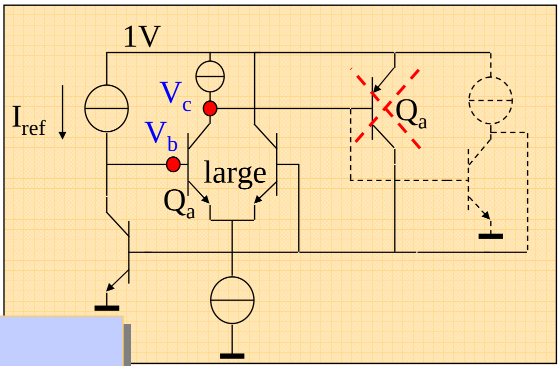


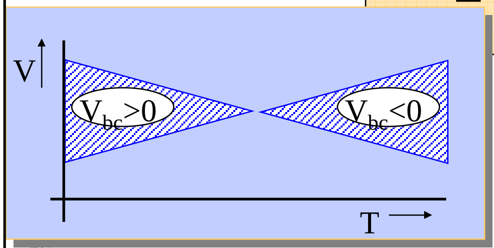
Both V_{BE}s have negative t.c. ⇨ scale factors must have opposite sign

- a_1 positive
- a_2 negative

Implementation of VBE generators



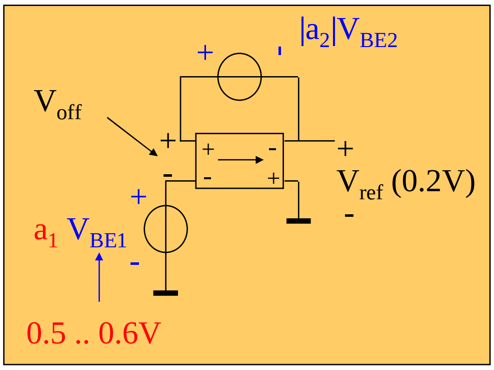


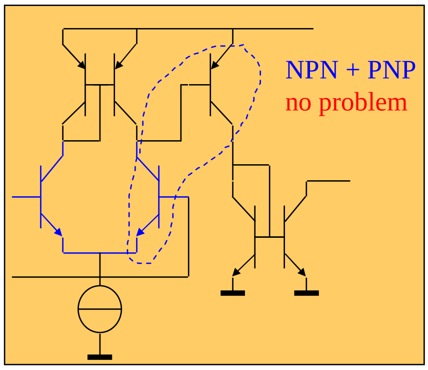


At low temperatures Q_a saturates ⇨ I_B of Q_a degrades I_{ref}

⇨ Use cascade of NPNs

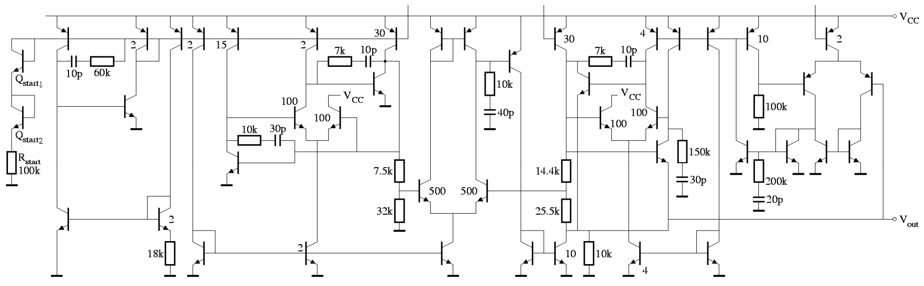
Implementation of the adder





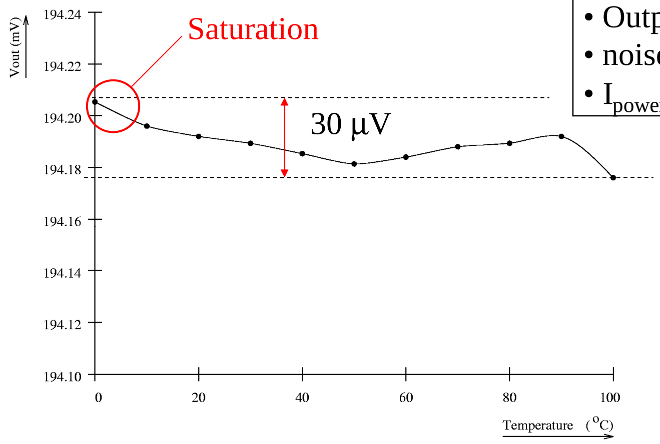
- V_{off} in series with V_{ref} ⇨ Use differential input stage
- Low voltage level at input ⇨ Use sized-emitter transistors

Total Circuit



Where are the different blocks?

Measurement results



- V_{out} = 194 mV
- Mean error = 1.5 ppm/K
- Output imp. = 43 Ω
- noise < 80nV/$\sqrt{\text{Hz}}$
- I_{power} = 100 μA