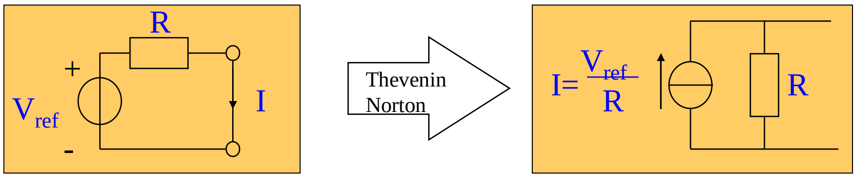
The current source

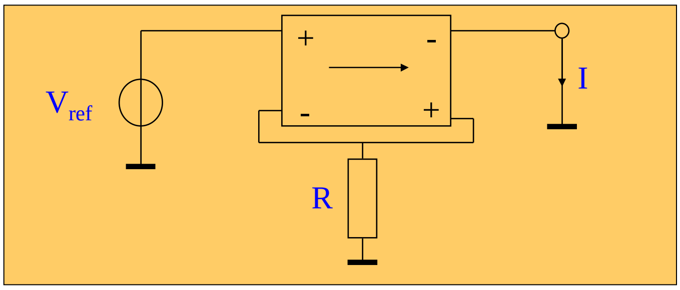


•Minimum noise equals: $\frac{4kT}{R}$

DC current through resistor gives an increase of 1/f noise (granular structure)
•Accuracy of source also determined by the accuracy of R
•Output impedance mostly too low

Use active V → I converter

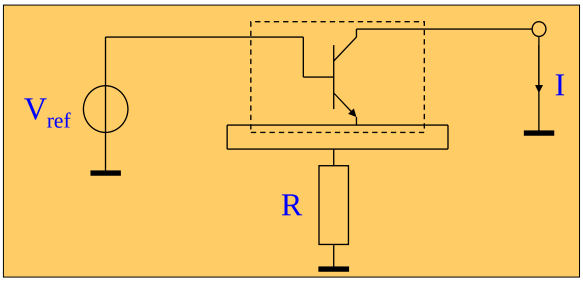
The Active Current Source



• Output impedance is ....

• What about the noise?

Nullor implemented by one CE stage

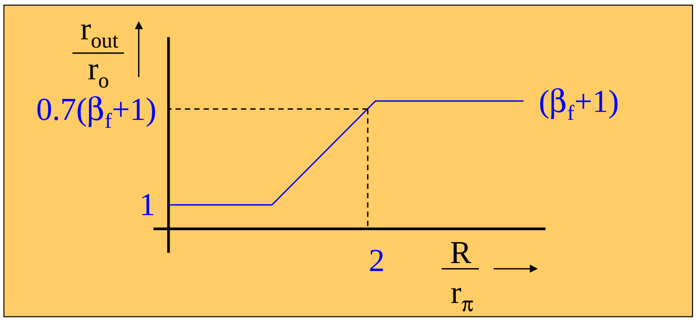


- $I = -(V_{ref} - V_{BE})/R$
- Temperature behavior V_{BE} found in I (how to solve?)
- Output impedance:

$$r_{out} = r_0 + R + R \cdot \frac{\beta_f r_o - R}{r_b + r_\pi + R}$$

- If $R >> r_\pi$ and $R >> r_b$ ⇨ $r_{out} = (\beta_f + 1) r_0$

Plot of the output impedance vs R

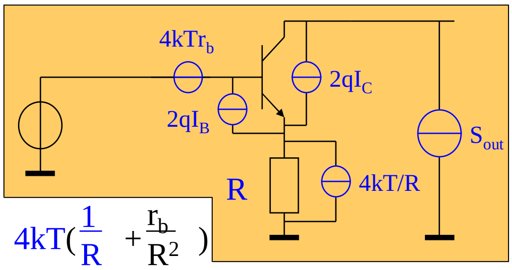


$$V_R = I \cdot R = I \cdot 2 r_\pi = 2\beta \frac{kT}{q} \qquad \beta_f = 100, \ \frac{kT}{q} = 25 \text{ mV}$$

⇨ V_R=5V

- Lower β_f reduces V_R but also r_{out}
- Better nullor approximation helps (r_o must be increased)

Noise behavior of active current source



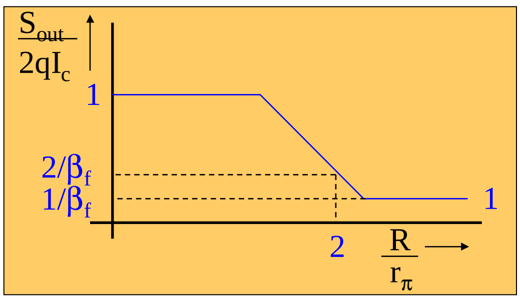
$$S_{out} = \underbrace{\frac{2qI_C}{\left(1+\frac{\beta_f R}{r_\pi}\right)^2}}_{\text{I}} + \underbrace{\frac{2qI_B}{\left(1+\frac{r_\pi}{\beta_f R}\right)^2}}_{\text{II}} + \underbrace{\frac{4kT\left(\frac{1}{R}+\frac{r_b}{R^2}\right)}{\left(1+\frac{r_\pi}{\beta_f R}\right)^2}}_{\text{III}}$$

$R \rightarrow$ infinite

I $\longrightarrow$ 0
II $\longrightarrow$ $2qI_B$
III $\longrightarrow$ 0 (4kT/R)

Only base shot noise remains

Plot of noise vs R



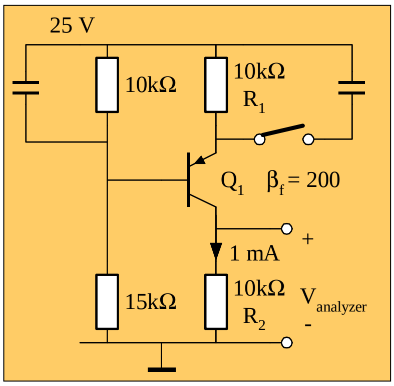
If contribution of $2qI_C$ plus $4kT/R$ equals $2qI_B$, then

$R = \frac{2\beta_f}{g_m}$ ⇨ $V_R = 5$ V and $S_{out} = 4qI_B$ $= 2 \cdot 2qI_B$

Lowering β_f for reducing V_R does not help also, as:

$S_{out} = 8kT\ I/V_R$ ⇨ The lower V_R the higher the noise

Current source demo



Switch open:

$$S_{out} \approx 4kT\frac{R_2^2}{R_1} + 4kTR_2 + 2qI_BR_2^2$$

$$v_{n,out} \approx 22\ \text{nV}/\sqrt{\text{Hz}} = -33\ dB\mu V$$

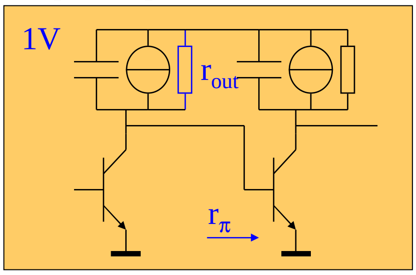
Switch closed:

$$S_{out} \approx 0 + 4kTR_2 + 2qI_CR_2^2$$

$$v_{n,out} \approx \quad \text{nV}/\sqrt{\text{Hz}} = \quad dB\mu V$$

Current sources in 1V circuits

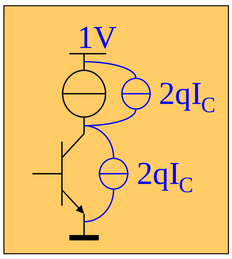
Output impedance:



V_R relatively small ⇨ $r_{out} = \frac{VAF}{I_C}$

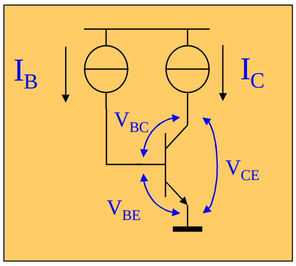
- Reduction of the DC loop gain ⇨ accuracy
- Does not need to cost bandwidth as pole also shifts

Noise:



- Noise of the active part approximately doubles

Saturating transistors



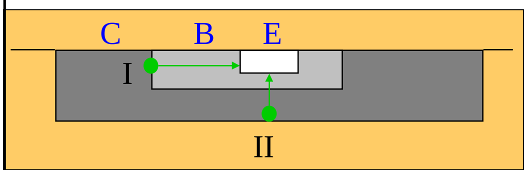
- Transistor saturates if $I_C/I_B < \beta_F$
- Collector-emitter voltage is the difference of V_{BE} and V_{BC}

$$V_{CE} = \frac{kT}{q} \ln \left[\frac{1 + \frac{1}{\beta_r}(1 + I_C / I_B)}{1 - \frac{I_C}{I_B \beta_f}} \right]$$

PTAT

- For $I_C/I_B = \beta_f$ denominator equals zero ⇨ V_{CE} not determined
- V_{CE} reduces for larger β_r (saturation voltage reduces)
- V_{CE} reduces for larger I_C/I_B (deeper saturation)

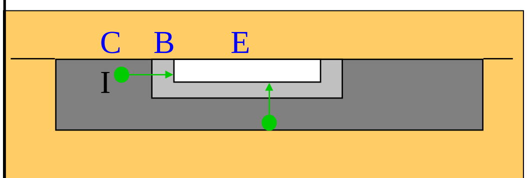
Influence of layout on $V_{saturation}$ (I)



- electron at I has a larger chance on recombination than electron at II

  ⇨ Bad for β_r

Take care of a large β_r



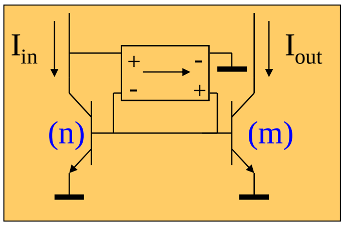
- Most of the electrons have a short way to go

  ⇨ Less recombination

  ⇨ β_r increases

General: Collector and emitter overlap should be as large as possible

The current mirror



Mirror used for:
- biasing purposes
- current-gain stages
- buffering (cascode)

Transfer : $\frac{I_{in}}{I_{out}} = \frac{m}{n}$

Again nullor can be implemented by wire ⇨ standard current mirror

Signal-to-noise ratio and dynamic range of a current mirror

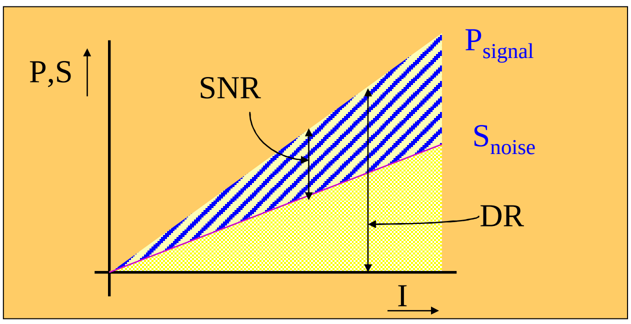
- SNR is the ratio of smallest and largest signal that can be processed at the same time
- DR is ratio of smallest and largest signal that can be processed, not necessarily at the same time
- Noise power proportional to collector current ($2qI_C$)
- Signal power proportional to the square of IC (I_C^2)

For I_C=1 nA and B=10 kHz

⇩

SNR = 52dB

DR $\rightarrow \infty$

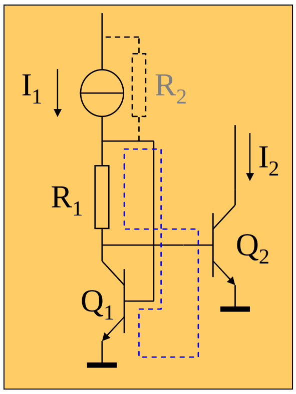


Peaking current source

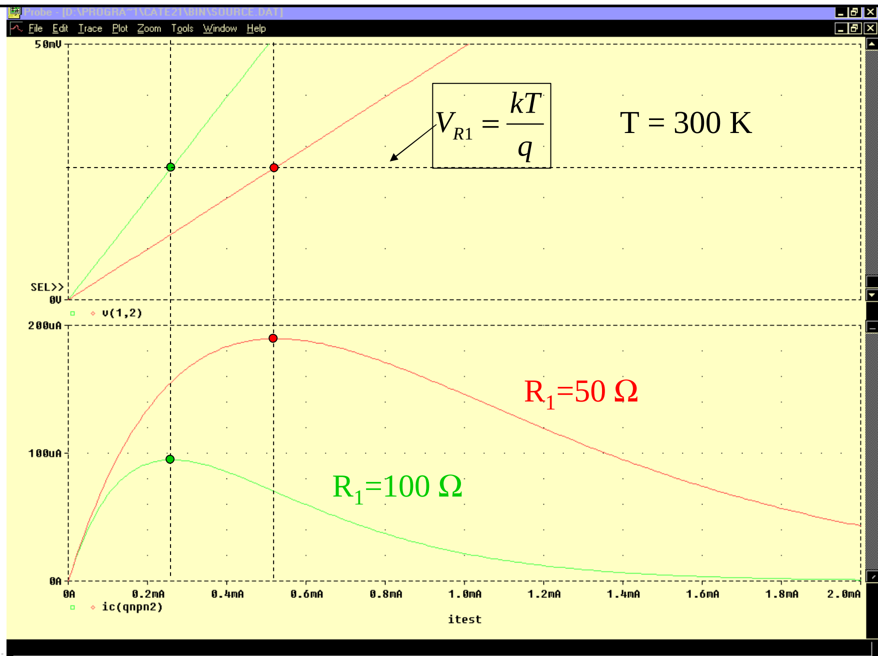
Derived from current mirror

$$\ln\left(\frac{I_2}{I_{S2}}\right) = \ln\left(\frac{I_1}{I_{S1}}\right) - \frac{I_1 R_1}{kT/q}$$

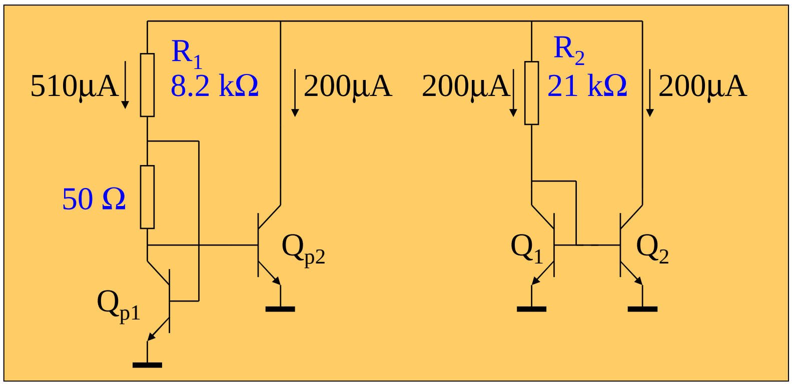
$$\frac{dI_{C2}}{dI_{C1}} = 0 \quad \text{for} \quad R \cdot I_{C1} = \frac{kT}{q}$$



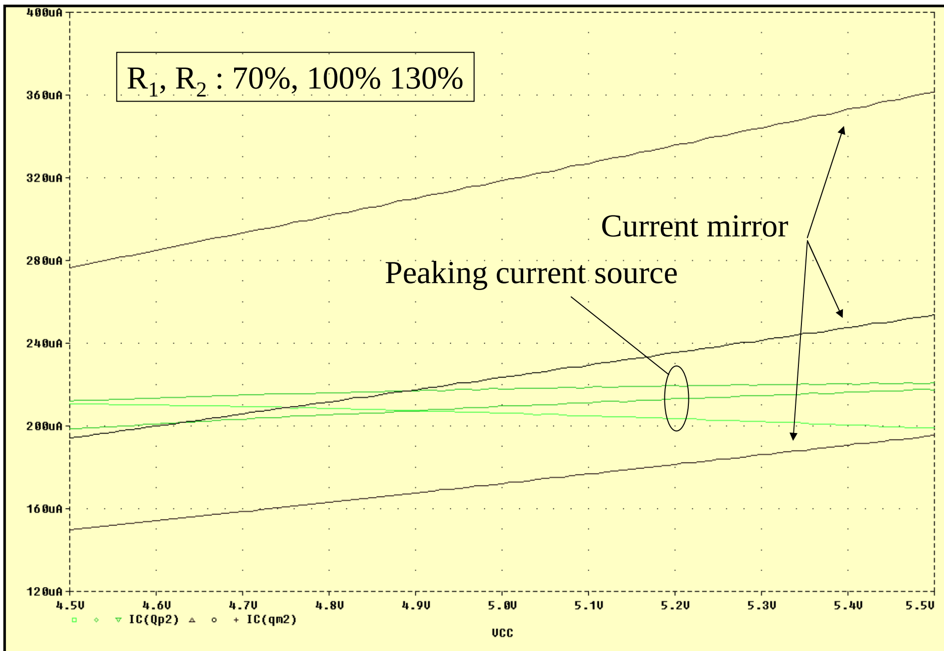
- Source I_1 can be implemented by a resistor
- R_1 relatively low ohmic and accurate ⇒ a broad resistor
- R_2 relatively high ohmic and not very accurate ⇒ a small resistor
- What about PSSR ?



Peaking current source vs Current mirror



- 50 must be accurate
- 8k2 does not need to be accurate
- 21k must be accurate



Conclusion/Summary

- Several configurations of voltage and current sources discussed
- Current level is the performance determining quality,
  not a 1V constraint
- Circuit design is hampered by 1V criterion ⇨ other topologies