Analog Integrated Circuit Design
ET4252
DC sources and references
Translinear Circuits

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Chapter 1

Integrable DC sources and references

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1.1 Introduction

Electronic systems can be seen as an implementation of mathematical functions. A system may contain all kinds of blocks, for example, integrators, multipliers and constants.

This chapter discusses system blocks, which are integrable, for generating a:

- voltage constant,
- current constant.

These constants are widely used in electronic design. For example, a current constant is used to determine the collector bias current of a transistor. In this case, the absolute accuracy is not that important. Mostly, a relatively large variation as a function of temperature, time or other parameter is allowed.

Another example is a voltage constant used in a voltmeter. An unknown voltage is compared indirectly with the voltage constant to determine its value. The absolute value of the constant is of prime importance. The accuracy of the measurement cannot be better than the accuracy of the voltage constant.

These two examples show two specific types of application of constants:

- The constant used as a source, i.e. a voltage or current *source*. The absolute value is not particularly important. The value may change within a certain region.
- The constant used as a reference, i.e. a voltage or current *reference*. The absolute value of the constant is of prime importance.

The application determines when the implementation of a constant is called a reference or a source. Both names are used in this chapter. When general theory of constants is treated, the most general name, the source, is used. When more specific implementations are treated, the most commonly used name is employed.

The next section of this chapter starts with the description of the ideal voltage and current constants. Using this description, implementations of voltage constants are given, from very simple (resistive divider) to more complicated circuits (bandgap reference). The non-ideal effects, like the finite current-gain factor, Early effect, etc. are discussed. The current constant is treated after the voltage constant, because the current source is often derived from a voltage source via a (trans)conductance. Implementations and non-ideal effects are discussed.

1.2 The ideal voltage and current constants

Voltage and current constants are generated, respectively, by a voltage source and a current source. The output signal of ideal sources is independent of the load, temperature and all other kinds of environmental disturbances. Further, the output signal is not contaminated by noise.

1.2.1 The ideal voltage source

In figure 1.1, the output signal versus the load current of the ideal voltage source is depicted in the V-I plane. As can be seen, the output voltage $V_{\rm ref}$ is independent of the load current $I_{\rm load}$. As

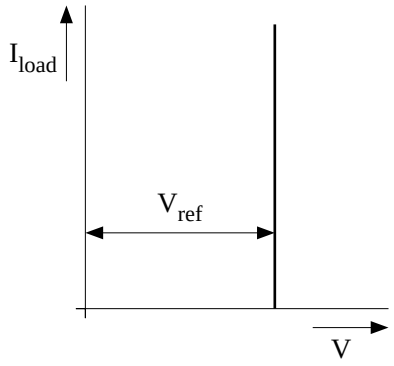

Figure 1.1: The output voltage $V_{\rm ref}$ versus the load current $I_{\rm load}$

the output impedance of a voltage source is defined as the ratio of output-voltage variation and load-current variation, the output impedance $r_{\rm out}$ of the ideal voltage source equals zero:

$$r_{\rm out} = \frac{dV_{\rm ref}}{dI_{\rm load}} = 0\Omega. \tag{1.1}$$

The ideal output voltage is not influenced by a change in the ambient temperature. Its temperature coefficient is zero:

$$\alpha_T = \frac{dV_{\rm ref}}{dT} = 0\text{V/K}. \tag{1.2}$$

Finally, all the power supplied has to be concentrated at dc. The signal-to-noise ratio of the output voltage is infinite. Sometimes it is more convenient to talk about the absolute value of the output noise. For the ideal case the power-density spectrum S_v of the noise voltage at the output equals:

$$S_v = 0\text{V}^2/\text{Hz}. \tag{1.3}$$

1.2.2 The ideal current source

In figure 1.2, the output current $I_{\rm ref}$ of the ideal current source is depicted in the I-V plane as a function of the load voltage. The output current is independent of this voltage. Therefore the

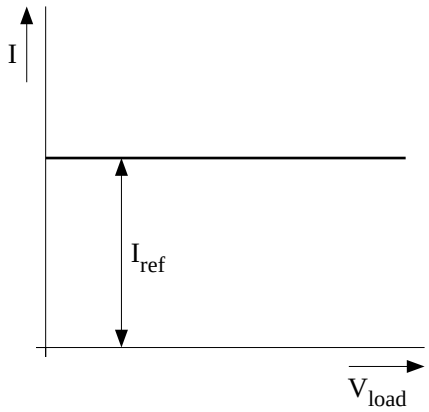

Figure 1.2: The output current $I_{\rm ref}$ as a function of the load voltage $V_{\rm load}$

output impedance $r_{\rm out}$ of the ideal current source is infinite:

$$r_{\rm out} = \frac{dV_{\rm load}}{dI_{\rm out}} = \infty\Omega. \tag{1.4}$$

Just like the ideal voltage source, the temperature coefficient of the output current and the power-density spectrum S_i of the noise current at the output are zero:

$$\alpha_T = 0\text{A/K}, \tag{1.5}$$
$$S_i = 0\text{A}^2/\text{Hz}. \tag{1.6}$$

Integrable implementations of the ideal voltage and current source are discussed in the following sections.

1.3 Implementations of the voltage source

As discussed in the previous section, an ideal voltage source has specific characteristics. Summarized:

- output impedance of 0Ω,
- temperature independent,
- noise free.

When practical implementations are made, the voltage source itself needs a power supply. The output voltage of the source must be independent of this power supply. Power-supply variations are not allowed to penetrate to the output of the voltage source. Thus the power supply

only supplies the dc bias current. The figure of merit for this quality aspect is the Power Supply Rejection Ratio or PSRR for short. The PSRR is defined as:

$$PSRR \triangleq \frac{dV_{\rm power}}{dV_{\rm ref}} \tag{1.7}$$

with $V_{\rm power}$ the supply voltage. For a voltage source approximating the ideal source it holds that

- The Power Supply Rejection Ratio has to be infinite.

Depending on the application, one or more of the four mentioned constraints are of prime importance.

The output voltage of a realistic voltage source is depicted in figure 1.3. The source behaves

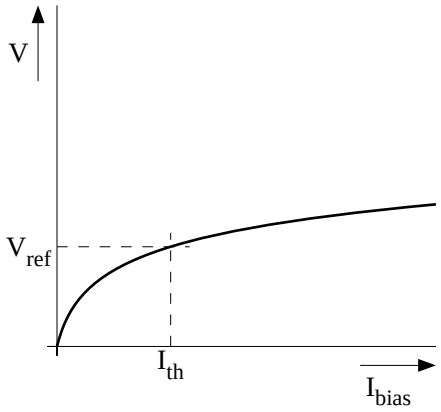

Figure 1.3: The output voltage $V_{\rm ref}$ versus the bias current $I_{\rm bias}$ of a realistic voltage source

as a voltage source when the bias current is above the threshold current $I_{\rm th}$. Thus practical implementations pose additional constraints.

Several implementations of voltage sources are discussed in the next section.

1.3.1 The resistive divider

The schematic of the voltage source implemented by a resistive divider is depicted in figure 1.4. The output voltage $V_{\rm ref}$ is a fraction of the power-supply voltage $V_{\rm cc}$:

$$V_{\rm ref} = \frac{R_2}{R_1 + R_2} V_{\rm CC}. \tag{1.8}$$

The accuracy of this source is determined by the accuracy of the power-supply voltage and the matching of the two resistors.

The output impedance, $r_{\rm out}$, of this source equals the parallel connection of the two resistors:

$$r_{\rm out} = \frac{R_1 R_2}{R_1 + R_2}. \tag{1.9}$$

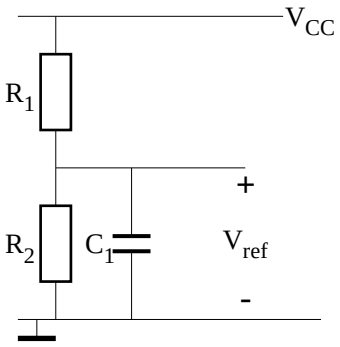

Figure 1.4: A voltage source implemented by a resistive divider

To obtain a low output impedance with this source, low resistances have to be used. This results in a high current consumption. This relation becomes more clear when the total supply current I_{bias} is expressed as a function of the output impedance. The following relation is found:

$$I_{\text{bias}} = \frac{V_{\text{CC}}}{R_1 + R_2} = \frac{1}{r_{\text{out}}} \left(1 - \frac{V_{\text{ref}}}{V_{\text{CC}}}\right) V_{\text{ref}}. \tag{1.10}$$

Thus for a given output voltage and power-supply voltage, the bias current is inversely proportional to the output impedance.

When the output impedance is important for higher frequencies only, the impedance can be made low with a capacitor. This is illustrated in figure 1.4 with capacitor C_1. Now C_1 determines the output impedance for relatively high frequencies. This capacitor may be too large for integration. In this case an additional pin is required to be able to keep the capacitor outside the chip.

The output noise is determined by the thermal noise of the parallel connection of the two resistors. The power-density spectrum, S_v, of the noise voltage equals:

$$S_v = 4kT(R_1 \parallel R_2). \tag{1.11}$$

Again, for a low-noise behavior, low resistances and thus a high current consumption are required. With capacitor C_1 this power-density spectrum can be reduced for the relatively high frequencies.

The PSRR is determined by the resistors and is given by:

$$PSRR = 1 + \frac{R_1}{R_2}. \tag{1.12}$$

To obtain a high power supply rejection ratio, the ratio R_1 and R_2 has to be large. However, for a given output voltage, this ratio is fixed. A solution is to decouple R_2 by using a sufficiently large capacitor. This can also be capacitor C_1 in figure 1.4.

The temperature behavior of this source is determined by the temperature stability of the resistor ratio and the temperature dependency of the supply voltage.

1.3.2 The non-linear divider

To improve the performance of the source, a non-linear impedance can be used for R_2. The principle is depicted in figure 1.5. The non-linear function is the I-V characteristic of the non-

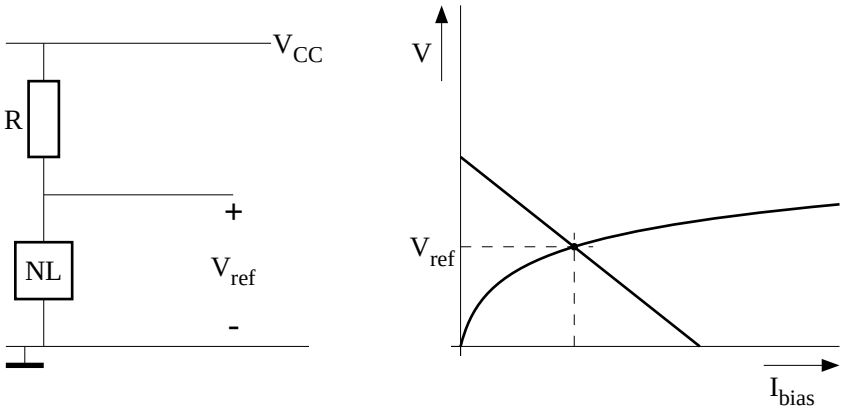

Figure 1.5: A voltage source using a non-linear device

linear device (NL), the affine load line is of the resistor (R). The output voltage is given by the intersection point of the two functions.

With this non-linear device, the large-signal behavior (the generation of an output voltage) and the small-signal behavior (a low output impedance) are different. The output impedance of the source is approximately the small-signal impedance of the non-linear device. This can be much lower than for the resistive divider.

The noise behavior of this source with respect to the linear divider with the same current consumption generally improves.

As seen in the previous section, the PSRR [see equation (1.12)] increases when R_2 decreases. For this source, R_2 is replaced by the small-signal impedance of the non-linear device. The PSRR can be considerably higher.

Various devices can be used for the non-linear part of the divider. Four possibilities are depicted in figure 1.6. The devices are:

a. diode-connected bipolar transistors,

b. diodes at reverse Breakdown,

c. diode-connected normally-off FETs,

d. bipolar transistors used at punch-through.

A diode-connected bipolar transistor

In figure 1.6a, the diode-connected bipolar transistor is used as the non-linear device. The output voltage equals the base-emitter voltage of the transistor and is in the range of 0.5V to 0.8V, depending on the collector-current density. For higher values more junctions in series have to

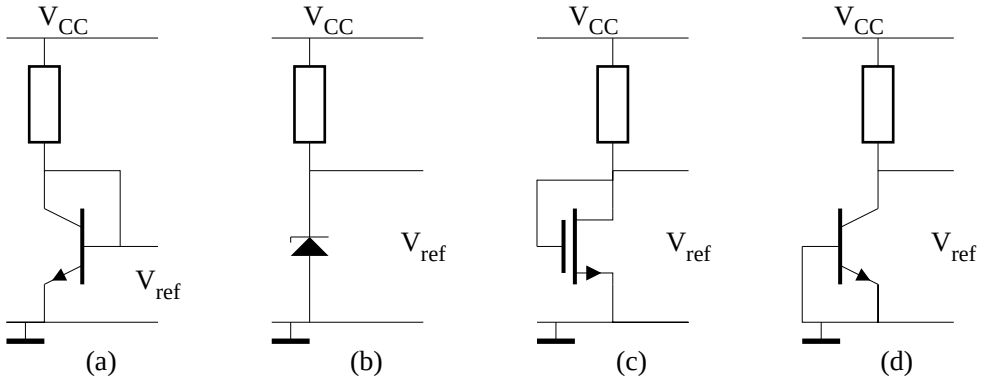

Figure 1.6: Four non-linear devices

be used. Lower voltages can be obtained with a Schottky junction, for instance, with a junction voltage of approximately 0.2V. The output impedance $r_{\rm out}$ is approximately:

$$r_{\rm out} \approx \frac{kT}{qI_{\rm bias}} \tag{1.13}$$

with $I_{\rm bias}$ the collector bias current of the transistor. The higher the current the lower the output impedance. The temperature dependency of this source is the temperature dependency of the junction voltage and is in the order of a few mV/K.

The noise of the source equals the noise generated by the transistor, when it is assumed that the noise of the resistor is negligible. The power-density spectrum S_v of the noise voltage equals:

$$S_v = 4kT(r_b + \frac{1}{2g_m}) \tag{1.14}$$

with r_b the base resistance and g_m the transconductance of the transistor. An improvement of the noise performance is obtained when higher bias currents (the g_m increases) or larger transistors (the base resistance reduces) are used.

A diode at reverse breakdown

A voltage source can also be made of a reverse-biased diode at breakdown. Zener diodes are optimized for use in this mode. The V-I characteristic of a Zener diode is depicted in figure 1.7. The forward behavior is comparable to that of a normal pn junction. But when the Zener diode is biased in reverse mode and the voltage is increased slowly, at a specific voltage the currents suddenly starts to increase very rapidly. This specific voltage is called the reverse-breakdown voltage, $V_{\rm br}$. Beyond this voltage the Zener diode behaves like a voltage source (c.f. figure 1.1). For normal diodes this reverse breakdown can be destructive.

The reverse breakdown is due to two distinct mechanisms, *avalanche multiplication*, which causes an avalanche breakdown and the *Zener effect*, which causes a Zener breakdown. Although diodes are optimized such that one of the two mechanisms is dominant, both types of diodes are called Zener diodes.

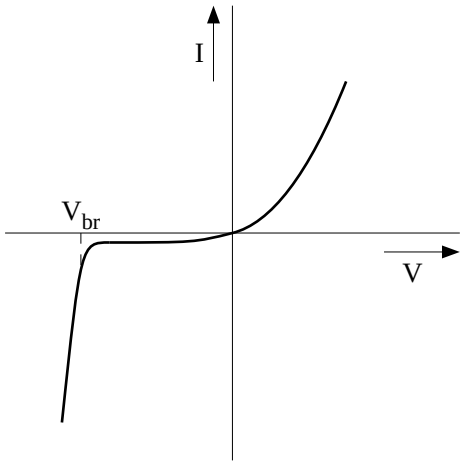

Figure 1.7: The V-I characteristic of a Zener diode

Avalanche breakdown
Avalanche breakdown occurs in the presence of high electric fields in relatively wide regions. The carriers are accelerated sufficiently to become able to ionize atoms. The newly created carriers are accelerated and the also ionize atoms. An avalanche of carriers arises and the current increases very rapidly. This effect is more apparent in lightly-doped materials and is proportional to the electric field strength. In lightly-doped materials, the carriers are able to travel a relatively large distance without collisions. The chance that they obtain enough energy for ionizing other atoms increases. For higher electric field strengths, the free path length, necessary for ionizing other atoms, decreases, more ionizations per unit length occur and the current increases. Avalanche breakdown is the dominant breakdown effect in junctions with a breakdown voltage higher than 6V.

When there is avalanche breakdown, the junction is overwhelmed by high-energetic carriers and the junction may be damaged. This results in an increase of 1/f and the non-ideal currents. The increase of the non-ideal currents is the cause of the deterioration in the low-current behavior. Thus, in normal junctions, avalanche breakdown has to be avoided.

Zener breakdown
In slightly reverse-biased junctions, the energy bands of a junction are as depicted in figure 1.8. Between the valence band (E_V) and conduction band (E_C) the energy gap E_g exists. A carrier has to gain an amount of energy equal to or more than this E_g to be able to reach the other band. When the diode is reverse biased and the reverse voltage is increased, the bottom of the conduction band and the top of the valence band of, respectively, the n and p material reaches the same energy level. When the distance W (see figure 1.9) between the bands is smaller than a critical value, the carriers can tunnel directly from the valence band in the p material to the conduction band in the n material, without the help of other carriers. A further increase in the reverse voltage leads to an overlap of the two bands (see figure 1.9) and the potential-barrier width, W, becomes smaller and smaller. Due to this reduction of barrier width, the tunneling probability increases

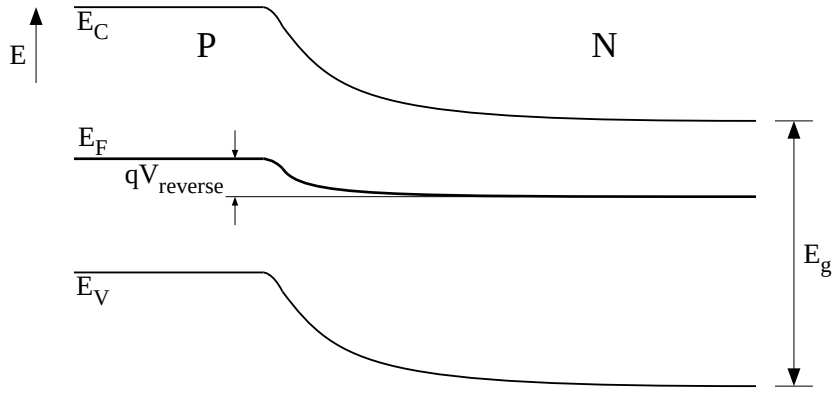

Figure 1.8: The band diagram of a slightly reverse-biased junction

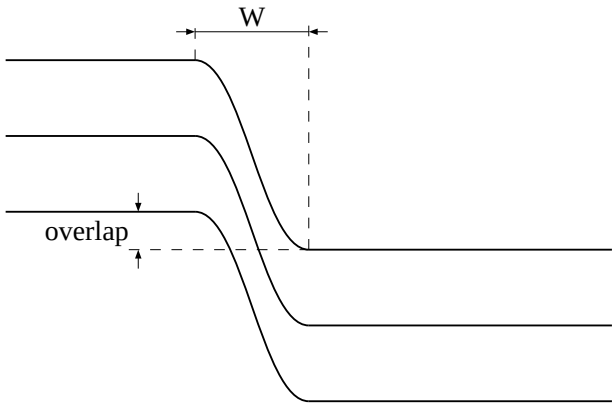

Figure 1.9: The band diagram when the conduction band and the valence band have an overlap

and the current increases even further. For higher-doped junctions, the depletion region is less wide and results in a lower Zener breakdown voltage. Since tunneling can start only when the bands are at equal levels, Zener breakdown occurs more abruptly than avalanche breakdown. Pure Zener breakdown occurs in highly doped junctions with a reverse-breakdown voltage lower than 5V.

The temperature dependency of the diode at reverse breakdown
The avalanche effect depends on the free path length of the carriers. When the temperature rises, lattice vibrations increase and the carriers are hindered more. The mobility decreases and a higher electric field is needed to reach breakdown. Thus, the avalanche breakdown voltage has a positive temperature coefficient. However, the Zener breakdown is strongly dependent on the barrier width. For higher temperatures, the barrier width reduces and the Zener breakdown occurs at a lower voltage. Thus, the Zener breakdown voltage has a negative temperature coefficient.

When the temperature dependency of the breakdown voltage is too high, temperature compensation has to be carries out. This can be accomplished in two ways. Firstly, the diode can be constructed in such a way that the Zener effect and the avalanche multiplication are both equally important. As the temperature behavior of these two effects are opposite, a zero temperature coefficient can be obtained. A second method is to use a forward-biased junction. The temperature coefficient of a forward-biased junction is negative (this is discussed later) and about -2mV/K. The temperature coefficient of the avalanche breakdown voltage is about +2mV/K. With a series connection of a reverse-biased Zener diode at avalanche breakdown and a forward-biased junction, the temperature coefficient can be nullified. The voltage necessary is approximately 7V, being about 6V for the Zener diode and about 0.8V for the forward-biased diode.

Zener diodes on chip
The diodes at reverse breakdown frequently used on chip are in the range below 5V. Thus, the dominant effect is the Zener effect. In IC technology two types of Zener diodes can be realized. Firstly, a Zener diode made of a junction at the surface of the chip. Because this diode is mainly located at the surface, surface effects like 1/f noise have a greater influence on the behavior of the diode. Secondly, the Zener diode can be made in the bulk of the chip, see figure 1.10 The diode is formed by the buried N layer (BN) and the deep P diffusion (DP the isolation diffusion). Both are highly doped and Zener breakdown is likely to occur. In the design manual, it can be seen that the corresponding breakdown voltages are low. This diode is completely surrounded by bulk material and, consequently, the behavior is less hampered by surface defects.

Diode-connected normally-off FETs

When a normally-off FET is used as the non-linear component in the divider shown in figure 1.5, the output voltage is determined by the intersection point of the V_{GS} versus I_R and V_R versus I_R (see figure 1.11).

The output impedance, $r_{\rm out}$, of this source equals approximately:

$$r_{\rm out} = \frac{1}{g_m} \tag{1.15}$$

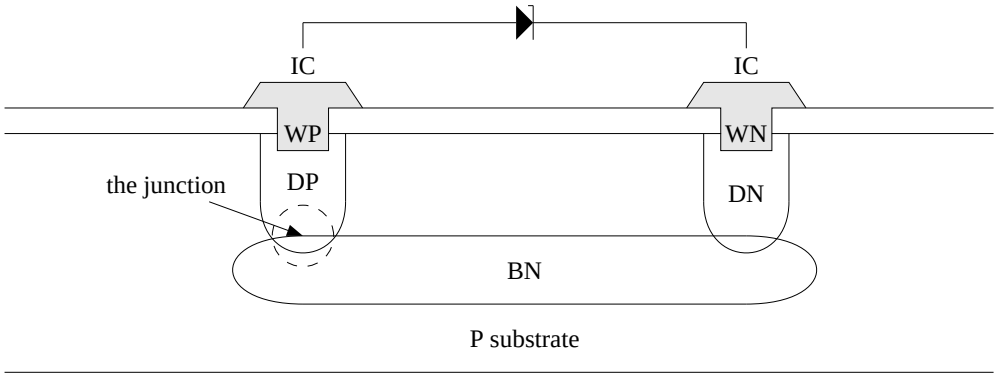

Figure 1.10: The realization of a Zener diode in the bulk of a chip

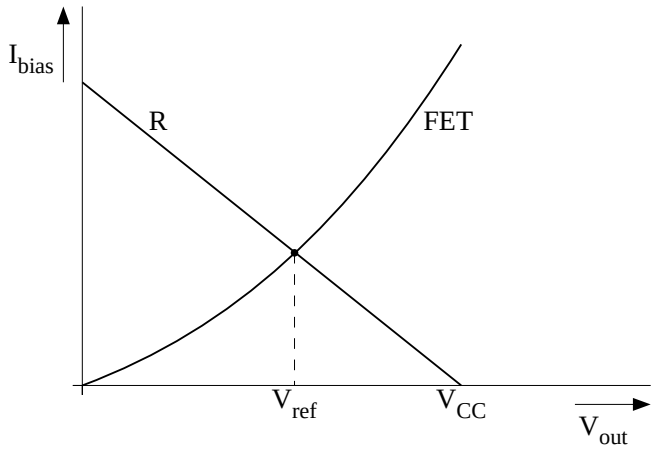

Figure 1.11: The output voltage of the voltage source using a FET

with g_m the transconductance of the FET. For lower output impedances, more current is required. The noise of this source is due to the thermal noise of the resistor and the drain noise of the FET. The PSRR equals:

$$PSRR = 1 + g_m R. \tag{1.16}$$

A transistor used at punch-through

When a junction is biased in reverse mode, the depletion layer becomes wider for higher reverse voltages. In a transistor, the base-collector junction is mostly reverse biased. The depletion layer of the base-collector junction reduces the effective base width (modeled by the forward Early voltage). When the reverse voltage is increased such that the depletion layer of the base-collector junction touches the depletion layer of the base-emitter junction, the effective base width is reduced to zero. An electric field now exists across this depleted area and transports every carrier that enters the region to the other side. Similar to the current through a collector-base depletion layer, the field cannot influence the number of carriers transported. The current is determined by the supply of carriers at the depletion layer boundaries. Since the emitter is highly doped, the current can become very large and an external current-limiting resistor has to be connected in series with the collector lead (see figure 1.6). For an increasing current, the voltage across the resistor increases, consequently, the voltage across the transistor decreases. At the biasing point, the voltage is such that the base-emitter and base-collector depletion regions just touch each other.

The output voltage of this circuit is indirectly determined by the number of available carriers. A small increase in the reverse base-collector voltage results in a very large increase in the output current. Thus, the output impedance of this source is very low.

1.3.3 Diode-connected transistors in forward mode

In this section, a base-emitter junction is used as an element with a very well-known I-V relation and temperature behavior. The voltage reference obtained can be very accurate with respect to output voltage and temperature behavior. The relation between the current and the voltage of a diode-connected transistor is firmly stated by physical relations. The I-V relation is given by:

$$I_C = I_S \left[\exp\left(\frac{qV_{BE}}{kT} \right) - 1 \right] \tag{1.17}$$

in which I_C is the collector bias current, I_S the collector saturation current, q the electron charge ($1.6 \cdot 10^{-19}$C), T the absolute temperature and k Boltzmanns constant ($1.38 \cdot 10^{-23}$J/K). The -1 term is negligible. Even for very small base-emitter voltages, the exponential term is already much larger.

The base-emitter voltage is the parameter of interest, so relation (1.17) is rewritten to make V_{BE} explicit. The expression for V_{BE} is:

$$V_{BE} = \frac{kT}{q} \ln\left(\frac{I_C}{I_S} \right). \tag{1.18}$$

With $\frac{kT}{q}$ the thermal voltage. At room temperature (≈ 300K) the thermal voltage equals:

$$\frac{kT}{q} \approx 26\text{mV}. \tag{1.19}$$

Because of the logarithm, a multiplicative change in the collector current becomes an additive change in the base-emitter voltage. For example, when the collector current is increased by a factor 10, the base-emitter voltage increases by 60mV. In the case of high-level injection, this increase is 120mV because of an additional factor 0.5 in the exponent of (1.17).

The temperature behavior

The temperature behavior of a junction voltage is easy to derive. This derivation is here more extensive because in a later paragraph the forward-biased junction is used as the core of a bandgap reference, and for this application the temperature behavior has to be well known. Equation (1.17) is changed into an equation with temperature-dependent variables:

$$I_C(T) = I_S(T) \exp\left[\frac{V_{BE}(T)q}{kT}\right]. \tag{1.20}$$

Then the temperature dependency is substituted for each variable. The temperature behavior of the collector current is determined by the bias current. It is assumed that the most convenient bias currents to realize are the currents with a temperature behavior equal to:

$$I_{\text{bias}} = I_{\text{bias}}(T_0)\left(\frac{T}{T_0}\right)^{\theta} \tag{1.21}$$

with T_0 a nominal temperature, $I_{\text{bias}}(T_0)$ the current at T_0 and θ the order of the temperature dependency (mostly θ is 0 or 1). The nominal temperature is the temperature from which later on the Taylor expansion is derived. The sources implementing this expression are treated in a later section.

For the temperature behavior of the saturation current, the following derivation suffices:

$$I_S(T) = \frac{qA{n_i}^2(T)\overline{D}(T)}{N_B} \tag{1.22}$$

in which A is the area of the junction, ${n_i}^2$ the intrinsic carrier concentration, $\overline{D}$ the mean minority-diffusion constant and N_B the Gummel number of the base region. For the intrinsic carrier concentration holds:

$${n_i}^2(T) = CT^3 \exp\left[-\frac{E_g(T)}{kT}\right] \tag{1.23}$$

with C a constant and $E_g(T)$ the bandgap energy as a function of the absolute temperature. The temperature dependency of $\overline{D}$ is found by using Einstein's relation. $\overline{D}(T)$ equals:

$$\overline{D}(T) = \frac{kT}{q}\overline{\mu}(T) \tag{1.24}$$

with $\overline{\mu}$ the mean mobility of the minority carriers in the base region. The temperature dependency of $\overline{\mu}$ can be defined as:

$$\overline{\mu}(T) = BT^{-n} \tag{1.25}$$

with B a constant and n the order of the temperature dependency. Putting all these equations together, the temperature dependency of the saturation current is given by:

$$I_S(T) = C' \left(\frac{T}{T_0}\right)^{\eta} \exp\left[\frac{-E_g(T)}{kT}\right] \tag{1.26}$$

with

$$\eta = 4 - n, \tag{1.27}$$

$$C' = \frac{T_0^{\eta} \cdot A \cdot B \cdot C \cdot k}{N_B}. \tag{1.28}$$

The combination of (1.20), (1.26) and (1.21) yields the temperature dependency of the base-emitter voltage:

$$V_{BE}(T) = \frac{E_g(T)}{q} - (\eta - \theta)\frac{kT}{q}\ln\left(\frac{T}{T_0}\right) + \frac{kT}{q}\ln\left(\frac{I_{C0}}{C'}\right) \tag{1.29}$$

with I_{C0} the collector bias current at the nominal temperature T_0. Two parameters, C' and I_{C0}, are eliminated when the equation for the base-emitter voltage is rewritten as:

$$V_{BE}(T) = V_{BE}(T) + \frac{T}{T_0}[V_{BE}(T_0) - V_{BE}(T_0)] \tag{1.30}$$

with $V_{BE}(T_0)$ the base-emitter voltage at the nominal temperature. For the temperature dependency of the base-emitter voltage a very convenient expression is found:

$$V_{BE}(T) = \frac{E_g(T)}{q} - \frac{T}{T_0}\left[\frac{E_g(T_0)}{q} - V_{BE}(T_0)\right] - (\eta - \theta)\frac{kT}{q}\ln\left(\frac{T}{T_0}\right). \tag{1.31}$$

This function is plotted in figure 1.12. At 0K the base-emitter voltage equals the bandgap voltage at 0K, $V_g(0)$, and for increasing temperature the base-emitter voltage decreases slowly.

To find the first-order temperature behavior of the base-emitter voltage the Taylor polynomial is examined. The first-order Taylor polynomial around T_0 is given by:

$$V_{BE}(T)_1 = V_{BE}(T_0) - \left[V_g(0)_1 + \frac{kT_0}{q}(\eta - \theta) - V_{BE}(T_0)\right]\frac{T - T_0}{T_0} \tag{1.32}$$

with $V_g(0)_1$ the bandgap voltage at 0K derived from a first-order Taylor polynomial of $V_g(T)$ near T_0. The temperature dependency of the base-emitter voltage is always negative and depends on the value of the base-emitter voltage. Further, the first-order approximation of the base-emitter voltage *always* intersects the y axis (T=0K) at:

$$V_{\text{geff}}(0)_1 = V_g(0)_1 + \frac{kT_0}{q}(\eta - \theta). \tag{1.33}$$

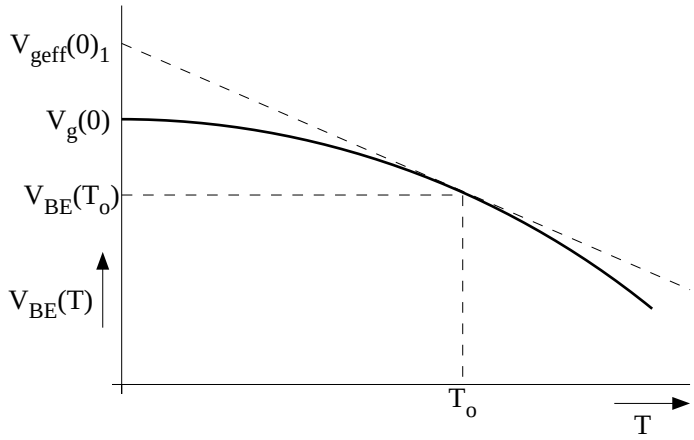

Figure 1.12: The base-emitter voltage as a function of the temperature

Example:
The temperature behavior of several base-emitter voltages is calculated in this example. For the constants holds: the bandgap voltage $V_g(0)_1$ equals 1.2V (silicon), $T_0 = 300$K and the temperature dependency of the saturation current is of the third order. In the following cases the temperature dependency is calculated:

I) $V_{BE}(T_0) = 600$mV and the transistor is biased with a constant current;

II) $V_{BE}(T_0) = 600$mV and the transistor is biased with a current which is proportional to the absolute temperature, PTAT;

III) $V_{BE}(T_0) = 800$mV and the transistor is biased with a constant current.

Results:

I) The transistor is biased with a constant current and the temperature behavior of the saturation current is of the third order, thus $\theta = 0$ and $\eta = 3$. The first-order temperature behavior equals:

$$\frac{dV_{BE}}{dT} \mid_{T=T_0} = -2.259\text{mV/K}. \tag{1.34}$$

II) Now the transistor is biased with a PTAT current, i.e. $\theta = 1$, the other variables remain the same. The first-order temperature coefficient equals:

$$\frac{dV_{BE}}{dT} \mid_{T=T_0} = -2.173\text{mV/K}. \tag{1.35}$$

III) In this case only the base-emitter voltage is changed with respect to I:

$$\frac{dV_{BE}}{dT} \mid_{T=T_0} = -1.592\text{mV/K}. \tag{1.36}$$

From the above it may be clear that the temperature behavior of the base-emitter voltage is dependent on the biasing conditions of the transistor. For higher base-emitter voltages the first-order temperature coefficient reduces. This can be seen from figure 1.12. The slope of the tangent at $V_{BE}(T_0)$ decreases for higher base-emitter voltages as the intersection point of the tangent with the y axis remains at $V_{\text{geff}}(0)_1$, which is independent of $V_{BE}(T_0)$.

When the base-emitter junction is used as an accurate voltage reference, a high degree of accuracy can be obtained. The value of the base-emitter voltage at a certain temperature is given by equation (1.18) and a simplified expression of the temperature behavior is given by equation (1.32).

The accuracy of the resulting voltage is determined by the accuracy of the saturation current I_S and the collector bias current I_C. The accuracy of the saturation current is given by the accuracy of the emitter area. The larger the emitter area is, the higher the degree of accuracy, because of the decreasing relative influence of stochastic errors in diffusion and mask lithography. The accuracy of the collector bias current is determined by the accuracy of the current itself and the way in which the transistor is biased. When, for instance, a very accurate current source is used for biasing the collector current, and this source is also used to supply the base-current, the resulting accuracy may be poor. A proper way of biasing is depicted in Figure 1.13. The biasing is

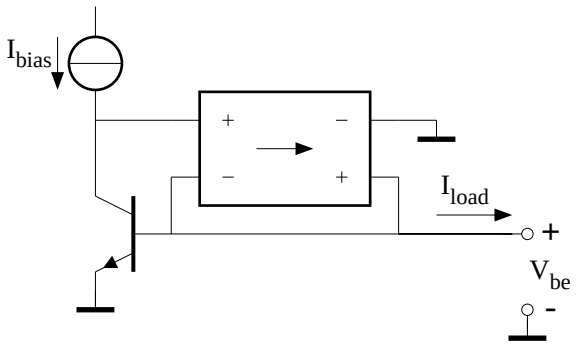

Figure 1.13: A proper way of biasing to get an accurate relation between V_{BE} and I_C

correctly done with the aid of a nullor. The nullor is an ideal circuit element. It controls its output current and voltage in such a way that the input voltage and current of the nullor become zero. In the circuit shown in figure 1.13, the nullor forces, by means of negative feedback, the base-collector voltage to be zero. Thus, the forward Early effect can be neglected. Further, because of the zero input current of the nullor, the current I_{bias} from the current source flows completely through the collector.

The load current is supplied by the nullor also. A load current cannot influence the collector current. Thus, the base-emitter voltage is buffered, ideally, by the nullor.

A realistic circuit uses an approximation for the nullor. The simplest is just a wire as depicted in figure 1.14. In this configuration, the transistor is connected as a diode and the base and load current are supplied by the collector bias source. This results in a difference between the actual collector current and the current supplied by the current source (the intended collector bias current).

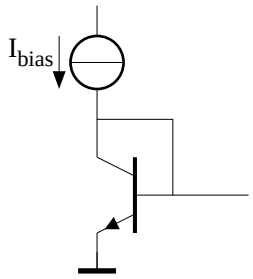

Figure 1.14: The nullor is implemented by a simple wire

As the transistor is diode connected, the output impedance $r_{\rm out}$ equals approximately:

$$r_{\rm out} = \frac{1}{g_m} \tag{1.37}$$

where g_m is the transconductance of the transistor. When this impedance is too high, the bias current needs to be enlarged. When this is not possible, the nullor has to be implemented by amplifying stages, instead of the simple wire.

The noise performance

The noise performance of the base-emitter junction reference is found by transforming all the noise sources to the output. The noise performance is dominated by the thermal noise of the base resistance r_b and the collector shot noise. The power-density spectrum of the noise voltage is approximately:

$$S_{V_{BE}} = 4kT(r_b + \frac{1}{2g_m}). \tag{1.38}$$

Reduction of the noise is possible by choosing a transistor with a lower base resistance (this can be done by taking several transistors in parallel) or by choosing a higher collector current. Which noise source is dominant depends on the specific circuit. In low-power circuits, mostly the collector shot noise is dominant and the noise of the base resistance is negligible.

For instance, a typical value for the base resistance of a minimal sized transistor is 500Ω. When the transistor is biased at 1μA, the equivalent noise resistor at the output, representing the collector shot noise, equals 13kΩ. Thus the noise of the base resistance is negligible.

When low-noise voltage references are needed, the use of base-emitter junctions is the correct choice. This is easily seen when the noise of the base-emitter voltage reference is compared with the noise of a voltage source that is made with a resistor and a current source.

Example:
A reference of 600mV is made with a large transistor (for a high absolute accuracy). Assume 100μA is available for the biasing of the transistor and its base resistance is 150Ω. The total equivalent noise resistor equals 280Ω. This voltage can also be realized by a current flowing

through a resistor. When the same bias current is used the required resistor equals:

$$R = \frac{U}{I} = \frac{0.6V}{100\mu A} = 6000\Omega. \tag{1.39}$$

Of course, the equivalent noise resistor is equal to this value. The noise power of the voltage reference made with the base-emitter junction is more than a factor 20 lower than the one made with the resistor.

The one-junction voltage reference can be very well used as a temperature sensor because of the good characterized temperature behavior. For instance, for a temperature dependency of approximately 2mV/K, a change in ambient temperature of 50K results in a change in the output voltage of 100mV. A voltage reference made by the difference of two junction voltages is discussed in the next section. The resulting expression for the temperature behavior is very accurate and simple.

1.3.4 The PTAT voltage source

The PTAT voltage source is a source with an output voltage which is proportional to the absolute temperature, or PTAT for short. Because of the proportionality to the absolute temperature, this voltage source is very well suited for use as a temperature sensor. The basis of a PTAT voltage source is the fact that the difference between two junction voltages is a PTAT voltage. The first section discusses a source that uses two transistors, each for one junction voltage. The following section treats a source where the two junctions in one transistor are used for the two required junction voltages, i.e. a saturating transistor.

Made with two transistors

The principle of a PTAT voltage using the difference between two base-emitter voltages is shown in figure 1.15. For the difference between two base-emitter voltages holds:

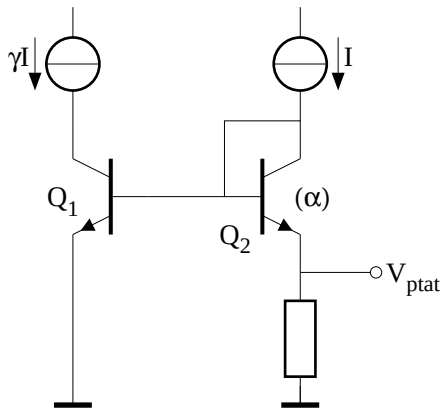

Figure 1.15: A PTAT voltage source using the difference between two base-emitter voltages

$$\Delta V_{BE} = V_{BE1} - V_{BE2} = \frac{kT}{q} \ln \left[\frac{I_{C1}(T)}{I_{C2}(T)} \cdot \frac{I_{S2}(T)}{I_{S1}(T)} \right]. \tag{1.40}$$

When the two collector currents have the same temperature behavior and the temperature behavior of the two saturation currents are equal, the expression simplifies to:

$$\Delta V_{BE} = \frac{kT}{q} \ln \left(\frac{I_{C1}}{I_{C2}} \cdot \frac{I_{S2}}{I_{S1}} \right) = \frac{kT}{q} \ln(\gamma\alpha) \tag{1.41}$$

with γ the ratio of the two collector currents and α the ratio of the two saturation currents. In figure 1.15, the collector currents of the two transistors are forced to have a ratio of γ. As the saturation current is proportional to the emitter area, α equals the ratio of the two emitter areas. From equation (1.41) follows that the difference between the two base-emitter voltages is PTAT.

Example: Assume the following holds for the collector and saturation currents:

- $I_{C1} : I_{C2} = 10 : 1$,
- $I_{S1} = I_{S2}$.

Then the PTAT voltage equals:

$$\Delta V_{BE} = \frac{kT}{q} \ln(10) = 199 \cdot \mu\text{V/K} \cdot T = 59.6\text{mV @ 300K}. \tag{1.42}$$

Thus for each degree Kelvin the temperature changes, ΔV_{BE} changes 199μV.

The output impedance, r_{out}, of this source equals:

$$r_{\text{out}} = \frac{1}{g_{m1}} + \frac{1}{g_{m2}} = \frac{kT}{qI} \left(\frac{1+\gamma}{\gamma} \right) \tag{1.43}$$

with g_{m1} and g_{m2} the transconductance of Q_1 and Q_2, respectively.

The power-density spectrum, S_u, of the PTAT voltage is given by the sum of the noise from the two base-emitter voltages and equals:

$$S_u = 4kT \left(r_{b1} + r_{b2} + \frac{0.5}{g_{m1}} + \frac{0.5}{g_{m2}} \right). \tag{1.44}$$

Using a saturated transistor

A very simple PTAT voltage source is the one that uses one saturated transistor. In this source, the two junction voltages are the base-emitter and the base-collector voltage. The difference between those two junction voltages is the collector-emitter voltage. The circuit is shown in figure 1.16. The transistor is saturated by forcing a base current into the base for which holds:

$$I_B \geq \frac{I_C}{\beta_f} \tag{1.45}$$

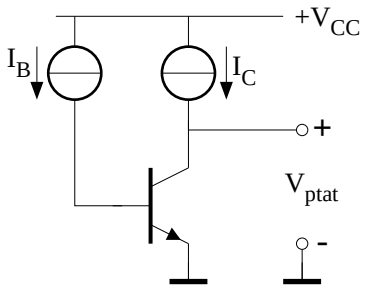

Figure 1.16: A PTAT voltage source using a saturated transistor

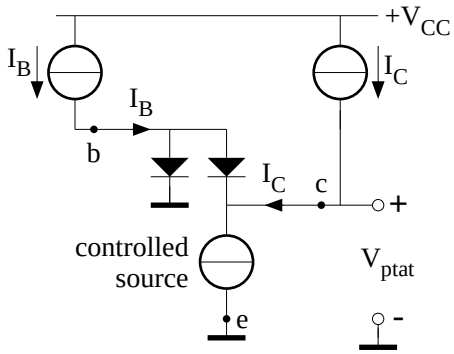

Figure 1.17: The collector-emitter voltage of a saturated transistor

with β_f the current-gain factor in the normal forward mode. The base-collector junction is also biased in the forward region. Thus, both junctions are conducting junctions and the collector-emitter voltage is determined by the difference between two junction voltages. This is depicted in figure 1.17. The collector-emitter voltage is given by:

$$V_{CE} = \frac{kT}{q} \ln \left(\frac{1 + 1/\beta_r + I_C/I_B\beta_r}{1 - I_C/I_B\beta_f} \right) \tag{1.46}$$

with β_r and β_f the reverse and forward current-gain factor in the normal regions, respectively. Both the collector current and the base current are forced into the transistor. This results in a "forced current-gain factor" β_{sat} of the saturated transistor and is defined by:

$$\beta_{\text{sat}} = \frac{I_C}{I_B}. \tag{1.47}$$

Substituting β_{sat} into the expression for the collector-emitter voltage, yields:

$$V_{CE} = \frac{kT}{q} \ln \left(\frac{1 + 1/\beta_r + \beta_{\text{sat}}/\beta_r}{1 - \beta_{\text{sat}}/\beta_f} \right). \tag{1.48}$$

Thus the collector-emitter voltage of a saturated transistor is PTAT. It is assumed that the three current-gain factors are temperature independent.

Example:
When for the three current-gain factors hold: $\beta_r = 3$, $\beta_f = 100$, $\beta_{\text{sat}} = 20$, the collector-emitter voltage equals:

$$V_{CE,\text{sat}} = 199\mu\text{V/K} \cdot T = 59.6\text{mV @ 300K}. \tag{1.49}$$

For higher output voltages, several saturating transistors may be stacked.

The small-signal output impedance of this source is given by the derivative of the collector-emitter voltage with respect to I_C, resulting in:

$$r_{\text{out}} = \frac{kT}{qI_C}\left(\frac{\beta_f}{\beta_f - \beta_{\text{sat}}}\right)\frac{1}{1 + (\beta_r + 1)/\beta_{\text{sat}}}. \tag{1.50}$$

For $\beta_{\text{sat}} \ll \beta_f$ and $\beta_r \ll \beta_{\text{sat}}$ this reduces to:

$$r_{\text{out}} = \frac{kT}{qI_C}. \tag{1.51}$$

The output impedance is similar to the impedance of a diode connected transistor and thus can be relatively low. For instance, for a collector current of 1mA the output impedance equals 25Ω.

The power-density spectrum, S_u, of the output noise voltage is again determined by the noise generated by the two junctions. S_u is given by:

$$S_u = 4kT\left(0.5\frac{kT}{qI_{BE}} + 0.5\frac{kT}{qI_{BC}}\right) \tag{1.52}$$

with I_{BE} the current flowing through the base-emitter junction and I_{BC} the current flowing through the base-collector junction.

1.3.5 The bandgap reference

When temperature-independent voltages are needed, the combination of a junction at avalanche breakdown and a forward-biased junction may suffice. However, the minimally required supply voltage is about 7V. In the growing area of low-voltage electronics, with supply voltages down to 1V, this kind of references is not feasible. Other types of references have to be used. A circuit that can still work at those low supply voltages is the bandgap reference.

A bandgap reference is a voltage source of which the output voltage is related to the bandgap voltage at 0K. Because this voltage is a constant, the output voltage of a bandgap reference is ideally temperature independent.

Equation (1.31) was found for the temperature behavior of the base-emitter voltage. This equation can be represented by a Taylor series around a nominal temperature T_0 as:

$$V_{BE}(T) = \alpha_0 + \alpha_1(T - T_0) + \alpha_2(T - T_0)^2 + \cdots \tag{1.53}$$

The objective of bandgap reference design is to cancel the temperature coefficients of this base-emitter voltage. This is possible by taking an appropriate linear combination of base-emitter

voltages:

$$\sum_{i=1}^{n} a_i V_{BE_i}(T) = \sum_{i=1}^{n} a_i \alpha_{0_i} + \sum_{i=1}^{n} a_i \alpha_{1_i}(T - T_0) + \sum_{i=1}^{n} a_i \alpha_{2_i}(T - T_0)^2 + \cdots \tag{1.54}$$

To obtain a temperature-independent reference voltage, V_{ref}, the first term on the right-hand side has to be equal to V_{ref} and the other terms on the right-hand side need to be zero. In this case the reference voltage is totally temperature independent. However, in most cases this is an overkill. Reasonable results can be obtained when only the first-order behavior is canceled, because this is by far the largest disturbing factor.

The linear combination of base-emitter voltages, an implicit compensation

In this section the linear combination of base-emitter voltages, in order to obtain a first-order compensated bandgap reference, is discussed. Because second and higher-order terms are not considered, only the first two terms of the Taylor series are used. For these two terms expression (1.32) was found. This equation can be rewritten to the convenient expression:

$$V_{BE}(T)_1 = V_{\text{geff}}(0)_1 - [V_{\text{geff}}(0)_1 - V_{BE}(T_0)] \left(\frac{T}{T_0}\right) \tag{1.55}$$

with $V_{\text{geff}}(0)_1 = V_g(0)_1 + \frac{kT_0}{q}(\eta - \theta)$ the effective bandgap voltage. This expression clearly shows the relation between the base-emitter voltage and the bandgap voltage.

Because only the constant term and the first-order behavior of the output voltage needs to be set, a linear combination of two base-emitter voltages is sufficient. The block diagram is depicted in figure 1.18. The linear combination is given by:

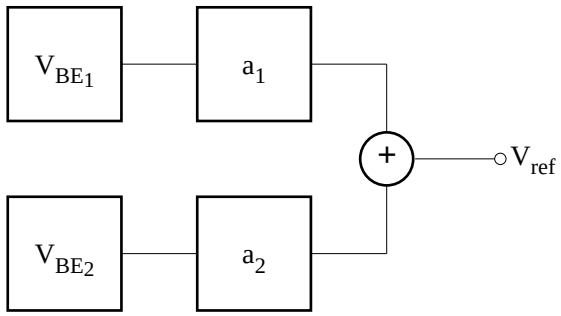

Figure 1.18: A linear combination of two base-emitter voltages

$$V_{\text{ref}} = (a_1 + a_2)V_{\text{geff}}(0)_1 - [(a_1 + a_2)V_{\text{geff}}(0)_1 - a_1 V_{BE_1}(T_0) - a_2 V_{BE_2}(T_0).] \left(\frac{T}{T_0}\right) \tag{1.56}$$

This equation may make the name “bandgap reference” clear: the reference voltage is directly related to the bandgap voltage and is given by:

$$V_{\text{ref}} = (a_1 + a_2)V_{\text{geff}}(0)_1. \tag{1.57}$$

The reference voltage can be set to all kinds of values by choosing the sum of the two scaling factors. Substitution of this expression in the first-order part of equation (1.56) results in a constraint for the first-order compensation:

$$a_1 V_{BE_1}(T_0) + a_2 V_{BE_2}(T_0) = V_{\text{ref}}. \tag{1.58}$$

From equations (1.57) and (1.58), the two scaling factors can be found to be:

$$a_1 = +\frac{V_{\text{ref}}}{V_{\text{geff}}(0)_1} \cdot \frac{V_{\text{geff}}(0)_1 - V_{BE2}(T_0)}{V_{BE1}(T_0) - V_{BE2}(T_0)}, \tag{1.59}$$

$$a_2 = -\frac{V_{\text{ref}}}{V_{\text{geff}}(0)_1} \cdot \frac{V_{\text{geff}}(0)_1 - V_{BE1}(T_0)}{V_{BE1}(T_0) - V_{BE2}(T_0)}. \tag{1.60}$$

These equations show that the two scaling factors have an opposite sign. This is because the first-order temperature coefficient of a base-emitter voltage is always negative. To obtain first-order compensation, the *difference* between the two base-emitter voltages has to be taken. Further, these two expressions show that the two base-emitter voltages have to be *different*. This is because equal base-emitter voltages have the same temperature dependency. Performing a first-order temperature compensation with equal V_{BE}s, and thus having the same temperature dependency, would result in a constant term equal to zero which is impractical.

The principle of the first-order temperature compensation with a linear combination of two $V_{BE}s$, is depicted in figure 1.19. In the figure, the base-emitter voltages do have a different value

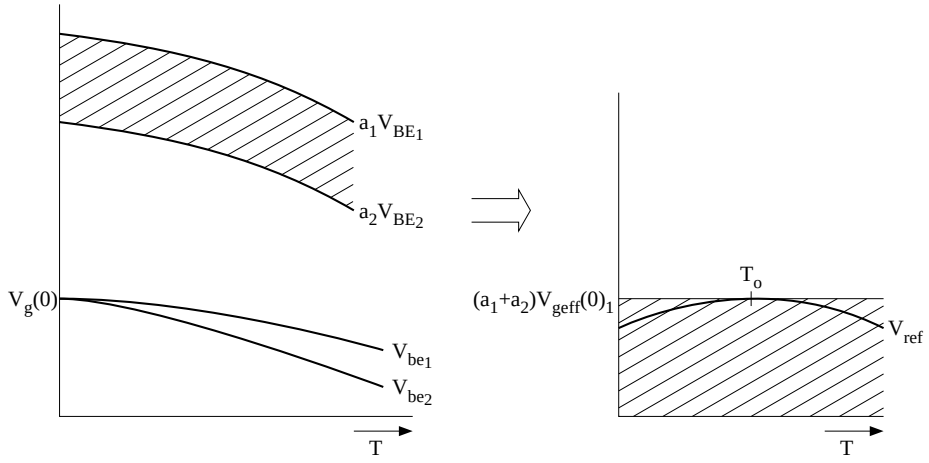

Figure 1.19: The principle of compensation with a linear combination

at T_0 and thereby a different first-order behavior. The remaining temperature behavior is of the second and higher order.

The noise behavior

In section 1.3.3, the noise behavior of a single-diode reference was discussed. In the previous section it was shown that the bandgap reference is just a weighted summation of a number of

those diode references (base-emitter voltages) . The power-density spectrum, S_v, of the noise voltage at the output of a bandgap reference is therefore given by:

$$S_v = 4kT\left[a_1^2\left(r_{b1}+\frac{1}{2g_{m1}}\right)+a_2^2\left(r_{b2}+\frac{1}{2g_{m2}}\right)\right]. \tag{1.61}$$

The noise is scaled by the same factor as the corresponding base-emitter voltages. Again, two types of noise sources are involved. The thermal noise of the base-resistances and the shot noise of the collector current. The former one can be lowered by using larger transistors with a lower base resistance. The latter can be decreased by using more current (g_m increases). For optimal use of the current with respect to noise, the influence of the base resistances has to be made negligible. This can easily be done for bias currents up to several 100μAs In this case the total noise (the implementations of the scaling factors a_1 and a_2 are assumed to be noiseless) is only from collector shot noise. When a noise minimization is done with the constraints of a first-order temperature-compensated bandgap reference and a limitation on the current consumption, the following holds:

$$\ln\left(x\frac{A_2}{A_1}\right) = -2\frac{1+x}{1-x} \tag{1.62}$$

with A_1 and A_2 the two emitter areas and x the ratio of I_{C1} and I_{C2}, the two collector currents. This expression states that:

For a given ratio of the two emitter areas, an optimal ratio of the two collector bias currents exists, for which the noise of the first-order compensated bandgap reference is minimal. This ratio is independent of the total current consumption $I_{C1}+I_{C2}$.

Note from the Editor: the equation above follows from taking into account (1.58), which gives a relation between a_1 and a_2, and (1.61), assuming r_{b1} and t_{b2} to be negligible, assuming the sum of I_{C1} and I_{C2} to be constant and minimizing S_v with respect to g_{m1} and g_{m2}.

A design example

In the previous sections, the theory of the bandgap reference was discussed using ideal $V_{BE}-I_C$ relations. In this section, a design example of a bandgap reference is presented using the Gummel and Poon model for $I_C = f(V_{BE})$. The $V_{BE}-I_C$ relation becomes more realistic, and the design aims at a minimization of the number of non-idealities that have to be taken into account. According to the Gummel and Poon model, the relation between the base-emitter voltage and the collector current for a normal biased transistor is:

$$I_C(T) = \left(1-\frac{V_{BC}}{V_{AF}}-\frac{V_{BE}}{V_{AR}}\right)\cdot\frac{I_{BE1}}{\frac{1}{2}\left[1+\left(1+4I_{BE1}/I_{KF}\right)^{NK}\right]} \tag{1.63}$$

with I_{BE1} defined as:

$$I_{BE1} = I_S(T)\cdot\exp\left(\frac{V_{BE}}{kT/q}\right) \tag{1.64}$$

and I_S according to:

$$I_S(T) = I_S(T_0) \cdot \exp\left[\left(\frac{T}{T_0} - 1\right)\frac{E_G}{kT}\right] \cdot \left[\frac{T}{T_0}\right]^{X_{TI}}. \tag{1.65}$$

When the transistor is biased far below high-level injection ($I_{BE1} \ll I_{KF}$) and the base-collector voltage is kept zero ($V_{BC} = 0$), (1.63) reduces to:

$$I_C(T) = \left(1 - \frac{V_{BE}}{V_{AR}}\right) \cdot I_S(T) \exp\left(\frac{V_{BE}}{kT/q}\right). \tag{1.66}$$

This is the same equation as (1.20) except for V_{AR} and some differences in the expression for $I_S(T)$. In the Gummel and Poon model, the parameter for the temperature behavior of I_S is X_{TI} instead of η. Further, the model uses a first-order temperature model for the bandgap energy.

V_{AR} is the reverse Early voltage. This parameter is used for describing the base-width modulation at the base-emitter junction. This Early voltage can be low, i.e. several volts. The errors in the base-emitter voltages, due to the V_{AR}, can be transformed to the output of the bandgap reference. The resulting error in the reference voltage equals:

$$V_{\text{error}} = \frac{kT}{q}\frac{V_{\text{ref}}}{V_{AR}}. \tag{1.67}$$

This error can be accounted for by adding to, for instance V_{BE1}, a term

$$V_{\text{additional}} = \frac{V_{\text{error}}}{a_1} \tag{1.68}$$

and by solving again the set of equations resulting from the linear combination.

From the foregoing, it appears that four parameters have to be known accurately: the key parameters. The other parameters have to be kept either as large or as small as possible. The four key parameters are:

- E_G the bandgap energy,
- I_S the saturation current,
- X_{TI} the order of temperature behavior of the saturation current,
- V_{AR} the reverse Early effect.

Now the blocks of the bandgap references need to be designed such that the simplifications made are valid. To obtain a base-emitter voltage according to relation (1.66) the topology of figure 1.20 can be used (c.f. figure 1.13). The nullor is implemented by a single MOS differential pair. The MOS transistor is favorable here because of the absence of a gate current so that the bias current I_C flows completely through the collector lead.

This cell is used as the core of a first-order compensated bandgap reference with an output voltage equal to $V_{\text{geff}}(0)_1$. According to (1.57), the sum of the two scaling factors is given by:

$$a_1 + a_2 = 1. \tag{1.69}$$

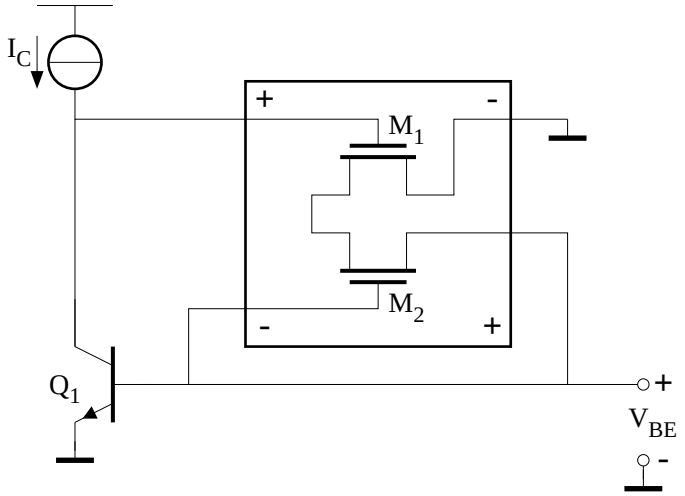

Figure 1.20: Generation of a base-emitter voltage

Because the sum of the two scaling factors equals one, equation (1.58) can be rewritten as:

$$\begin{aligned} V_{\text{ref}} &= (a_1 + a_2)V_{BE1}(T_0) + a_2[V_{BE2}(T_0) - V_{BE1}(T_0)] \\ &= V_{BE1}(T_0) + a_2[V_{BE2}(T_0) - V_{BE1}(T_0)]. \end{aligned} \tag{1.70}$$

The bandgap reference can thus be made by the topology as depicted in figure 1.21. The voltage scaler a_2 is realized by a bipolar differential pair, and resistors R_1 and R_2. The scaling factor is given by

$$a_2 = 1 + \frac{R_2}{R_1} \tag{1.71}$$

Here, a bipolar differential pair is used because of the low input-offset voltage. This voltage is directly in series with the reference voltage and thus needs to be as low as possible.

The two collector bias currents can be derived from a PTAT voltage source via a resistor. The resistor needs to be accurate because its absolute value is important. The ratio of the two currents is given by the equation for noise minimization.

There are a few important design aspects, with respect to integration, to pay attention to:

- Use large reference transistors for optimal matching. Take care that the effective emitter areas are equal (emitter crowding).
- Use relatively large-sized resistors for accurate scaling factors. The scaling factor depends only on the matching of the resistors.
- Place components to be matched close to each other.

Unfortunately, the total error in the output voltage of the bandgap reference may still be such that trimming is needed to obtain a temperature-independent voltage again. For this purpose R_1 or R_2 needs to be adjustable.

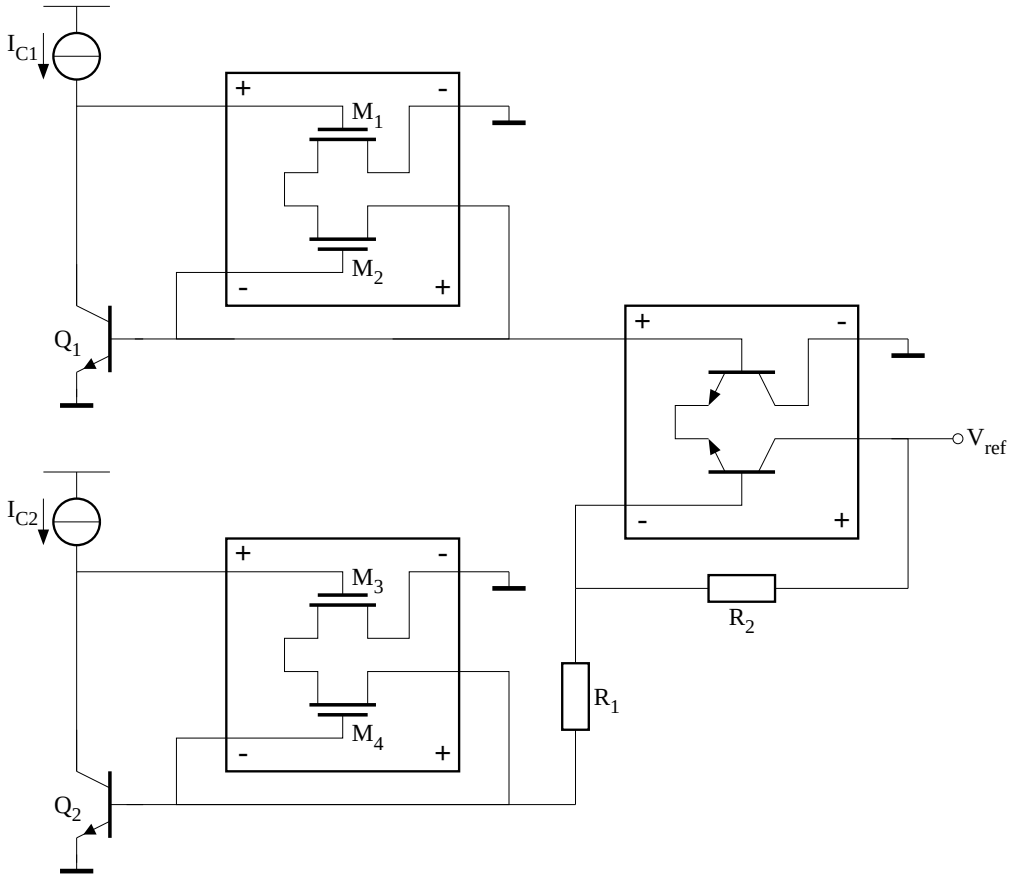

Figure 1.21: The topology of the bandgap reference circuit

The conventional way, an explicit compensation

In the previous section, the temperature behavior of a base-emitter voltage was compensated implicitly. Two scaled base-emitter voltages were added to set the output voltage and, at the same time, compensate the first-order temperature behavior. Both voltages have a constant and a first-order term. In this section, the temperature behavior is compensated explicitly. The compensation of the first-order temperature behavior of a base-emitter voltage is done by a separate PTAT voltage which is added to the base-emitter voltage. The principle of this method is depicted in figure 1.22. From this figure, it can be seen what has to be done to obtain a temperature-

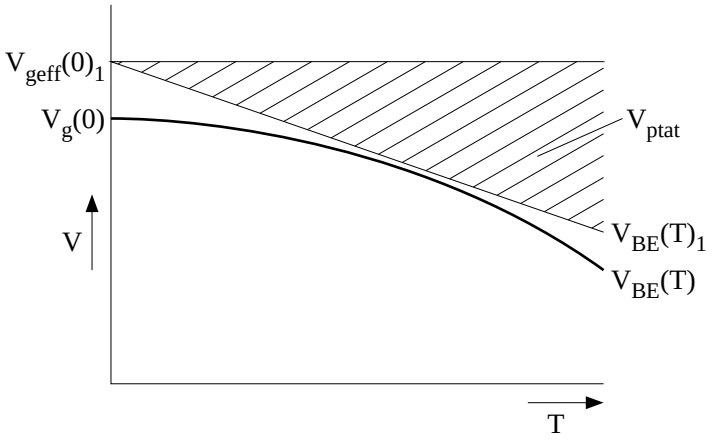

Figure 1.22: Explicit compensation of the temperature behavior of a base-emitter voltage

independent voltage equal to $V_{\text{geff}}(0)_1$. A voltage, represented by the shaded area, has to be added to a base-emitter voltage. This compensation voltage is zero at 0K and increases linearly for increasing temperature. Thus the compensation voltage needs to be PTAT. When the y axis is scaled by a factor a, an output voltage, V_{out}, equal to:

$$V_{\text{out}} = aV_{\text{geff}}(0)_1 \tag{1.72}$$

is obtained. In this case, the temperature behavior of a fraction a of a base-emitter voltage has to be compensated.

Assume a reference voltage equal to $V_{\text{geff}}(0)_1$ is required and transistor II from section 1.3.3 is used:

- $V_{BE}(T_0) = 600\text{mV}$,
- $\alpha_{1_{VBE}} = -2.173\text{mV/K}$ (transistor is biased with a PTAT current).

To compensate α_1, a PTAT voltage with a first-order temperature dependency of 2.173mV/K is required. In section 1.3.4, it was calculated that for a PTAT voltage source with emitter scaling one and current scaling ten holds:

- $V_{\text{PTAT}}(T_0) = 59.6\text{mV}$,

- $\alpha_{1,\mathrm{PTAT}} = 199\mu$V/K.

To attain total compensation, the PTAT voltage needs to be amplified by an factor A_V of :

$$A_V = \frac{-\alpha_{1,VBE}}{\alpha_{1,\mathrm{PTAT}}} = \frac{2.173mV/K}{198\mu V/K} = 10.92. \tag{1.73}$$

When the amplified PTAT voltage is added to the base-emitter voltage, the reference voltage equals at 300K:

$$V_{\mathrm{out}} = V_{BE} + A_V V_{\mathrm{PTAT}} = 0.6\mathrm{V} + 10.92 \cdot 59.6\mathrm{mV} = 1.25\mathrm{V} \tag{1.74}$$

and equals to:

$$V_{\mathrm{out}} = V_{\mathrm{geff}}(0)_1 = V_g(0)_1 + \frac{kT_0}{q}(X_{TI} - \theta) = 1.25\mathrm{V}. \tag{1.75}$$

This voltage has a temperature coefficient of 0mV/K at the nominal temperature 300K. The block diagram of the bandgap reference is depicted in figure 1.23.

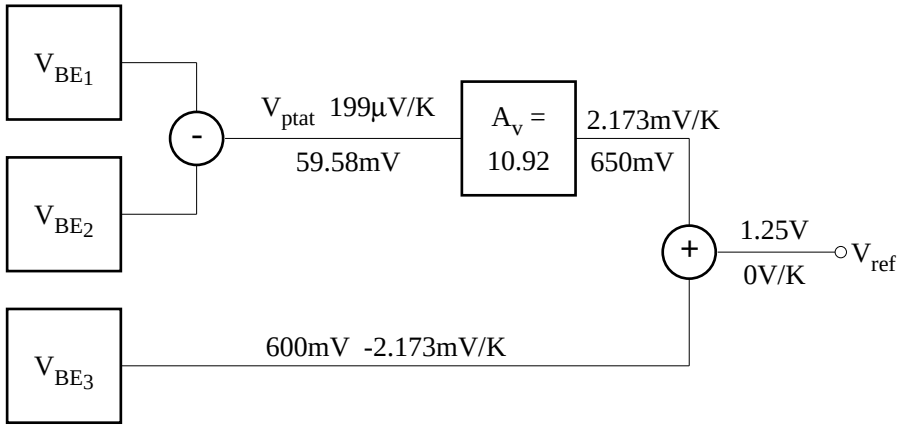

Figure 1.23: The block diagram of a bandgap reference with explicit compensation

Accuracy aspects

The design of accurate bandgap references relies on the compensation of one temperature-dependent voltage with another, thus, matching is evidently of prime importance. This can be seen from the expression describing the output voltage:

$$\begin{aligned} V_{\mathrm{ref}} &= (a_1 + a_2)V_{\mathrm{geff}}(0)_1 \\ &- \{a_1[V_{\mathrm{geff}}(0)_1 - V_{BE1}(T_0)] + a_2[V_{\mathrm{geff}}(0)_1 - V_{BE2}(T_0)]\}\,\frac{T}{T_0} \end{aligned} \tag{1.76}$$

The accuracy of several parameters is important:

- The scaling factors a_1 and a_2. These have to be implemented by ratios made of components with a good matching.
- $V_{BE1}(T_0)$ and $V_{BE2}(T_0)$. The transistors used should have matched emitter areas and the two collector bias currents should be derived with the help of matching.
- $V_g(0)$ and X_{TI}, via $V_{\text{geff}}(0)_1$. These are process parameters and their accuracy depends on process stability and, of course, on the accuracy of the parameter extraction.

Several parameters are involved in the design of the bandgap reference. All of them have more or less stochastic spread. Thus, one of the two scaling factors needs to be trimmed to account for this spread. Moreover, there is one more component that has a rather great influence up on the accuracy. This is the resistor by which the bias currents are related to a well-known voltage (most easy is a PTAT voltage). Its absolute value is important. Resistors on chip have an absolute accuracy of about 10 to 20%. The error caused by this uncertainty can easily by the major reason for trimming.

The design of bandgap references in MOS processes

There are two general ways of making a bandgap reference in a MOS process. Firstly, the parasitic substrate PNP can be used. See figure 1.24. The drawback of this method is the uncertainty

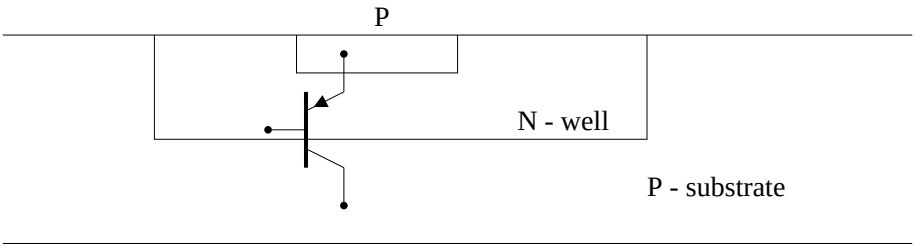

Figure 1.24: A parasitic PNP in a MOS process

in the collector current. For accurate bandgap reference design the relation between the base-emitter voltage and the collector current has to be used. In the case of a parasitic PNP transistor, the collector current is determined *indirectly* via the emitter current. The base current now influences the behavior of the base-emitter voltage.

Secondly, the bandgap reference can be made by using MOS transistors in weak inversion. In this case, the relation between the gate-source voltage and the drain current is exponential, as it is for bipolar transistors. The bandgap energy occurs in the same way in this relation as it does in the case of bipolar transistors. The problem is in the definition of the gate-source voltage. This is depicted in figure 1.25. The effective gate-source voltage is the voltage that is across the channel, V_{channel}. This effective voltage is related to the external voltage by the capacitive division of C_{ox} and C_{channel}. These two parameters directly introduce an uncertainty in the gate-source voltage. For accurate design, this ratio has to be well known.

Therefore, currently, for *accurate* bandgap reference design, a bipolar transistor process is best suited.

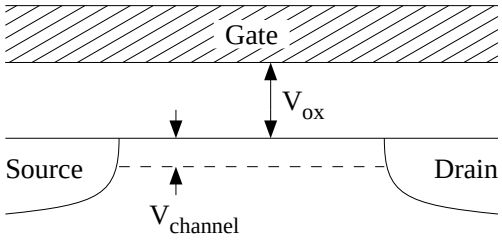

Figure 1.25: The gate-source voltage of a weak inversion MOS transistor

The influence of stress in a chip

After the wafer with bandgap references returns from the ic foundry, the bandgap reference is trimmed to obtain the low temperature dependency. Subsequently, the wafer is sawed into separate chips. Each chip contains a bandgap reference. Next, these chips are mounted in a package with glue, and the total package is heated to dry the glue. The problem arises in this last step. Due to the different thermal behaviors of the glue and the silicon, during this heating step stresses arise in the chip and the behaviors of the devices on the chip change slightly. Now the bandgap reference is no longer optimally trimmed and a second trim procedure has to be performed. This stress seems to depend on the orientation of the molecule lattice with respect to the surface, e.g. a perpendicular orientation or under a certain angle. The former is less sensitive to stresses than the latter.

Some concluding remarks

In this section, the first-order compensated bandgap reference has been discussed. With this reference, temperature dependencies of about some tens of ppm/K over a range of 100K can be obtained. When lower dependencies are needed, higher orders of the temperature behavior also have to be compensated for. These bandgap references, mostly called second-order compensated or curvature-corrected references, can have temperature dependencies of only 1ppm/K over a range of 100K.

1.3.6 Conclusions on voltage sources

In the foregoing sections, several ways of implementing voltage constants were discussed. The simplest implementation derives a voltage from the supply voltage by means of a resistive divider. This source consumes a rather high bias current to obtain a low output impedance and a low noise level.

The source using a non-linear device in the divider has a better performance. The forward-biased junction has shown to be a very good candidate for this non-linear device. A low-noise behavior combined with a low output impedance is feasible.

A voltage source with an output voltage which is Proportional To the Absolute Temperature (PTAT) is obtained when the difference between two junction voltages is used. The junctions may be from two separate transistors or from one saturating transistor, i.e. the base-emitter junction and the base-collector junction.

Finally, the bandgap reference was treated. This source has an output voltage that is related to the bandgap voltage at 0K and has, consequently, a temperature coefficient of 0V/K, ideally. When constructed with a linear combination of two base-emitter voltages, there is an optimal bias-current ratio for the two base-emitter voltage generators with minimum noise level. For the implementation of the bandgap reference, the absolute value of at least one resistor is important, which makes trimming inevitable.

1.4 The current source

In electronics there are voltage references (i.e. the bandgap voltage), currents references, however, do not exist because of the absence of a magnetic monopole. The current references which are realized are all derived from a voltage reference with the aid of a (trans)conductance. This is depicted in figure 1.26. When the voltage source is assumed to be ideal, the power-density

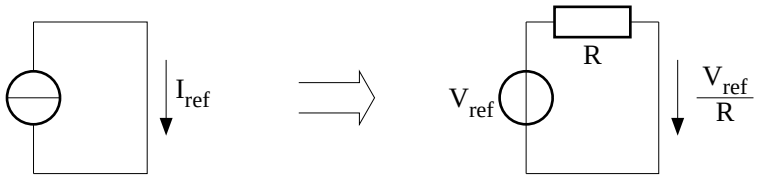

Figure 1.26: Derivation of a current source from a voltage source

spectrum S_i of the noise current at the output equals:

$$S_i = \frac{4kT}{R} \tag{1.77}$$

and can ideally be zero when a source with an infinitely high voltage is used such that an infinitely high resistance can be used. But in practice, the noise is worse than given in equation (1.77). This is because a current flowing through a resistor induces 1/f noise due to the granular structure of the resistive material. Especially in high ohmic resistors is the structure of the material relatively rough, for instance, in poly-silicon resistors. In metal film and diffused resistors this effect is of less influence.

When both high output impedances and high output currents are needed, this type of current source gives problems because high reference voltages are required. It is better to realize a high output impedance with an active circuit.

1.4.1 An active current source using a transconductance

The basic configuration of an active current source is given in figure 1.27 in which a nullor is used. The current is again given by:

$$I_{\text{ref}} = \frac{V_{\text{ref}}}{R}. \tag{1.78}$$

The output impedance is enlarged by the negative feedback, and is actually infinite due to the nullor. Ideally, the output impedance is independent of the resistor R.

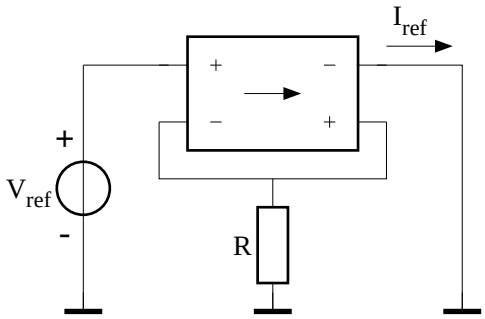

Figure 1.27: A current source realized by an active transconductane amplifier and a reference voltage

Using bipolar transistors

When the simplest implementation for the nullor is used, a CE stage, the series stage of figure 1.28 is obtained. The output current is given by (the base current is ignored):

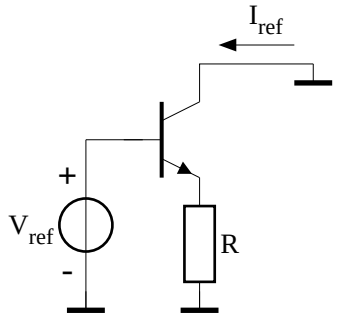

Figure 1.28: The nullor implemented by a single CE stage

$$I_{\text{out}} = \frac{V_{\text{ref}} - V_{BE}}{R}. \tag{1.79}$$

As the base-emitter voltage is temperature dependent, the output current of the source is temperature dependent also. Resistor R performs a feedback action, and through this a higher output impedance is obtained. To see what the increase of output impedance is as a function of the feedback (or loop gain), the output impedance is calculated. The output impedance equals:

$$r_{\text{out}} = \frac{(r_b + r_\pi)R}{r_b + r_\pi + R} + \beta r_o \frac{R}{r_b + r_\pi + R} + r_o = r_o + R + R\frac{\beta_f r_o - R}{r_b + r_\pi + R}. \tag{1.80}$$

This function is plotted in figure 1.29. The output impedance is normalized to r_o and the feedback resistor to r_π. For values of R much larger than r_π plus r_b the expression for the (maximum) output impedance becomes:

$$r_{\text{out,max}} = (\beta_f + 1)r_o. \tag{1.81}$$

Usually, this results in very high values for R. For 70% of the maximal output impedance, thus for $r_{\text{out}} = 0.7 \cdot r_{\text{out,max}}$, R needs to be approximately 2 times larger than r_π. Then, the voltage

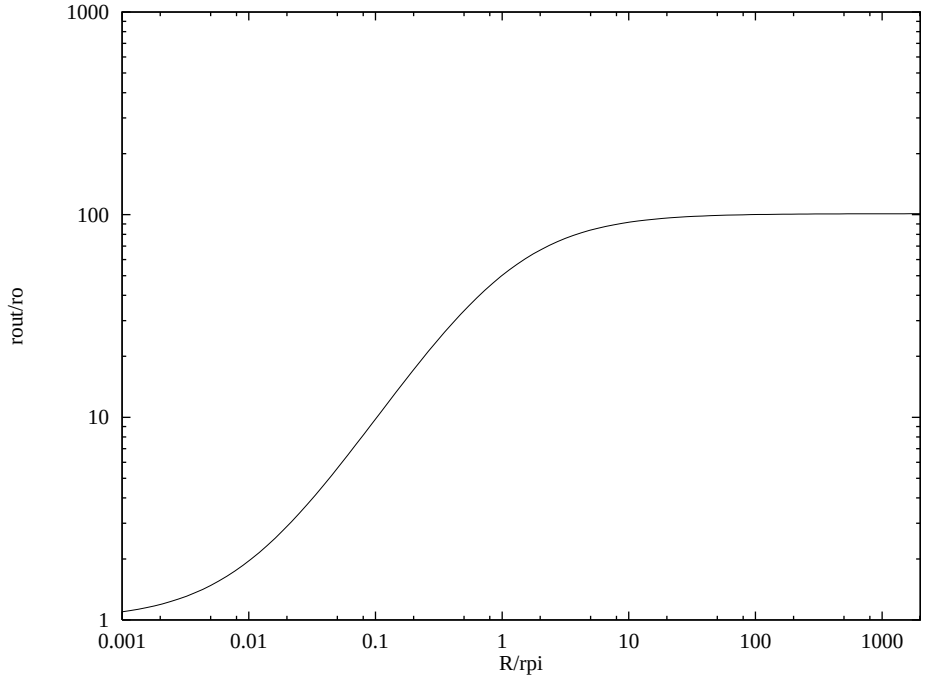

Figure 1.29: The normalized output impedance as a function of the normalized feedback resistor for β=100

across the feedback resistor equals:

$$V_R = I \cdot R = I \cdot 2r_\pi = I \cdot 2\beta\frac{kT}{qI} = 2\beta\frac{kT}{q} \tag{1.82}$$

For $\beta = 100$ and at room temperature the voltage across the resistor is about $5V$. This 5V constitutes a limitation for this type of current source. Because, in the increasing area of low-voltage design, i.e. a supply voltage of 1V, this current source cannot be so implemented. Another limitation is given by the required resistance. In low-current applications, the output current can easily be in the order of nAs or μAs, which is demanding for feedback resistors in the order of MΩs and GΩs.

Increasing the output impedance of the source shown in figure 1.28, without the need for very high resistances, can be realized in two ways:

- Increase of the loop gain ($\beta + 1$). Output current *variations* due to an output voltage variations are more suppressed. A better approximation is made for the nullor.
- Increase of the output impedance of the active part (r_o). Now the output impedance without loop gain is already higher.

For the first option, the nullor is implemented, for instance, with a two-stage bipolar amplifier. The output impedance increases by a factor β. The second option is obtained when the CE stage is cascoded, see figure 1.30. Transistor Q' is the cascode transistor. It is a current buffer for the

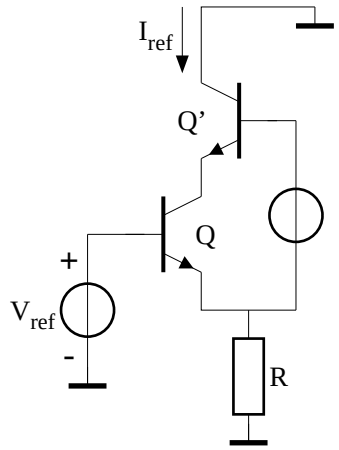

Figure 1.30: An active current source with a cascoded transistor

output of the CE stage, transistor Q. Without feedback, the output impedance of the buffered CE stage is approximately βr_o. When subsequently the feedback action is added to the current source, the output impedance can increase even further to approximately $\beta^2 r_o$. When a still higher output impedance is required, the loop gain has to be increased. An additional cascode transistor does not help.

Using FETs

The current source with one FET is depicted in figure 1.31. The nullor shown in figure 1.27 is

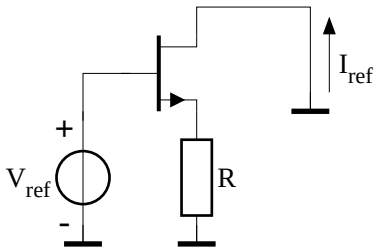

Figure 1.31: An active current source with a FET

now implemented with a CS stage. The output resistance equals:

$$r_{\text{out}} = R + (1 + g_m R) r_d \tag{1.83}$$

with r_d the small-signal output resistance of the FET and g_m its transconductance factor. In contrast with the output impedance for the bipolar source, which is limited to $(\beta_f + 1) r_o$, the output impedance of the FET source tends to infinity for a feedback resistor tending to infinity. But, again, high resistances are required. To increase the output impedance, without the need for high resistances, two options are possible:

- Make a better approximation for the nullor;

- Enlarge r_d by means of cascoding.

An example of the second option is depicted in figure 1.32. The output impedance of the cas-

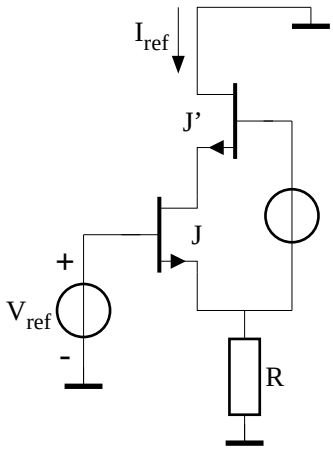

Figure 1.32: A FET current source with a cascoded FET

coded CS stage without the feedback is now:

$$r_{d,\text{cascode}} = g_m r_d \cdot r_d = \mu r_d. \tag{1.84}$$

The output impedance is increased by a factor equal to the voltage-gain factor of the FET. For each additional cascode FET, the output impedance increases a factor μ, in contrast to the bipolar implementation where a second cascode transistor does not help.

The difference in the behavior of the current source made by the bipolar transistor and the FET is caused by the nature of the effect that causes the finite output impedance of these devices:

- Bipolar: r_o is caused by base-width modulation at the *base-collector* junction;
- FET: r_d is caused by the channel-length modulation, i.e. a *source-drain* effect.

In the case of the bipolar transistor, a part $1/\beta_f$ of the current (the base current) leaks away via the base terminal. This leakage current is not seen by the feedback. The FET does not have this "leakage". Theoretically an infinite impedance can be obtained with only cascoding.

Noise behavior

In this section, the influence of the amount of feedback on the noise behavior is discussed. The current source with all its noise sources is depicted in figure 1.33. The power-density spectrum S_i of the equivalent noise current at the output follows from shifting and transforming all noise sources to the input and multiplying the equivalent input noise voltage power-density spectrum

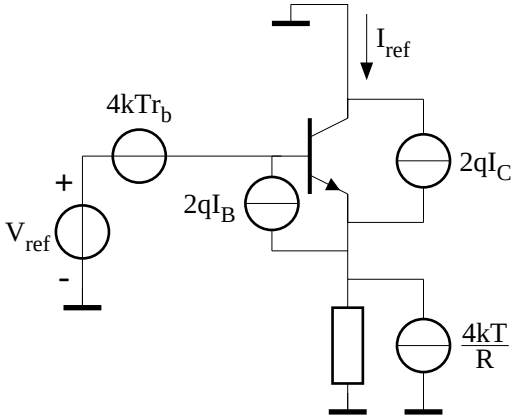

Figure 1.33: The noise sources in the active current source

$S_v$with the square of the voltage-to-current transfer G. The result is given by:

$$S_i = G^2 \cdot S_v = G^2 \left[\frac{2qI_C}{g_m^2} + 2qI_B(R + r_b) + 4kTR + 4kTr_b \right] \tag{1.85}$$

$$= \left[\frac{\beta}{r_b + r_\pi + R(1+\beta)} \right]^2 \left[\frac{2qI_C}{g_m^2} + 2qI_B(R + r_b) + 4kT(R + r_b) \right] \tag{1.86}$$

$$\approx \frac{2qI_C}{(1 + \beta R/r_\pi)^2} + \frac{2qI_B}{(1 + r_\pi/\beta R)^2} + \frac{4kT(R + r_b)}{(R + r_\pi/\beta)^2}. \tag{1.87}$$

The first term the latter equation represents the effect of the collector shot noise. For very high feedback-resistor values, this term disappears completely. The second term is due to the base shot noise. For very high values for R this term reduces to $2qI_B$. The last term accounts for the noise of the feedback resistor and the base resistance. This term vanishes for high values of the feedback resistor. The function is plotted in figure 1.34. The noise-power density has been normalized to $2qI_C$ and the feedback resistor has been normalized to r_π.

To obtain the minimum noise-power density level, of $2qI_B$, a rather high value for the feedback resistor is required (c.f. the discussion about increasing the output impedance by negative feedback). A +3dB point, with respect to the minimal value, is obtained when the resistor is chosen such that the noise due to the resistor equals the base shot noise. In this case, the noise of the base resistance can, in general, be neglected. Then, R equals:

$$R = \frac{2\beta_f}{g_m}. \tag{1.88}$$

Mostly $\beta_f \approx 100$ and with $kT/q \approx 26$mV the voltage across R equals:

$$V_R = I_C R = 2\beta \frac{kT}{q} \approx 5\text{V} \tag{1.89}$$

This is the same value as for the -3dB in the output impedance as a function of the feedback resistor. Apparently high-quality current sources need a supply voltage of minimally 5V.

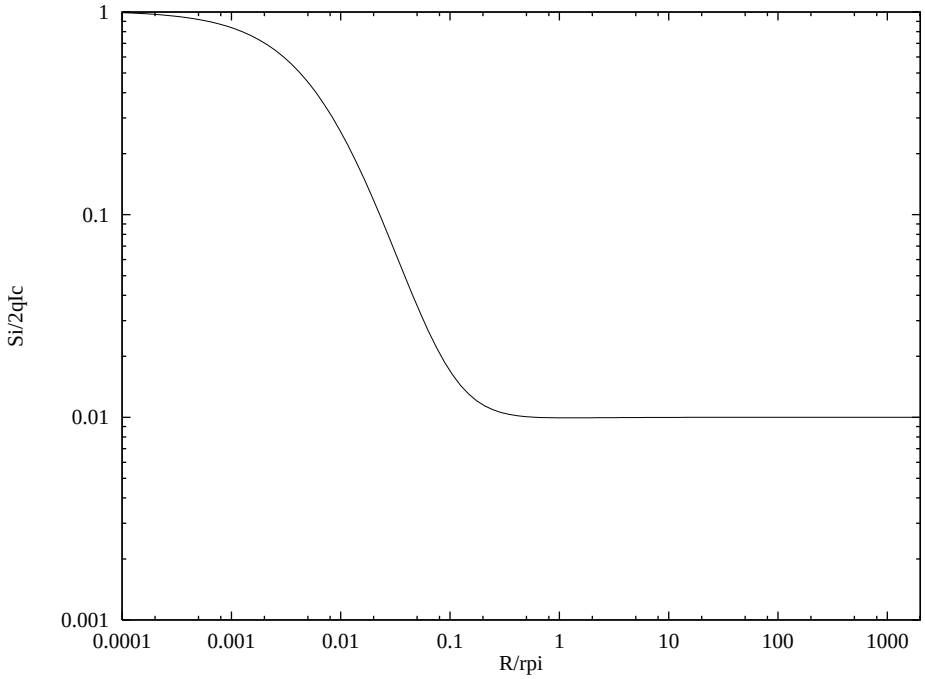

Figure 1.34: The noise of an active current source as function of the feedback resistor. The noise is normalized to $2qI_C$ and the feedback resistor to r_π and $\beta = 100$.

HF behavior

In the previous, sections only the dc behavior of the current source was discussed. However, that is only one part of the story. The current source has to behave well for high-frequency signals also, i.e. its output impedance has to remain relatively high. In figure 1.35, the source with its parasitic capacitances is depicted. The output impedance is given by:

$$r_{\rm out}(j\omega) = \frac{r_{\rm out}(0)}{1 + j\omega r_{\rm out}(0)(C_\mu + C_{js})} \tag{1.90}$$

and has a pole at

$$p = \frac{-1}{r_{\rm out}(0)(C_\mu + C_{js})}. \tag{1.91}$$

For frequencies above $1/[r_{\rm out}(0)(C_\mu + C_{js})]$ the output impedance is dominated by the parallel capacitance $(C_\mu + C_{js})$. The effectivity of cascoding, at relatively high frequencies, depends on the values of C_μ and C_{js}. Four situations are depicted in figure 1.36. Function 1 depicts the output impedance of a single CE stage, no feedback or cascoding is used. Function 2 represents the output impedance of the source when feedback is used. The low-frequency impedance is increased. The high-frequency impedance is not affected by the feedback. Both capacitors $(C_\mu + C_{js})$, are still in parallel with the high output impedance of the series stage (see figure 1.35). The current leaking away through the two capacitors is not "seen" by the feedback resistors and, consequently, the feedback loop cannot suppress these currents. Function 3 depicts the output

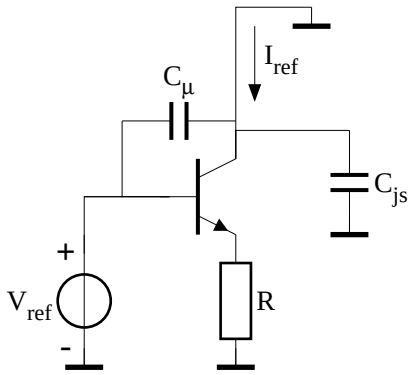

Figure 1.35: The parasitics of the active current source

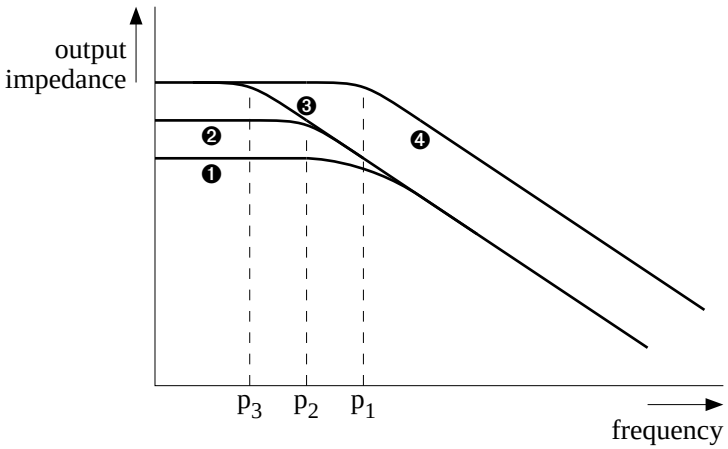

Figure 1.36: The effect of cascoding on the high-frequency output impedance: 1) without feedback and cascoding, 2) only feedback used, 3) feedback and cascoding is used, 4) as 3 but without substrate capacitors

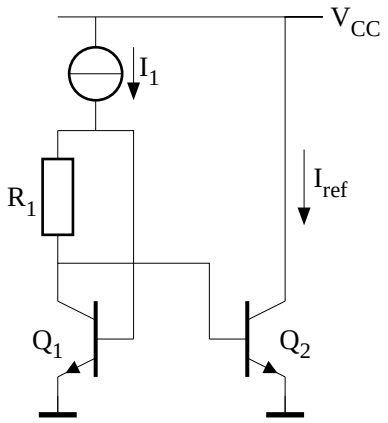

Figure 1.37: The peaking current source

impedance of the source when cascoding is also used. The low-frequency output impedance is increased further. The high-frequency output impedance is again not affected. A substrate capacitor is still in parallel with the output impedance of the source (It is assumed that C_{js} is much larger than C_μ). Function 4 depicts the output impedance of a source using feedback and cascoding when no substrate capacitance is present. The high-frequency impedance is drastically increased. All the parasitic capacitors are part of the feedback loop and thus their influence is suppressed.

It may be clear that negative feedback and cascoding does not decrease the *influence* of substrate capacitors. However, when the *capacitance* of the parasitics is decreased, some profit can be obtained. When a PNP transistor is used instead of the NPN, the sign of the current is changed but the output capacitance is decreased, because the substrate capacitor is connected to the base of the PNP and thus cascoding may help.

Still, when all the measures are taken, the output impedance may be too low at (very) high frequencies. A very straightforward method used in HF design is putting a resistor in series with the current source. The output impedance is now, at high frequencies, dominated by this resistor instead of by the parasitic capacitance.

1.4.2 The peaking current source

The peaking current source is a special type of current source. The circuit is shown in figure 1.37. The relation between I_1 and $I_{\rm ref}$ is given by:

$$\ln\left(\frac{I_{\rm ref}}{I_{S2}}\right) = \ln\left(\frac{I_1}{I_{S1}}\right) - \frac{I_1 R_1}{\frac{kT}{q}} \tag{1.92}$$

or

$$I_{\rm ref} = I_1\left(\frac{I_{S2}}{I_{S1}}\right)\exp\left(-\frac{I_1 R_1}{\frac{kT}{q}}\right) \tag{1.93}$$

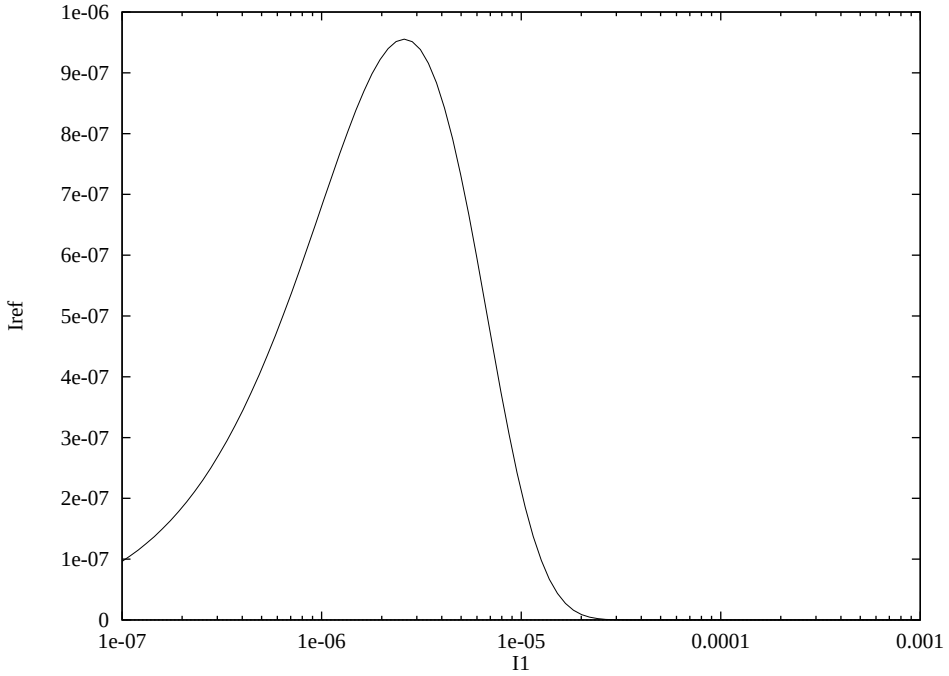

Figure 1.38: The relation of the input and output current (I_1 and $I_{\rm ref}$) of the peaking current source

with I_{S1} and I_{S2} the saturation currents of Q_1 and Q_2, respectively. The function is depicted in figure 1.38 with $\frac{kT}{q} = 26$mV, $I_{S1}/I_{S2} = 1$ and $R_1 = 10\text{k}\Omega$. This function exhibits a peak, which explains the name "peaking current source". At this extreme, a deviation in I_1 is not transferred to I_2. The source is biased at this extreme when:

$$RI_1 = \frac{kT}{q}. \tag{1.94}$$

When the voltage across R is equal to the thermal voltage, a change in the current I_1 is totally suppressed. No change in the output current is seen. At this extreme, the ratio between the input and output current is given by:

$$\frac{I_2}{I_1} = \frac{1}{\text{e}} \left(\frac{I_{S1}}{I_{S2}} \right). \tag{1.95}$$

An example of a peaking current source of 100μA is given in figure 1.39. The current in the left branch, I_1, must be 272μA. At 300K, R_1 must have a value of 95Ω (1.94). The current source on top of the left branch (figure 1.37) is implemented by resistor R_2 and must have a value of:

$$R_2 = \frac{V_{\rm CC} - V_{BE}}{272\mu\text{A}} \approx 15.8\text{k}\Omega \tag{1.96}$$

in the case of $V_{\rm CC} = 5$V and $V_{BE} = 0.7$V.

Only resistor R_1 needs to be accurate. This poses no problem because it has a rather low value. On chip, a relatively wide resistor can be used. For resistor R_2, it is not necessary to

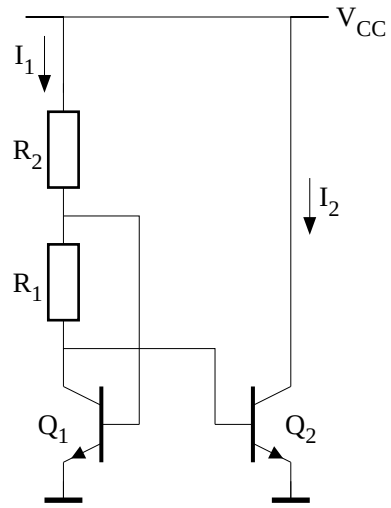

Figure 1.39: An example of a peaking current source

be accurate because small changes in R_2 can be seen as small changes in I_1 and these are not transferred to I_2. For R_2, a rather thin resistor can be used.

As a consequence of the suppressing of small changes in I_1, this type of current source exhibits a very high PSRR. Even better results can be obtained by the enhanced peaking current source. This source is depicted in figure 1.40. The current mirror (to be discussed in section 1.5) at the top of the source forces the ratio of the two branch currents to be constant.

The non-ideality which has the most dominant influence on the performance of this source is the Early effect. When this effect is taken into account, the optimum bias condition is changed. The optimal ratio of the two branch currents equals in this case:

$$\frac{I_2}{I_1} = \exp\left(-\left[1+\frac{V_{AF-pnp}}{V_{AF-npn}}\right]\left[1-\frac{2V_{CE,\mathrm{pnp}}}{V_{AF,\mathrm{pnp}}}\right]\right) \tag{1.97}$$

with $V_{AF,\mathrm{npn}}$ and $V_{AF,\mathrm{pnp}}$ the forward Early voltages of the npn and pnp transistor, respectively. A current variation of only 0.05% over a supply voltage range of 10V can be obtained with this source.

1.5 The current mirror

The current mirror is a rather general-purpose circuit. The current mirror can be used as:

- current inverter/amplifier,
- bias source,
- translinear circuit.

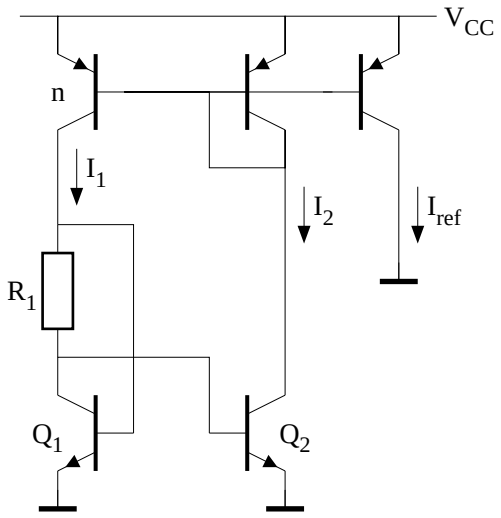

Figure 1.40: The enhanced peaking current source

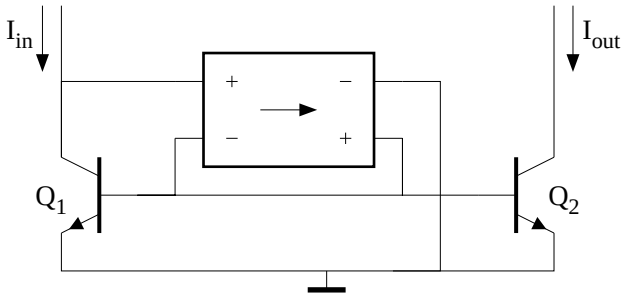

Figure 1.41: The basic current mirror

The current mirror is usually used as a current source. The mirror when used as a translinear circuit is discussed in another chapter. The basic current mirror, based upon two bipolar transistors, is given in figure 1.41. The nullor forces the input current to flow completely through the collector terminal of Q_1 and the output transistor mirrors that current. When the output transistor is chosen to be n times larger than the input transistor, and the Early effect of the transistor is negligible, the output current equals n times the input current:

$$I_{\text{out}} = nI_{\text{in}}. \tag{1.98}$$

By choosing the input transistor to be larger than the output transistor, n can be made smaller than one.

The simplest current mirror is depicted in figure 1.42. In this current mirror, the nullor is implemented by just a wire. Due to several non-idealities, the ratio of the input and output current is not exactly equal to n.

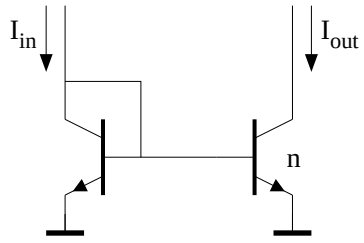

Figure 1.42: The simplest current mirror

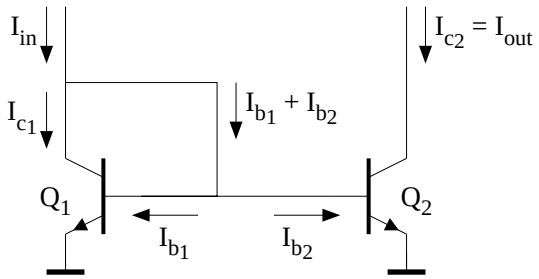

Figure 1.43: The simplest current mirror with all the currents flowing in the circuit depicted

1.5.1 Errors in the mirror factor

There are three main sources of error in the current mirror shown in figure 1.42, namely:

- the base current (finite β),
- mismatch in the emitter areas,
- the Early effect.

Errors due to the base currents

In figure 1.43, the simplest current mirror is again depicted but now with all the currents flowing in the mirror and a scaling factor of 1. The output current is equal to the collector current of the input transistor and is equal to:

$$I_{\text{out}} = I_{C1} = I_{\text{in}} - \frac{I_{C1}}{\beta_1} - \frac{I_{C2}}{\beta_2}. \tag{1.99}$$

Consequently, the transfer equals:

$$\frac{I_{\text{out}}}{I_{\text{in}}} = \frac{1}{1 + 2/\beta}. \tag{1.100}$$

The higher the current-gain factor is, the smaller the difference between the input and output current and the closer the transfer approaches 1. The relative error is:

$$\frac{I_{\text{in}} - I_{\text{out}}}{I_{\text{in}}} = \frac{1}{1 + \frac{1}{2}\beta}. \tag{1.101}$$

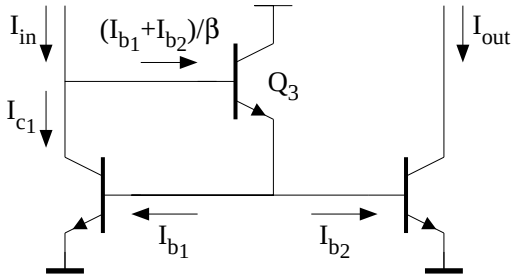

Figure 1.44: A current mirror with a reduced influence of the base currents

It is assumed that the transistors have equal current-gain factors. The influence of the base currents can be minimized by using a better implementation for the nullor shown in figure 1.41. This is depicted in figure 1.44. The nullor is now implemented by a CE stage. For the input and output currents holds:

$$I_{\text{in}} = I_{C1} + \frac{I_{C1} + I_{C2}}{\beta^2} \tag{1.102}$$

and

$$I_{\text{out}} = I_{C1} \tag{1.103}$$

again with equal emitter areas. The relative error is given by:

$$\frac{I_{\text{in}} - I_{\text{out}}}{I_{\text{in}}} = \frac{1}{1 + \frac{1}{2}\beta^2}. \tag{1.104}$$

The influence of the base current is decreased by a factor β. This equals the increase of loop gain in the mirror due to Q_3.

Errors due to mismatch in emitter areas

In practical implementations, the two emitter areas are never exactly the same size. There is always a mismatch between them. Because of the linear dependence of the saturation current of the transistor on the emitter area, the two saturation currents have the same mismatch. Assume the two emitter areas, A_1 and A_2, relate to each other as:

$$A_1 = (1 + \Delta)A_2 \tag{1.105}$$

with Δ the relative matching error. The relative error of the input and output current is then given by:

$$\frac{I_{\text{in}} - I_{\text{out}}}{I_{\text{in}}} = \frac{A_1 - A_2}{A_1} = \frac{\Delta}{1 + \Delta} \approx \Delta. \tag{1.106}$$

It is assumed that the matching is not too bad, thus $\Delta \ll 1$. The relative error in the mirror factor is equal to the relative error in the emitter areas.

The error due to mismatch can be reduced by the use of emitter resistors. This is depicted in figure 1.45. Now the mirror factor is not only determined by the transistor areas but by the

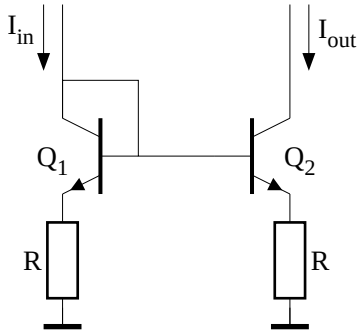

Figure 1.45: A current mirror with emitter resistors

emitter resistors also. For the maze of this mirror holds:

$$I_{\text{in}}R + V_{BE1} = I_{\text{out}}R + V_{BE2}. \tag{1.107}$$

The relative error in the mirror factor, Δ', for the current mirror using emitter resistors is defined as:

$$\Delta' = \frac{I_{\text{in}} - I_{\text{out}}}{I_{\text{in}}}. \tag{1.108}$$

Combining equations (1.107) and (1.108) results in:

$$\begin{aligned} \frac{(I_{\text{in}} - I_{\text{out}})R}{\frac{kT}{q}} &= \ln\left(\frac{I_{\text{out}}}{I_{\text{in}}} \cdot \frac{A_1}{A_2}\right) && (1.109)\\ &= \ln(1-\Delta') - \ln(1-\Delta) && (1.110)\\ &\approx \Delta - \Delta' && (1.111)\\ . && (1.112) \end{aligned}$$

Rewriting for Δ' yields:

$$\Delta' = \Delta\left(\frac{1}{1 + \frac{I_{\text{in}}R}{kT/q}}\right). \tag{1.113}$$

The mismatch error is approximately reduced by a factor equal to the ratio of the voltage across the emitter resistor and the thermal voltage. As was seen in the previous section, the emitter resistors also reduce the noise level and increase the output impedance of the mirror. A drawback is the required higher power-supply voltage. The use of emitter resistors improves the performance of the mirror considerably, but, for optimal performance, more than 5V supply voltage is required.

Of course, the matching of the resistors is important. For large voltages across the resistors, the transistor mismatch becomes negligible, only the mismatch of the resistors remains. However, usually, the matching of resistors is better than the matching of transistors because they are larger.

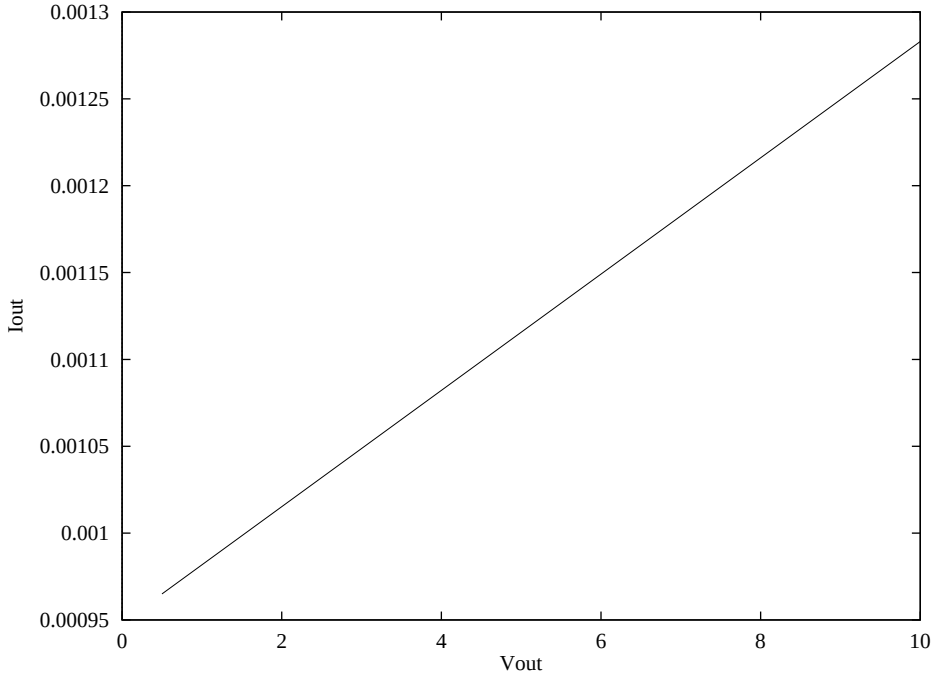

Figure 1.46: The influence of the output voltage on the output current

Errors due to the Early effect

The influence of the Early effect on the mirror factor is depicted in figure 1.46. The input current equals 1mA, and the output current varies between approximately 1 and 1.3mA. It is clear that major errors can occur due to the Early effect, i.e. the output impedance, of the transistor. There are two solutions for this problem. They can be used simultaneously:

- Use emitter resistors to increase the output impedance;
- Use a voltage follower which makes the two collector voltages equal.

The mirror with reduced Early effect is depicted in figure 1.47. Because of the emitter resistors the influence of the Early effect reduces, and the output impedance increases, as discussed in section 1.4.1. A further reduction of the error is attained by ensuring the equality of the two base-collector voltages. Q_3 is used as a voltage follower. The difference between the input and output voltage is one base-emitter voltage. The second pnp transistor, Q_4, is used as a level shift of one base-emitter voltage to compensate for this remaining difference. Now both base-collector voltages are equal and the error due to the Early effect is reduced even further.

The influence of the base currents is the same as it is in the simplest current mirror. Because PNP Q_3 functions as a current follower for the base currents of Q_1 and Q_2, the difference of the input current and the collector current I_{C1} is still the two base currents of Q_1 and Q_2. The output current of the mirror as a function of the output voltage is depicted in figure 1.48. Again an input current of 1mA was chosen. The influence of the output voltage on the mirror factor is decreased dramatically.

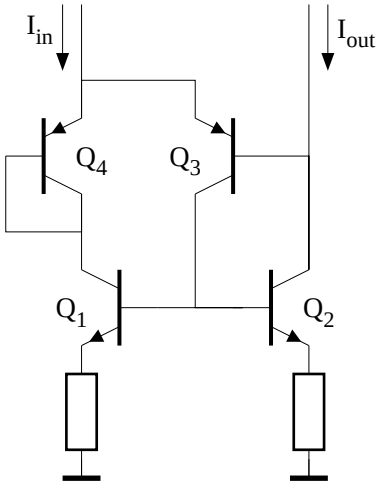

Figure 1.47: A current mirror with a reduced Early effect

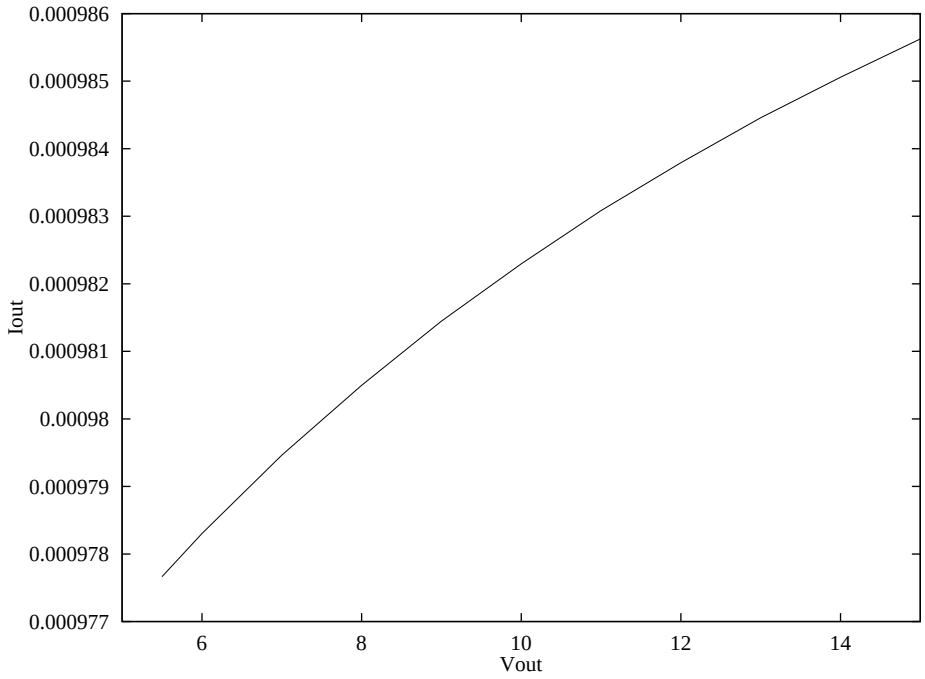

Figure 1.48: The output current as a function of the output voltage

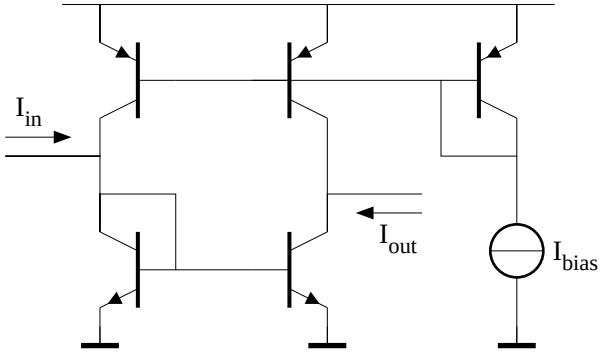

Figure 1.49: A PNP-like mirror with the frequency behavior of NPNs

High-frequency behavior

To examine the high-frequency behavior of the current mirror, the current-gain factor of the transistors, is described by:

$$\beta_f = \beta_0 \cdot \frac{1}{1 + j\omega\tau_f\beta_0}. \tag{1.114}$$

The pole at $-1/\beta_0\tau_f$ represents the finite bandwidth of the transistors. Substitution of this expression for β in the expression for the transfer of the current mirror (1.100) results in:

$$\frac{I_{\text{out}}}{I_{\text{in}}} = \frac{1}{1 + 2/\beta_0} \cdot \frac{1}{1 + 2j\omega\tau_f}. \tag{1.115}$$

The high-frequency behavior is given by a pole at half the transit frequency of the transistor. Of course, the substrate capacitance and the collector bulk resistance have influence on the high-frequency behavior also.

In bipolar processes, the npn characteristics are optimized and the pnp transistor is mostly a lateral transistor with minor HF behavior with respect to the npn. For example in the DIMES-01 process:

pnp: $\tau_f = 8ns \rightarrow f_t = 20$MHz,

npn: $\tau_f = 30ps \rightarrow f_t = 5$GHz.

Sometimes in a design, a PNP mirror seems to be needed in the signal path. In such a case, the current mirror would introduce a pole at 10Mhz in the signal path. This can be a very inconvenient pole. However, it is possible to make a PNP-like mirror with the frequency behavior of an NPN mirror. The mirror is depicted in figure 1.49. The PNP mirror is taken away from the signal path and only used for biasing an NPN mirror. The NPN mirror performs the mirror function for the signal. The behavior of the PNP mirror is only important in respect to dc. Of course, the output impedance of the PNP mirror needs to be high in relation to the NPN mirror. The pole of this mirror is now at 2.5GHz.

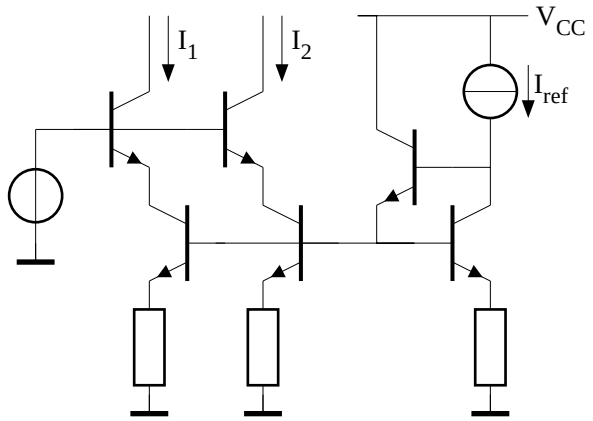

Figure 1.50: A current mirror extended to a current copier

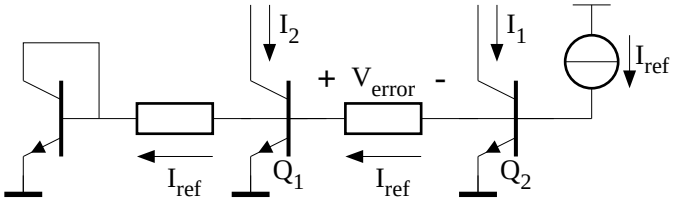

Figure 1.51: Errors due to incorrect wiring

1.5.2 Copying currents

When the current mirror is extended with additional output stages, a current copier is obtained. This copier is depicted in figure 1.50. The matching between I_1 and I_2 is equal to the matching of the emitter resistors. This can be very good. The matching between the input and output currents is as it is for the current mirror. Again the cascoding is needed for the reduction of the Early effect. When these current copiers are realized, care has to be taken with the connection of the base and emitter terminals. If there is a voltage drop across the wiring the effective base-emitter voltages can differ from each other, as depicted in figure 1.51. In the copier the reference current is connected far away from the input transistor. The reference current has to flow through the base terminal wiring. A voltage drop V_{error} of only 2mV between the base terminals of Q_1 and Q_2 already results in an error of 10%. The reference current should be supplied via a separate wire.

1.5.3 The MOS current mirror

In the previous sections, the current mirrors discussed were built with bipolar transistors, but they can be implemented with MOS transistors also. The MOS current mirror is depicted in figure 1.52. The transistors must always be in the pinch-off region. The gate-source voltage is higher than the threshold voltage (normally-off device) and the gate-drain voltage is zero.

The behavior of this current mirror is analogous to its bipolar equivalent. Errors due to the

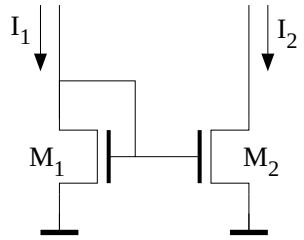

Figure 1.52: The MOS current mirror

mismatch of transistor areas and parameters are mostly larger than for the bipolar equivalent due to the larger spread in parameters. The error due to the channel-length modulation ("Early effect") is generally larger too, because the output impedance of MOS transistors is lower, making cascoding favorable. In contrast with bipolar, the MOS mirror does not suffer from errors due to gate currents.

1.6 Self-biasing sources

Sources which need no additional sources for biasing purposes are called self-biasing sources. The value of the output signal and the biasing currents and voltages are referred to a internal voltage.

1.6.1 A self-biasing MOS current source

A very simple self-biasing source is depicted in figure 1.53. This source uses a normally-on

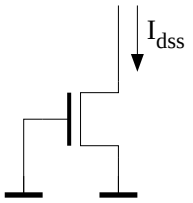

Figure 1.53: A very simple self-biasing current source

MOS transistor. The reference to which the output current is referred is an internal voltage. No additional reference is needed for the biasing. For a drain voltage higher than the threshold voltage, the MOS transistor is in the saturation region. In that region the current is given by:

$$I_d = \frac{\mu C_{\text{ox}}}{2} \frac{W}{L} \left(V_{GS} - V_{TO}\right)^2 . \tag{1.116}$$

For the transistor shown in figure 1.53, the gate-source voltage is zero and consequently the output current is equal to the maximal saturation current:

$$I_{dss} = \frac{\mu C_{\text{ox}}}{2} \frac{W}{L} \left(V_{TO}\right)^2 . \tag{1.117}$$

The MOS transistor suffers from a relatively low output impedance. To reduce the effect of channel-length modulation, a transistor with a relatively long channel needs to be used. To sink a large current the channel needs to be wide too, which results in a rather large MOS transistor.

1.6.2 A self-biasing PTAT current source

When a combination of a linear and a non-linear mirror is used, a self-biasing current source can be obtained also. This is depicted in figure 1.54. The linear mirror forces a linear relation between

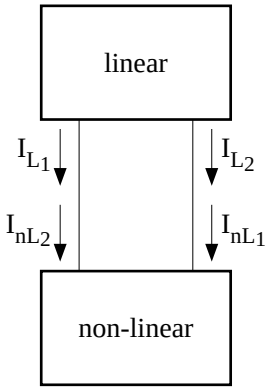

Figure 1.54: A self-biasing source using a linear and a non-linear mirror

the two branch currents and the non-linear mirror a non-linear relation. The stable situation is the one for which both relation are fulfilled. These stable situations are given in figure 1.55 by the intersection points of the two transfer functions of the mirrors. There are two stable solutions: A

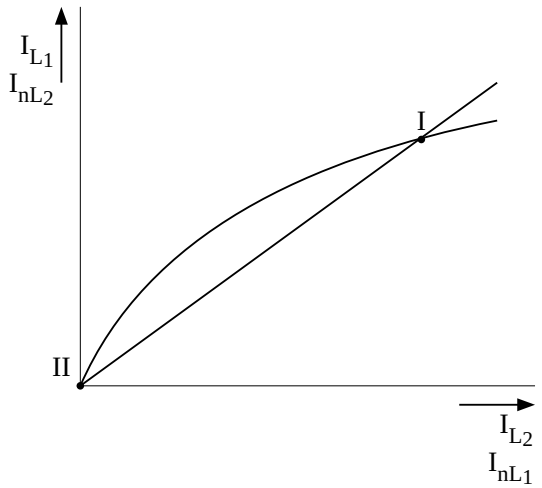

Figure 1.55: The solutions of the self-biasing current source using a linear and a non-linear current mirror

trivial solution in which all the currents are zero, and the desired solution with currents unequal to zero. To force the circuit to the non-zero solution, additional measures have to be taken.

An implementation of this type of source was given in the previous section, the enhanced peaking current source. Another widely used source is the PTAT current source. This source is given in figure 1.56. The source is just the PTAT voltage source discussed in section 1.3.4,

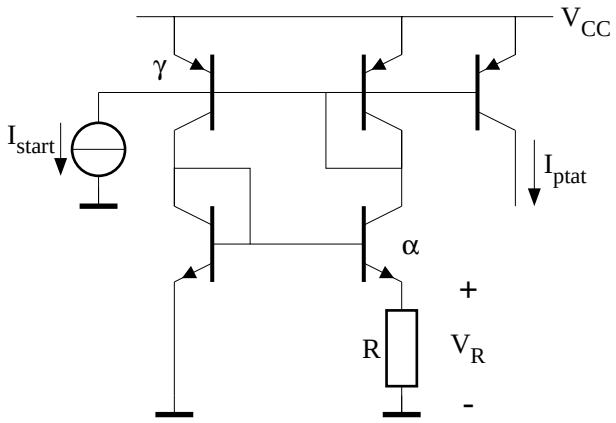

Figure 1.56: The PTAT current source

with the two current sources in figure 1.15 implemented by a current copier. Because the voltage across the resistor R is PTAT, the current through the resistor is PTAT also and this current is copied to the output. The output current is given by:

$$I_{\text{out}} = \frac{kT}{qR} \ln(\gamma\alpha) \tag{1.118}$$

with γ and α the scaling of the upper and lower mirror, respectively. To ensure the non-zero solution a start-up current is required. This current can be very low.

1.6.3 A self-biasing bandgap reference

A small extension to the source discussed in the previous section results in a self-biasing bandgap reference. The circuit is depicted in figure 1.57. Through the resistors R_1 and R_2 flows a PTAT current, I_{PTAT} and $(1+\gamma)I_{\text{PTAT}}$, respectively. The voltage across the two resistors is PTAT also and equals:

$$V_{R_1+R_2} = V_{\text{PTAT}} = I_{\text{PTAT}}R_1 + (1+\gamma)I_{\text{PTAT}}R_2. \tag{1.119}$$

The base-emitter voltage of Q_1 is added to this PTAT voltage. By choosing the appropriate values for the resistors, the PTAT voltage compensates the first-order temperature behavior of the base-emitter voltage. This is just a bandgap reference of the type discussed in section 1.3.5. Although the quality is minor to the quality of the bandgap reference described in previous sections, this bandgap reference is a very simple one. Some errors in this bandgap are due to:

- base currents,
- errors in the mirror factor,
- the Early effect.

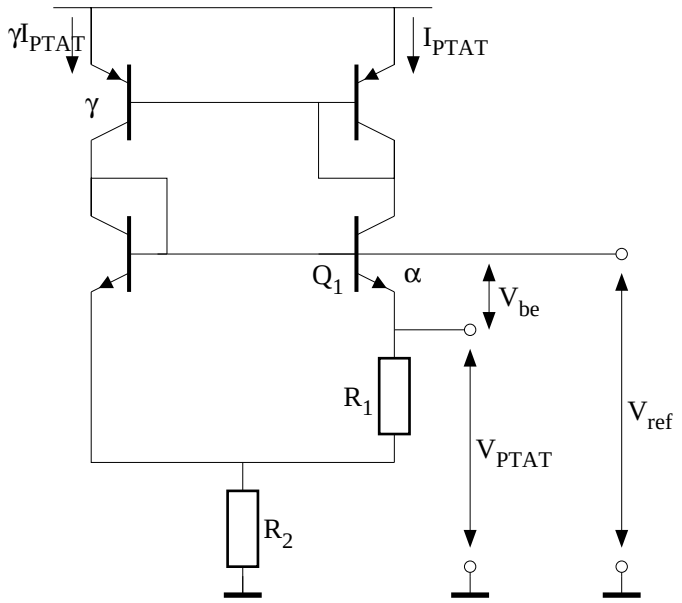

Figure 1.57: A self-biasing bandgap reference

1.7 Reduction of the saturation voltage

The saturation of the transistor as discussed in section 1.3.4, is a desirable effect. For current sources, however, this is a highly disturbing effect. A single-transistor current source is depicted in figure 1.58. When the voltage $V_{\rm out}$ becomes too high the transistor goes into the saturation region. The base-collector junction becomes forward biased and the collector starts injecting charge carriers into the base region, resulting in a reduction of the output current.

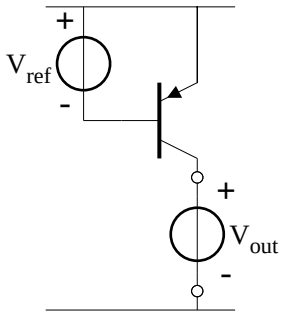

Figure 1.58: A single-transistor current source

Especially in low-voltage design, saturating current sources are a considerable problem. Because only a low supply voltage is available, i.e. 1V, the output voltage of a current source may not go beyond 0.8-0.9V. In such a case, the collector-emitter voltage remains higher than 0.1-0.2V and the source does not saturate. But the available supply voltage is reduced by 10-20%. To allow a larger output voltage swing, a reduction of the saturation voltage is favorable.

In section 1.3.4, an expression for the saturation voltage was given:

$$V_{CE} = \frac{kT}{q} \ln \left(\frac{1 + 1/\beta_r + \beta_{\rm sat}/\beta_r}{1 - \beta_{\rm sat}/\beta_f} \right). \tag{1.120}$$

The saturation voltage can be made small by a high reverse current-gain factor. For instance, the transistor from the example given in section 1.3.4 is changed to have a reverse beta of 6. The saturation voltage with $\beta_{\rm sat} = 20$ becomes:

$$V_{CE_{\rm sat}} = 44.7\text{mV @ 300K}. \tag{1.121}$$

A reduction of 25%. The reverse current-gain factor is the key parameter in reducing the saturation voltage. The reverse current-gain factor is, besides by layout, determined by the doping levels. However, for a given process, the doping levels cannot be changed by the circuit designer.

The influence of the layout is depicted in figure 1.59 for a vertical transistor. In figure 1.59a, a tiny emitter is made in a large base and collector. When this transistor is biased in reverse

Figure 1.59: The influence of the layout on the saturation voltage. a) A transistor with a relatively tiny emitter and b) A transistor with a relatively large emitter

mode the collector works as the reverse emitter. Many carriers injected from the reverse emitter have to travel a relatively large distance to the reverse collector. The carriers injected at point A have to travel a larger distance to the reverse collector than the carriers injected at point B. The chance that a carrier from point A reaches the reverse collector is lower, due to the higher chance of recombination, than the chance that a carrier from point B reaches the reverse collector. The transistor shown in figure 1.59b has a relatively large emitter. Now most carriers injected from the reverse emitter have to travel only a short distance, reducing the total recombination. As the base current is determined by the recombination in the base region, the latter transistor has a higher reverse current-gain factor than the former transistor. Therefore, to obtain a low saturation voltage, the collector and emitter areas have to overlap each other as much as possible.

1.8 Conclusions on current sources

Several implementations of current constants have been treated above. The simplest current source uses a single resistor to derive the current from a voltage source. This source, however, requires a high supply voltage in the case of a high output impedance combined with a high output current. The active current source is able to realize a high output impedance and a high output current with a reasonable supply voltage. This source uses negative feedback. The feedback resistor determines the voltage-to-current conversion. When there is 5V across this resistor, noise performance and output impedance are close to the optimal values for this type of source.

The performance of the current mirror discussed thereafter, is shown to improve when emitter resistors are used: the output impedance increases, the mirror factor is closer to n, and the output noise level and the sensitivity for matching errors in the transistors reduce.

Finally, some self-biasing current sources were discussed. The advantage of this type of source is their simple structure. However, some of these sources may suffer from start-up problems.

Chapter 2

Translinear Circuits

Albert van der Woerd

2.1 Introduction

2.1.1 About the term "translinear"

Early translinear circuits were strictly based on the remarkable fact that the *trans*conductance of a bipolar transistor is *linear*ly proportional to its collector current. This fact is a consequence of the logarithmic relation between I_C and V_{BE}

$$V_{BE} = V_T \ln(I_C/I_S(T)) \tag{2.1}$$

from which it follows

$$\frac{\delta I_C}{\delta V_{BE}} = g_m = \frac{I_C}{V_T} \tag{2.2}$$

This is the key to the strictly translinear principle and, basically, only devices showing a very exact logarithmic relation are suitable. As MOSTs operating in weak inversion show a comparable relation between the gate-source voltage and the drain current, they are suitable too for application of the strictly translinear principle.

Distinction between Translinear Loops (TL) and Translinear Networks (TN)

A general property of a TL circuit is that it contains one or more closed loops of emitter-base junctions (gate-source junctions) with a voltage-current relation according to (2.1). A TN circuit, however, contains no such loops but yet the relations (2.1) and(2.2) are intentionally and profitably used. In practice, configurations are often combinations of TL and TN circuits.

However, over time the term "translinear" has come to refer to a wider class of circuits, for some "translinear" circuits contain MOSTs in strong inversion, whose $V_{GS} - I_D$ relation is quadratic instead of exponential, whereas the other properties (the presence of loops of gate-source junctions and/or the intentional use of the $V_{GS} - I_D$ relations) are maintained.

2.1.2 General classification of translinear circuits within the world of analog circuits

As stated before, all analog circuits where the logarithmic voltage-current relation of individual devices is intentional and is profitably used are called Translinear Networks (TN). However, a special class of circuits, containing one or more closed loops of junctions (TL), needs further consideration.

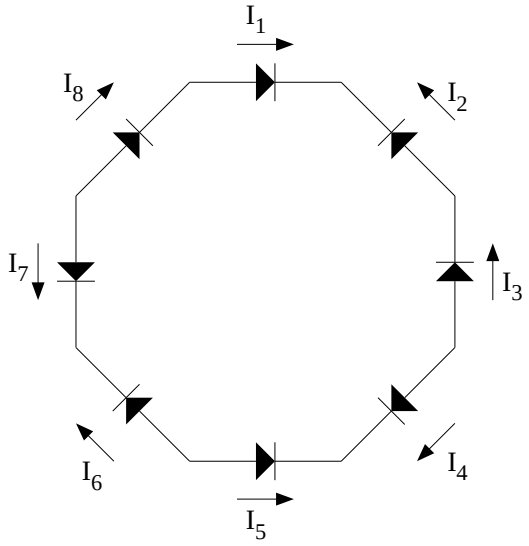

Figure 2.1: Closed loop of junctions

To begin with we consider the closed loop of junctions shown in Fig. 2.1. We assume that all junctions (which can be diodes or the input ports of transistors) are forward-biased with circuitry that is not shown. Other boundary conditions are that the loop must contain an *even number of junctions (at least two)* and that there are an *equal number of junctions clockwise facing and counterclockwise facing* (shorted CW and CCW). If the forward voltage of each junction $(1, 2, 3, ...n)$ in Fig. 2.1 is V_{FK}, it follows

$$\sum_{k=1}^{k=n} V_{FK} = 0 \tag{2.3}$$

If we assume that V_T is device-independent and the collector (drain) current of the device with junction number k is I_k , (2.1) and (2.3) yield

$$\prod_{k=1}^{k=n} \frac{I_k}{I_{sk}} = 1 \tag{2.4}$$

If we distinguish the clockwise and counterclockwise facing junctions (each $n/2$) we can write

$$\prod_{CW} \frac{I_k}{I_{sk}} = \prod_{CCW} \frac{I_k}{I_{sk}} \tag{2.5}$$

Since for bipolar transistors the saturation currents I_{sk} are proportional to the correspondent emitter areas A_k, we can rewrite (2.5) as

$$\prod_{CW} \frac{I_k}{A_k} = \prod_{CCW} \frac{I_k}{A_k} \tag{2.6}$$

or as

$$\prod_{CW} J = \prod_{CCW} J \tag{2.7}$$

where J is the saturation current density of each junction.

Equation (2.7) gives the ultimate translinear principle, in words (Gilbert [1]):
In a closed loop containing an even number of forward biased junctions, arranged so that there are an equal number of clockwise facing and counterclockwise facing polarities, the product of the current densities in the clockwise direction is equal to the product of the current densities in the counterclockwise direction.

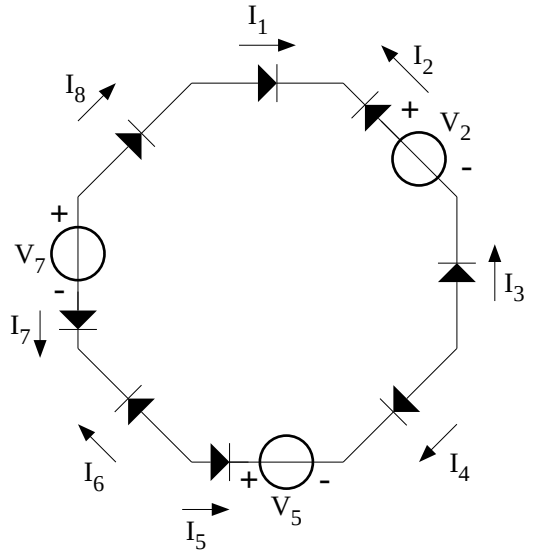

Figure 2.2: Closed loop of junctions and some voltage sources

2.1.3 Extension of TL theory to include dc voltage generators

Fig. 2.2 depicts a modification of the general circuit shown in Fig. 2.1, where some dc voltage sources have been added. If V_L is the net voltage in the loop, the modified form of Eq. (2.3) is

$$\sum_{k=1}^{k=n} V_T \ln \frac{I_k}{I_{sk}} = V_L \tag{2.8}$$

A few practical circuits using TL loops including dc voltage sources will be shown in Section 3.

2.1.4 Application areas of translinear circuits

Linear amplification must be considered to be the most important class of analog signal processing. Though Gilbert introduced in 1968 "a new wide-band amplifier technique" based on the translinear idea, later developments in structured amplifier design have shown that "basic" amplification is surely not the most powerful translinear circuit issue. Because indirect feedback techniques are used in translinear circuits such a design does not have optimal noise, accuracy and linearity qualities [2]. However, if the gain must be *controllable*, the translinear principle can yield great advantages. Further, they have proved to be very powerful for providing a great amount of different *nonlinear* signal processing functions, such as analog multiplying/dividing, rms-dc conversion, vector summation, squaring and square-rooting. A general restriction is that the special features of the translinear principle are only obvious at relatively low frequencies. At high frequencies other principles to provide nonlinear signal processing are often more powerful.

A special class of analog electronics that has attracted much interest during the last few decades is the design of *low-power/low-voltage* circuits. In this class we observe a revival of some types of translinear circuits. This is mainly because the *current-mode* operation of translinear circuits perfectly fits with *low-voltage* operation, whereas *low-power* operation generally implies that the system bandwidth is restricted. (Note, that the low-frequency area is the most powerful operation area of TL circuits).

2.1.5 Suitable semiconductor components

If we only consider circuits operating according to the *strict* translinear principle (Eq. 2.7), we must resort to devices with a perfectly exponential transfer. BJTs fulfill this requirement within a very large collector current range. Fig. 2.3 gives an example of the measured $I_C - V_{BE}$ characteristic of a typical BJT.

Other suitable devices for the strictly translinear principle are MOSTs operating in weak inversion. Fig. 2.4 shows the $I_D - V_{GS}$ characteristic of a typical MOST.

If the strictly translinear principle is no longer maintained, MOSTs operating in moderate/strong inversion are also suitable.

2.2 Design strategies for translinear circuits

2.2.1 The heuristic approach

The term "heuristics" literally means "method of solving problems by inductive reasoning, by evaluating past experience and moving by trial and error to a solution". The first design approaches of most known electronic circuits were done in this way and, consequently, generally only experienced engineers are able to find new solutions by using this approach.

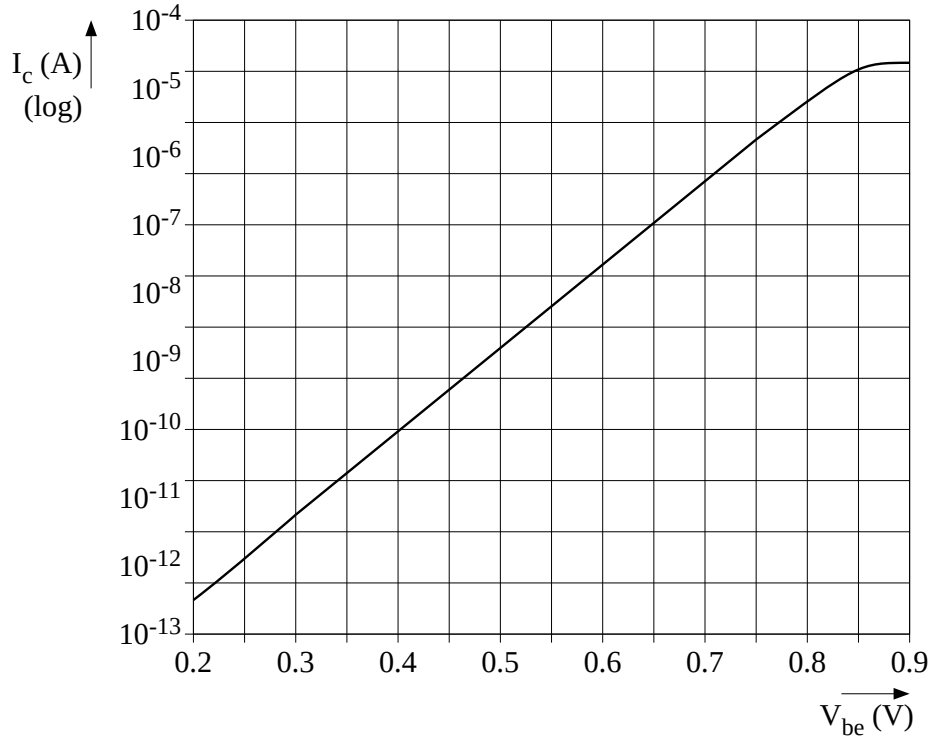

Figure 2.3: Measured $I_C - V_{BE}$ characteristic of a typical BJT

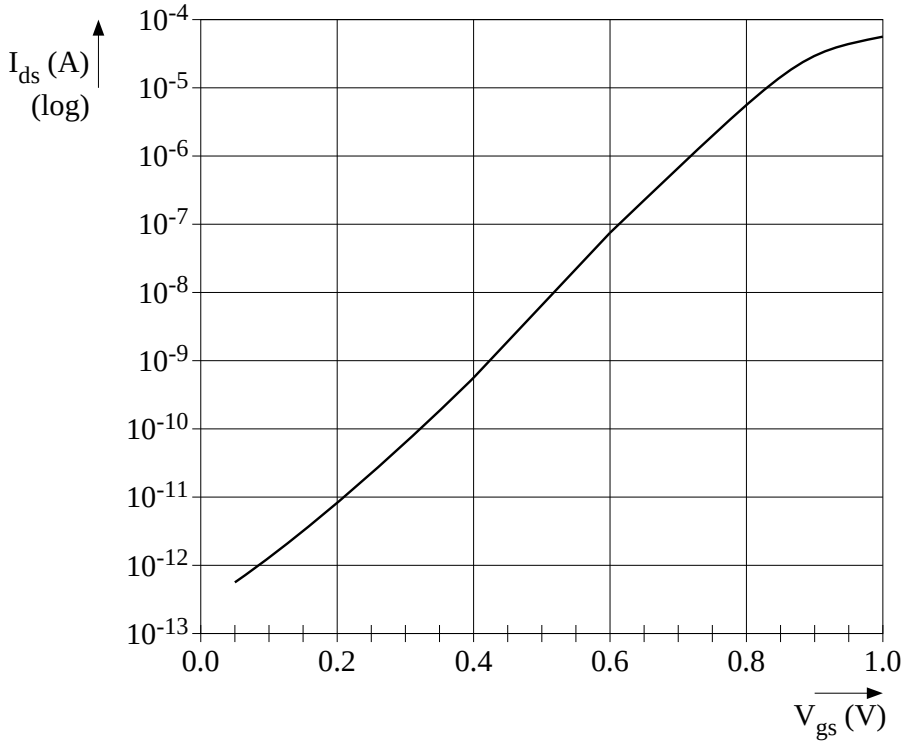

Figure 2.4: $I_D - V_{GS}$ characteristic of a typical MOST in weak inversion

2.2.2 The systematic approach

A systematic design system must contain a set of generally valuable, structured design rules. These rules must be structured in a hierarchical way, so that, from a restricted set of suitable basic configurations, all possible solutions to a preliminary stated problem are generated. The approach has successfully been applied to the design of amplifiers with overall feedback and also to translinear circuits. The advantages of this approach are twofold. First, a well-structured design system can be used by designers without specialized talent or experience. Second, it generally generates more (and sometimes better) solutions to the same problem than would have been found by heuristic designing.

However, systematic design systems have some serious drawbacks too. Generally, the solutions generated by such systems preferably must be selected by an experienced designer, first because not all solutions are practically appreciable and second because some solutions don't work at all. The last phenomenon is because the system generally is not able to process all electrical properties. As an example: in synthesis systems for translinear circuits some resulting circuits may show positive feedback loops (resulting in oscillation or latching) because the system is not able to recognize this item.

2.2.3 Interaction between the heuristic and the systematic approaches

The development of systematic design systems has always been the result or continuation of much work carried out in a heuristic way. They are valuable to generalize and complete the heuristically found solutions. Therefore, the importance of heuristic reasoning should never be depreciated. However, new, systematically found solutions can deliver new impulse and fresh understanding to the heuristically reasoning designer.

2.3 Examples of heuristically found TL configurations

2.3.1 General

This Section deals with the most well-known TL circuits. All of them were initially designed for realization in a bipolar process, and hence some quality parameters are coupled with the influence of finite base currents. To date, the quality standards of these devices are according to the state of the art. However, as soon as comparable circuits are designed with MOSTs in weak inversion, some quality standards will undoubtedly have to be revised. As an example, in Section 2.3.3 the "beta-immune" type-A analog multiplier cell is considered to have better linearity and accuracy than the "beta-sensitive" type B cell. However, with MOSTs operating in weak inversion, which have infinite "betas", this comparison is senseless. As still little is known about the quality aspects of standard TL circuits operating with MOSTs in weak inversion, we resort to bipolar circuits in this Section.

2.3.2 Current mirrors

Note: We only deal with the basic current mirror form here from a translinear viewpoint. Numerous developments of the basic form, with properties suited to special applications, have been made. They are extensively dealt with in Chapter 1 of this book.

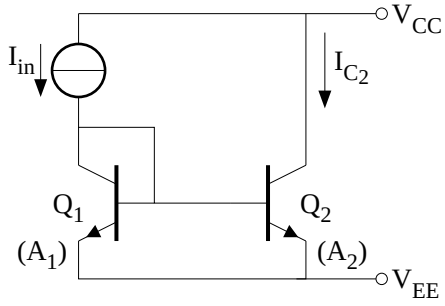

Figure 2.5: Simple current mirror

Fig. 2.5 shows the simplest current mirror. If the general TL equation (2.6) is applied to this circuit we observe that there is one translinear loop with only one CW junction and one CCW junction, yielding

$$\frac{I_{C1}}{A_1} = \frac{I_{C2}}{A_2} \tag{2.9}$$

If the circuit is fed with an input current I_{in} , disregarding the Early effect, and assuming $h_{FE1} = h_{FE2}$, some calculation with (2.9) and the relation of a BJT: $I_C = h_{FE} I_B$ yields

$$I_{C2} = \frac{I_{in}}{\frac{A_1}{A_2}\left(1 + \frac{1}{h_{FE}}\right) + \frac{1}{h_{FE}}} \tag{2.10}$$

Hence, the circuit can be considered to be a dc current amplifier or attenuater with a gain that depends on the value of A_1/A_2 and an error that depends on the influence of the finite value of h_{FE}.

If both transistors are biased with appropriate collector currents (Fig. 2.6), class-A current amplification/attenuation is possible too. In that case I_{C2}, I_{in} and h_{FE} in (2.10) must be replaced by i_{out}, i_{in} and β_{ac}, respectively.

2.3.3 (Controllable) amplifiers and attenuaters; analog multipliers

Note: Because analog multipliers can be used as controllable amplifiers by replacing one of the input signals by a control signal, they are dealt with together.

The "Gilbert Gain Cell"

Fig. 2.7 depicts a circuit that is suitable for controllable current amplifiers. The transistors Q_1 through Q_4 have equal emitter areas and form a translinear loop. Using Eq. (2.6) we have

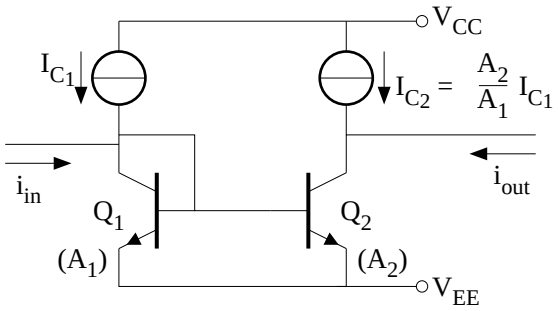

Figure 2.6: Current mirror as a class-A amplifier/attenuater

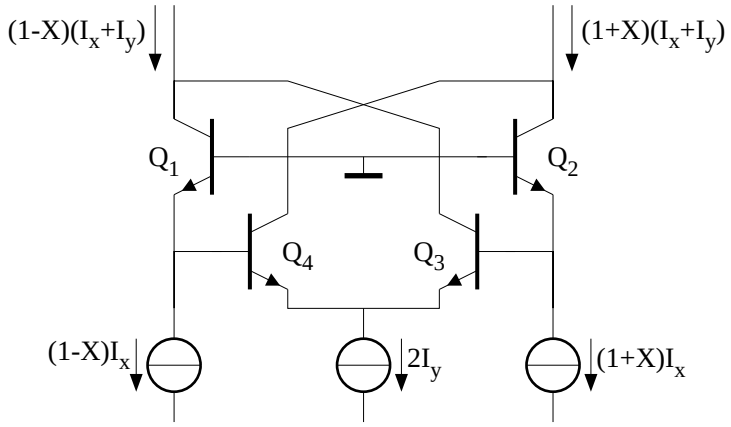

Figure 2.7: The “Gilbert Gain Cell”

$$I_{C1}I_{C4} = I_{C2}I_{C3} \tag{2.11}$$

First the base currents are disregarded. The circuit is symmetrically fed with input currents I_i^+ and I_i^- which are the emitter currents of Q_1 and Q_2. To get suitable expressions for the output currents I_o^+ and I_o^- we introduce a *modulation index*, X, and write

$$I_i^+ = (1+X)I_X \tag{2.12}$$
$$I_i^- = (1-X)I_X \tag{2.13}$$

with $-1 < X < +1$. Combination of (2.11) and (2.13) yields

$$I_o^+ = (1+X)(I_X + I_Y) \tag{2.14}$$
$$I_o^- = (1-X)(I_X + I_Y) \tag{2.15}$$

Example: If I_Y is chosen 9 times I_X, the circuit will show a (differential) current gain of 10.

Note: The above-introduced notation method with one or more modulation indexes will be frequently used in the following.

Errors caused by finite base currents $I_{B,Q3,4}$ is (much) larger than $I_{B,Q1,2}$. These currents are added to the output currents via Q_1 and Q_2, but in anti-phase. Therefore, the error in the output currents due to base currents is considerable and the maximum gain is in practice limited to about 10.

The types A and B translinear cells; two-quadrant multipliers

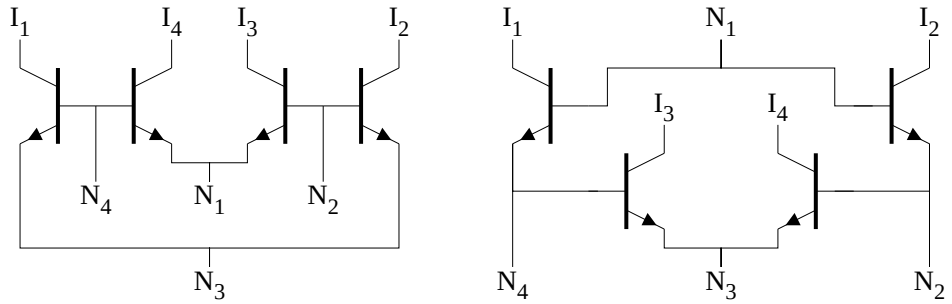

Figure 2.8: Types “A” and “B” TL cells

If four junctions are series-circuited in a closed TL loop there are two possibilities, depicted in Fig 2.8. Left, the junction polarities are **a**lternating and right they are **b**alanced. Therefore, the structures in Fig. 2.8 are referred to as the “A” and “B” cell types. We now take a closer look at both cells.

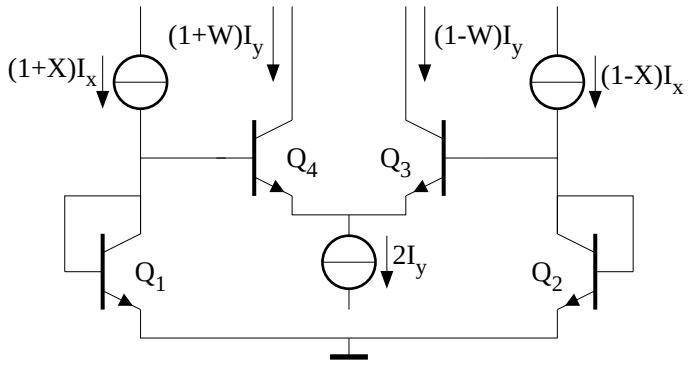

Figure 2.9: The "A" cell with biasing

The "beta-immune" Class-A cell Fig. 2.9 gives the cell, completed with suitable in- and output signals. The translinear condition (Eq. 2.6) yields

$$I_1 I_3 = I_2 I_4 \tag{2.16}$$

or equivalently

$$\frac{I_1}{I_2} = \frac{I_4}{I_3} \tag{2.17}$$

From (2.16) and (2.17) it is immediately apparent that the cell can be used as a one-quadrant analog multiplier or divider by choosing one of the currents to be constant. However, we will show now, that the circuit is also suitable as a two-quadrant multiplier. Therefore, we apply a modulation index to the currents I_1 through I_4, so that

$$(1+W)I_y(1-X)I_x = (1-W)I_y(1+X)I_x \tag{2.18}$$

From (2.18) it is apparent that $W \equiv X$ *for any value of* X *between -1 and +1, irrespective of* β*, transistor geometry and temperature!* This is the reason why this cell is called "beta-immune". If the differential output current is called $I_w = (1+W)I_y - (1-W)I_y$, we obtain

$$I_w = 2XI_y \tag{2.19}$$

Hence, the cell can operate as a two-quadrant multiplier. Since the differential input signal is $2XI_x$, the current gain is just I_y/I_x.

The "beta-allergic" Class B cell Fig. 2.10 shows the basic cell as a two-quadrant multiplier. It is somewhat more affected by finite beta than the Class A cell. To demonstrate this, we introduce a "base current defect factor" δ to represent either $I_B/I_C(= 1/\beta)$ or $I_B/I_E(= 1/(\beta+1))$ [3]. Applying the translinear relation (2.7) to Fig. 2.10 now yields

$$(1+W)I_y\left((1-X)I_x + \delta(1+W)I_y\right) = (1-W)I_y\left((1+X)I_x + \delta(1-W)I_y\right) \tag{2.20}$$

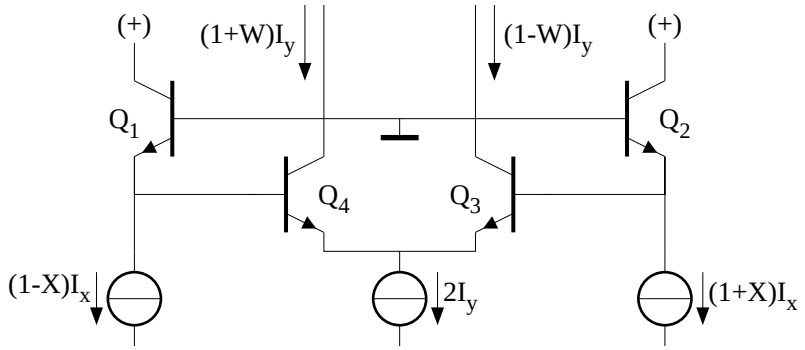

Figure 2.10: The "B" cell with biasing

or

$$W = \frac{X}{1 + \delta \frac{I_y}{I_x}} \tag{2.21}$$

Hence, now the modulation index W is not an exact replica of X, thus resulting in some errors caused by finite betas.

Four-quadrant multipliers

The Class-B cell as a four-quadrant analog multiplier With suitable input signals and summing the collector currents of $Q_{1,4}$ and $Q_{2,3}$ respectively, the Class-B cell can also be used as a four-quadrant multiplier. The circuit with in- and output currents is shown in Fig. 2.11. Applying the translinear relation (2.7) we find

$$I_4 I_1 = I_2 I_3 \tag{2.22}$$

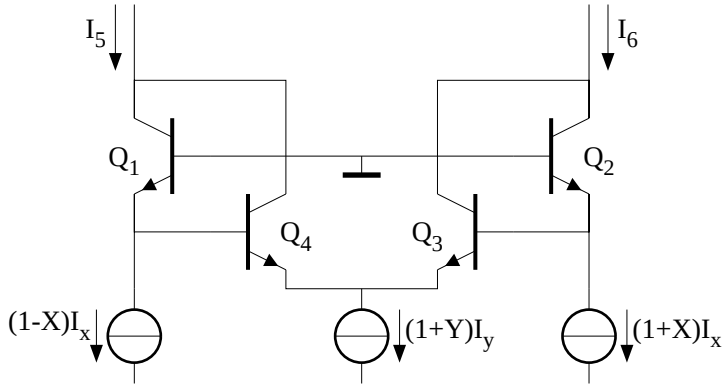

Figure 2.11: The "B" cell as a four-quadrant multiplier

Further it appears from Fig. 2.11

$$I_3 + I_4 = (1+Y)I_Y \tag{2.23}$$

From (2.22) and (2.23) we easily find

$$I_3 = \frac{(1+Y)(1-X)I_Y}{2} \tag{2.24}$$

and

$$I_4 = \frac{(1+Y)(1+X)I_Y}{2} \tag{2.25}$$

which results in

$$I_{out} = I_5 - I_6 = -2XI_X + XYI_Y + XI_Y \tag{2.26}$$

If I_Y is chosen $2I_X$ the final result is

$$Z = \frac{i_{out}}{I_Y} = XY \text{ for } -1 \leq X, Y \leq +1 \text{ (four-quadrant operation)} \tag{2.27}$$

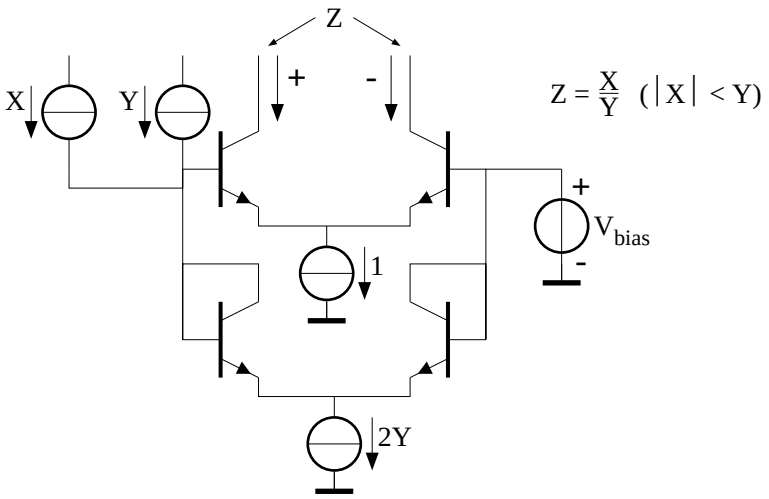

Figure 2.12: Class-"A" cell as an analog divider

Operation as a squarer, as an analog divider or as a square-rooter If X and Y are fed with the same input signal, the cell acts as a squarer. Further, two-quadrant dividing is realized if the functions of one of the input signals (X or Y) and the output signal Z are reversed. Fig. 2.12 shows a possible implementation of a class A cell, where the variables are simply identified with the (normalized) currents. (This circuit was found by employing the systematic design method, outlined in 2.4.2). However, since $|X| < Y$, its dynamic range is restricted. If a translinear multiplier is placed in the feedback loop of a current amplifier with two identical outputs, the dynamic range can be enlarged (Fig. 2.13). Finally, square-rooting is provided if $X = Z$ in Fig. 2.13.

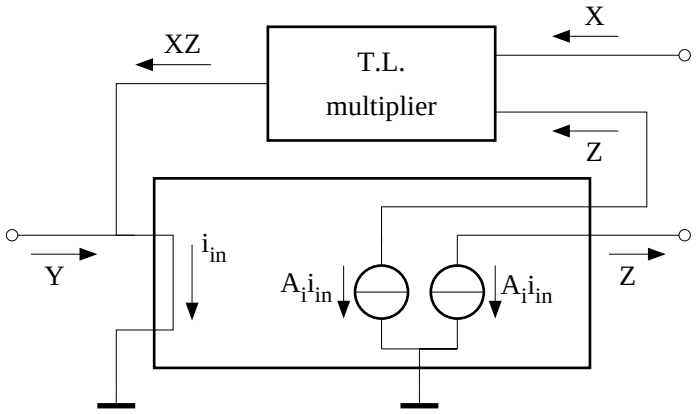

Figure 2.13: High-range analog divider

The "six-pack" translinear four-quadrant multiplier The best-known four-quadrant translinear core (dubbed the "six-pack") is shown in Fig. 2.14. This circuit is completely balanced and contains two overlapping Class-B cells. The reader is invited (in the same way as in Fig. 2.11) to find the expression for $I_{out} = I_7 - I_8$ as a function of X, Y and the biasing currents I_X and I_Y.

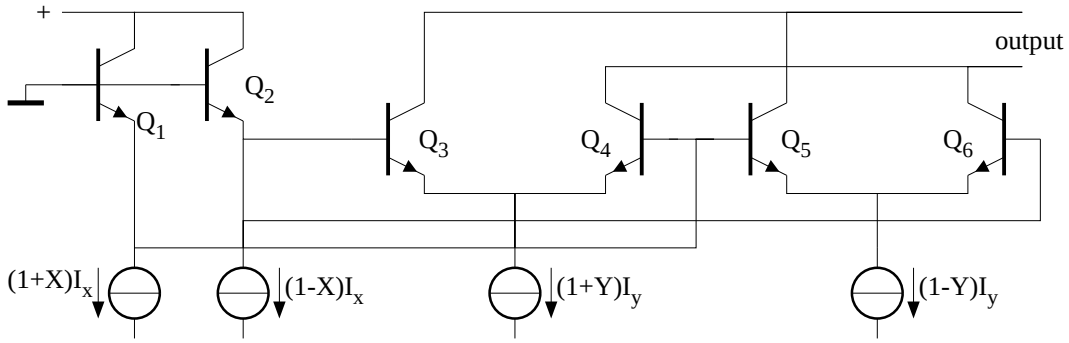

Figure 2.14: The "six-pack" four-quadrant multiplier

2.3.4 The translinear "cross-quad" and its applications

The basic core Though it is not strictly TL (the loop is broken, making it a TN form) it is closely related and has many uses, both by itself and embedded in TL circuits. Fig. 2.15 depicts the generic cell. Say that, in some way, a current I_a is established in $Q_{1,2}$ and I_b in $Q_{3,4}$. The voltage in the open port is

$$V = V_{BE4} + V_{BE1} - V_{BE3} - V_{BE2} \tag{2.28}$$

Hence, if the base currents are disregarded, V is always zero, irrespective of the values of I_a and I_b. In a real circuit V can come quite close to zero. It's easily shown that for $\beta = 100$, I_a is fixed and I_b is swept from $0.1I_a$ to $10I_a$, $V_{\max}$ would be $\pm$ 2.5 mV. Conversely, $V_{\max}$ could be

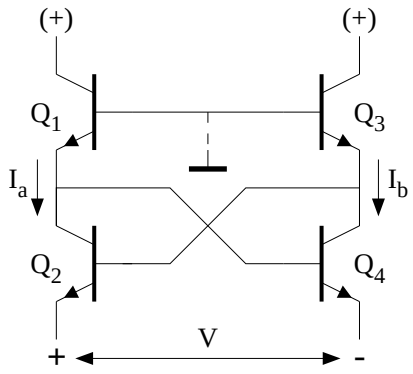

Figure 2.15: The basic TL cross-quad

viewed as the voltage required to establish a 10:1 current ratio in the two transistor pairs. Note that this is much lower than the "60mV per decade", associated with a simple pair of junctions. The input resistance with $I_a = I_b = I$ is found to be

$$R_{in} \approx \frac{4V_T}{\beta I} \tag{2.29}$$

One drawback of the cell is the fact that the radical reduction of the input resistance is obtained by 100% positive feedback, and the circuit is prone to oscillation if not correctly used. Nevertheless, the circuit has many useful applications. Some of them will be included here.

Caprio's Quad

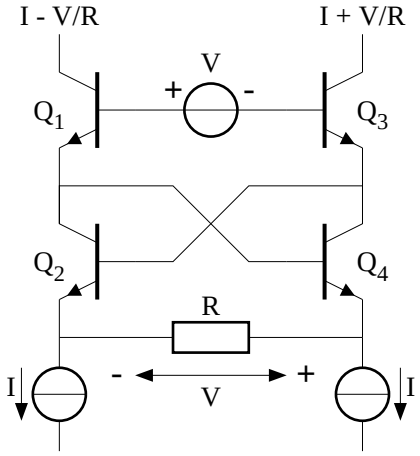

Figure 2.16: Caprio's quad

By applying a voltage source between the bases of Q_1 and Q_3 as shown in Fig. 2.16 (dubbed Caprio's quad [3]), this voltage will be replicated across the resistor R. Hence, owing to the V_BE cancellation, the circuit operates as an accurate and linear transconductance. A major drawback

is that the circuit has a negative input resistance ($-R$) between the bases of Q_1 and Q_3 (the reader is invited to prove this). This can easily lead to instabilities if the source is slightly reactive. Fig. 2.17 shows a special application: a linear half-wave rectifier results, if one of the current sources (I) is chosen to be zero. Fig. 2.18 depicts the simulated transfer $I_C(Q2) = f(V)$.

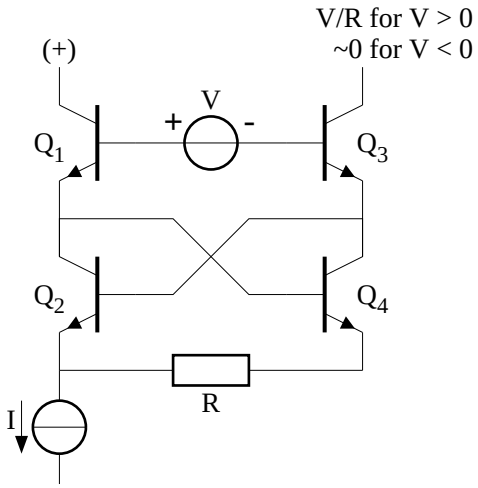

Figure 2.17: Half-wave rectifier derived from Caprio's quad

The translinear cross-quad as a PTAT cell

Most well-known PTAT generators are self-supporting: they produce a PTAT current without external biasing current. Because those cells show a second stable biasing position, where all currents are zero, a starting circuit is generally indispensable. Fig. 2.19 depicts a PTAT cell with a translinear cross-quad. Consideration of the TN path shows that

$$I_{C3} = \frac{V_T}{R} \ln \frac{A_1 A_4}{A_2 A_3} \tag{2.30}$$

Hence, the PTAT current is independent of the input current I, which can be considered as a (non-critical) starting current.

Operation in class-B (AB); applications in power amplifiers

From the translinear relation (2.6) it appears that in each translinear loop the small signal operation is independent of the loop current. Hence, all current relations are maintained, if the input and output signals are directly used as biasing currents, provided that they remain > 0 (class-B operation). This means that all true translinear circuits are basically suitable for class-B operation. The most well-known application is the traditional complementary class-AB power amplifier, shown in Fig. 2.20.

$Q_{3,4}$ are the output (power) transistors and $Q_{1,2}$ are the drivers. The addition of a quiescent current I_Q (dashed), which is always smaller than the peak values of the input current, makes it class-AB operated.

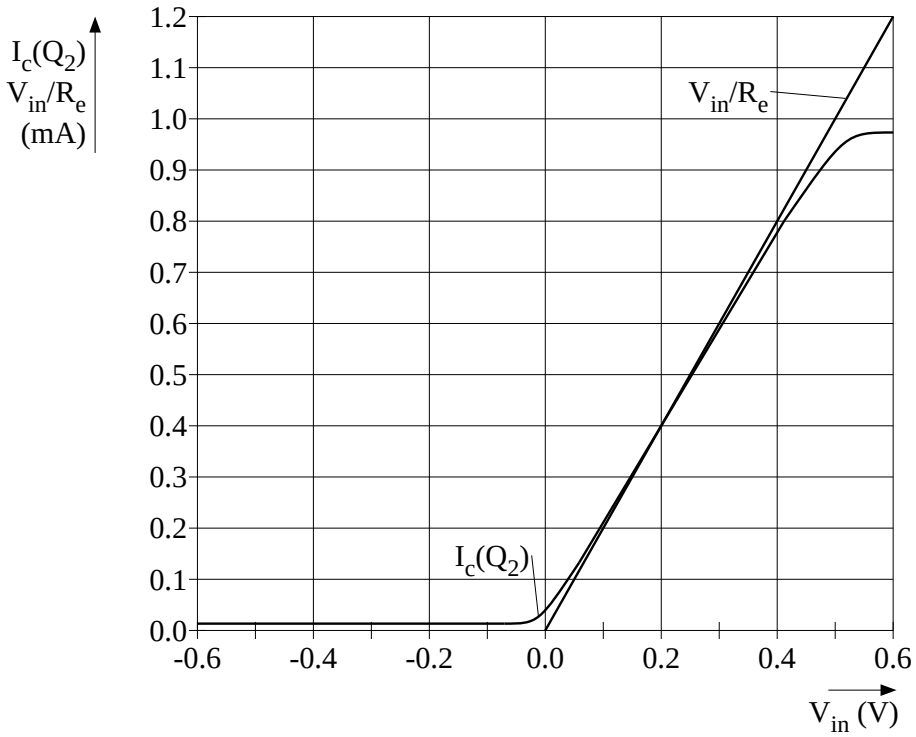

Figure 2.18: Simulated transfer of the half-wave rectifier

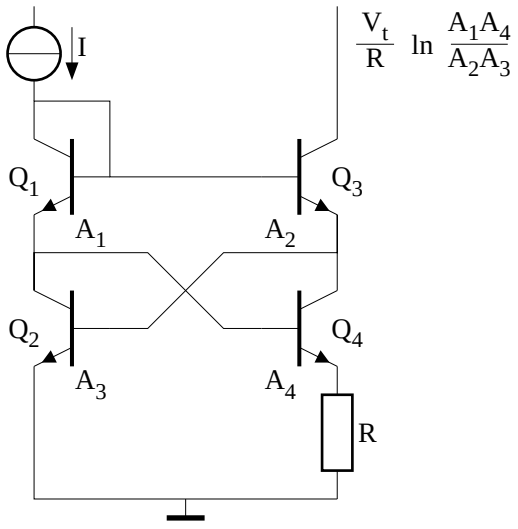

Figure 2.19: PTAT generator with TL cross-quad

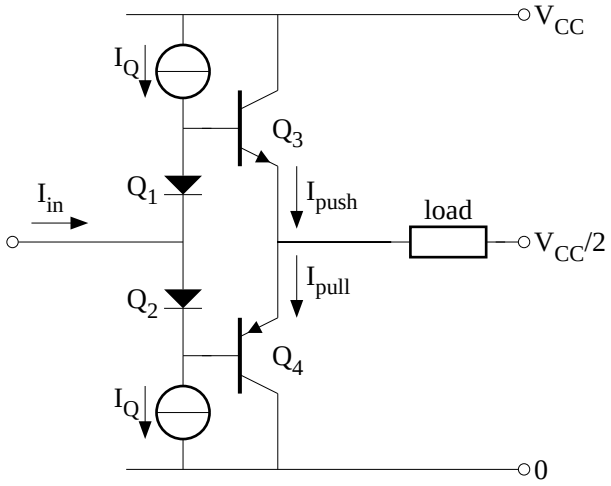

Figure 2.20: Basic class-AB output stage

Applying the translinear law in Q_1 through Q_4 yields

$$I_{\text{push}} I_{\text{pull}} = I_Q^2 \tag{2.31}$$

A convenient way to demonstrate the basic operation is to sketch the currents in Q_3 (I_{push}) and Q_4 (I_{pull}) as a function of the input current (Fig. 2.21).

A major advantage is the fact that neither of the output currents can ever become completely zero, which prevents excessive distortion by switching effects. Many variants of the traditional circuit with special specifications (e.g. for supply voltages below 2 V_{BE}) are found in literature. Some of them are true translinear circuits, others are not.

2.3.5 Miscellaneous translinear circuits

Apart from the translinear circuits described in the foregoing a lot of other special applications of the principle have been developed. These circuits provide special functions such as trigonometric functions, signal normalization, minimum and maximum functions. However, they lie beyond the scope of this chapter and we resort to referring to literature [3].

2.4 Systematic design methods for TL circuits

2.4.1 Introduction

Because TL circuits show common topological properties, they invite a systematic design approach. Seevinck [4] has carried out extensive research into the analysis and synthesis of TL circuits with bipolar transistors of the same polarity. The synthesis method is restricted to TL structures with less than 10 branches and one or two loops. Thus, all possible topologies of TL-circuits with the restrictions mentioned and with a number of prescribed transfer functions can

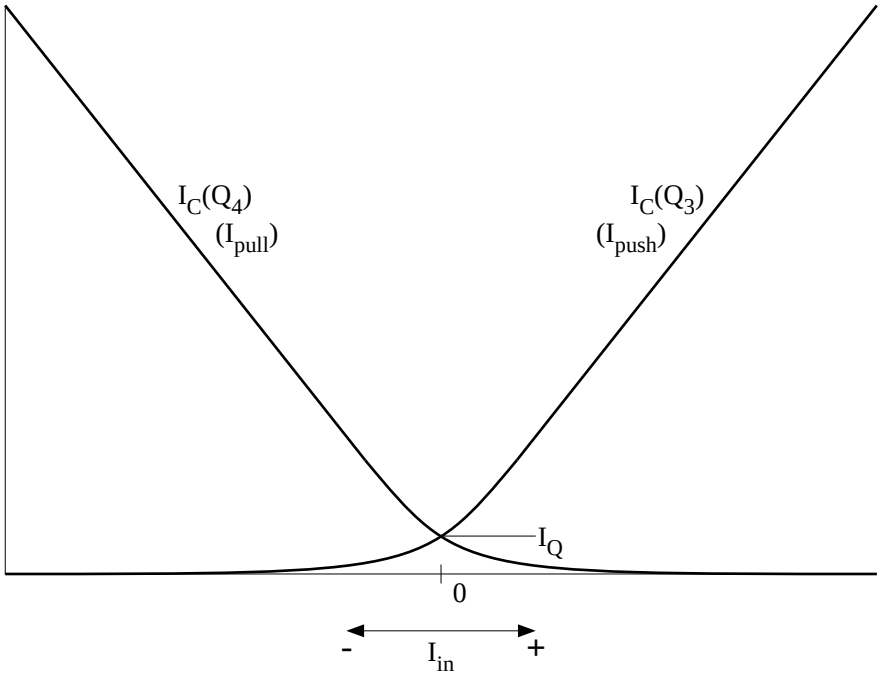

Figure 2.21: $I_{\rm push}$ and $I_{\rm pull}$ as a function of the input current

be synthesized. However, it is surprising that nearly all fruitful and promising topologies found, have earlier been found with heuristic methods. But this is not true in all cases. As the methods are mainly based on network-theoretical and mathematical grounds, an extensive treatment lies beyond the scope of this book. Therefore we confine ourselves to a brief outline in Section 2.4.2 and refer to literature for details [4]. Further, an example of a useful TL circuit obtained by synthesis, that was not found earlier, will be shown.

2.4.2 The Seevinck synthesis method for bipolar semiconductor devices; an example of a systematically found TL circuit

The general aim is the design of TL networks realizing a prescribed (non)linear, time-invariant transfer function. The strategy shows some similarity with traditional synthesis methods for passive networks. The synthesis procedure can be divided into four general steps:

1. Approximation of the prescribed function by suitable algebraic formulations
2. Decomposition of the algebraic formulations found into forms suitable for TL realization
3. Realization of networks, based on topological properties of those TL networks, which fit with the forms found in 2.
4. Selection of the networks found as to their complexity, cost, stability, sensitivity to parameter tolerances, etc.

The parts 1 through 3 will briefly be explained now.

1: function approximation Only *algebraic* functions are suitable, of which rational functions need special attention, because they provide greater precision than polynomials of the same degree. Hence, non-algebraic functions need to be approximated by algebraic functions. As an example, a pretty accurate approximation of a cosine function is given below

$$\cos \pi X \approx \frac{(1-4X^2)(2-X^2)}{2+X^2} \ , \ |x| \leq 1 \tag{2.32}$$

2: function decomposition For synthesis purposes it is convenient to write the TL relation (2.6) in a slightly different form. Say that a TL loop has N elements (branches), numbered from 1 to N with branch currents I_1 through I_N, divided into odd and even ones, and with device areas A_1 through A_N, then (2.6) can be written as

$$\prod_{n=1}^{N/2} I_{2N} = \lambda \prod_{n=1}^{N/2} I_{2n-1} \ , \text{where } \lambda = \prod_{n=1}^{N/2} \frac{A_{2n}}{A_{2n-1}} \tag{2.33}$$

Any TL network has one or more input currents $I_{i1,2,...}$ and output currents $I_{o1,2...}$ Further, every branch currents I_1 through I_N can be expressed in linear combinations of the input and output currents.

Generally, if the expressions of the branch currents into the input and output currents are called f_1 through f_N, application of (2.33) yields

$$f_1(I_{i1,2,...}I_{o1,2,...})f_3(I_{i1,2,...}I_{o1,2,...})... = \lambda f_2(I_{i1,2,...}I_{o1,2,...})f_3(I_{i1,2,...}I_{o1,2,...})... \tag{2.34}$$

Hence, function decomposition means that the prescribed function (approximation) is "translated" into forms according to (2.34).

Note: As all functions f_1 through f_N represent currents in TL elements, they must remain positive for all (positive and negative) values of the input and output currents. This must be checked after decomposition.

Many decomposition techniques are known in mathematics. Suitable techniques for TL synthesis are those using *explicit forms; implicit forms; parametric forms; rational functions; continual fractions, etc.* Generally, each of them is suitable for a class of function approximations. For details we resort to referring to literature [4].

3: network realization techniques An arbitrary TL network always contains one or more (interwoven) TL loops with minimally four branches. If the branch currents and node voltages are left out of consideration and if, besides, every TL element is symbolized by a line, the result is the so-called *undirected graph* of the TL network. Every graph represents a class of TL networks. Of course, the number of branches (= TL elements) is theoretically unlimited. However, due to practical parameter tolerances it has been shown to be senseless to construct TL networks with more than 9 branches and/or more than 2 loops. This limitation results in maximally 6 different graphs. Any graph can more precisely be characterized by numbering its nodes and

choosing the direction of the branch currents. Then every graph has a corresponding *node-branch incidence matrix (the T matrix).* The total number of different T matrices corresponding to the 6 graphs amounts to 26. To date, the connections of the in- and output currents and the values and connections of biasing currents have not yet been chosen. Hence, it will be clear that any T matrix generally results in a great number of possible TL networks. Checking them all would be possible, but this immense job would be entirely a matter of analysis, and give hardly any insight. To make a real synthesis of TL circuits feasible, the possible general function structure of the relations between the branch currents that can be realized by any graph, has to be investigated.

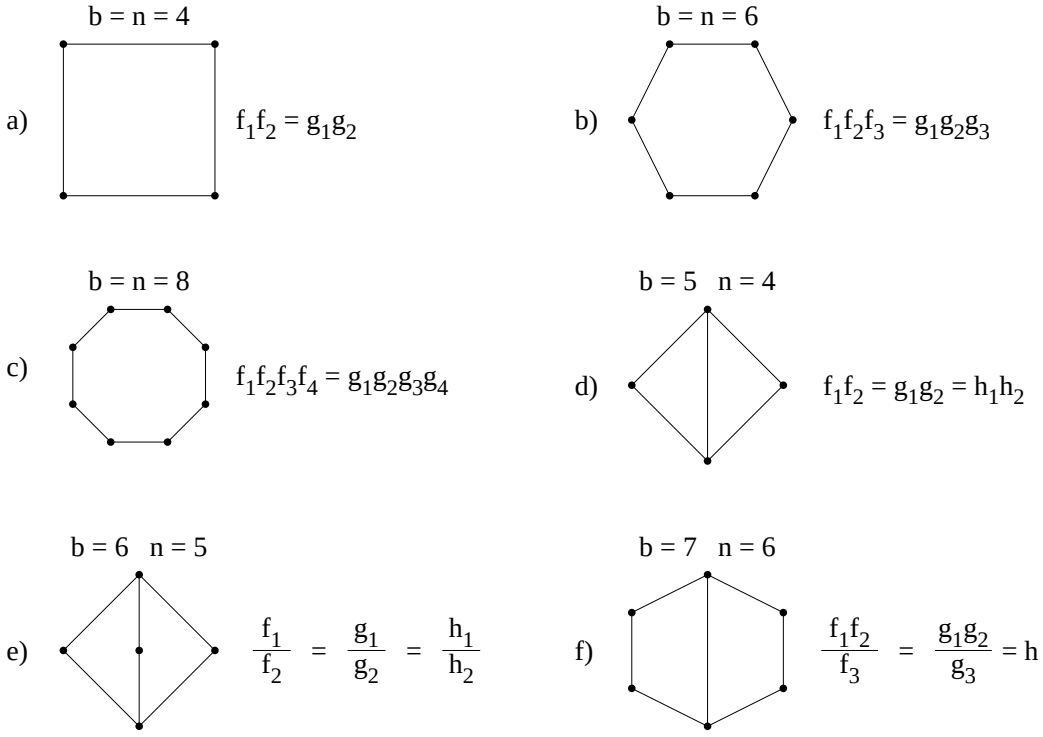

Figure 2.22: The six undirected graphs. b and n are the numbers of branches and nodes

Fig. 2.22 shows the 6 (undirected) graphs with their appropriate general function structures. Now the synthesis procedure is as follows. First, the (approximation of the) desired function is decomposed in one or more ways, so that the results fit with one (or more) of the general function structures shown in Fig. 2.22. Second, all possible T matrices are derived from the (directed) graphs. Third, all possible TL networks are derived from the T matrices. Finally, the resulting networks are checked and selected on feasibility and quality. The complete procedure will be demonstrated with a simple example: Say, a TL two-quadrant divider with transfer $z = x/y$, with $|x| < y$ must be made. The function can be decomposed into

$$z + 1 = \frac{x + y}{y} \text{ or } y(z + 1) = x + y \tag{2.35}$$

or into

$$\frac{1+z}{1-z} = \frac{y+x}{y-x} \text{ or } (1+z)(y-x) = (1-z)(y+x) \tag{2.36}$$

Both functions fit with the general form $f_1 f_2 = g_1 g_2$, where all functions remain positive. From Fig. 2.22 the first graph is selected. After directioning, this graph results in two possible T matrices [4] (see Fig. 2.23).

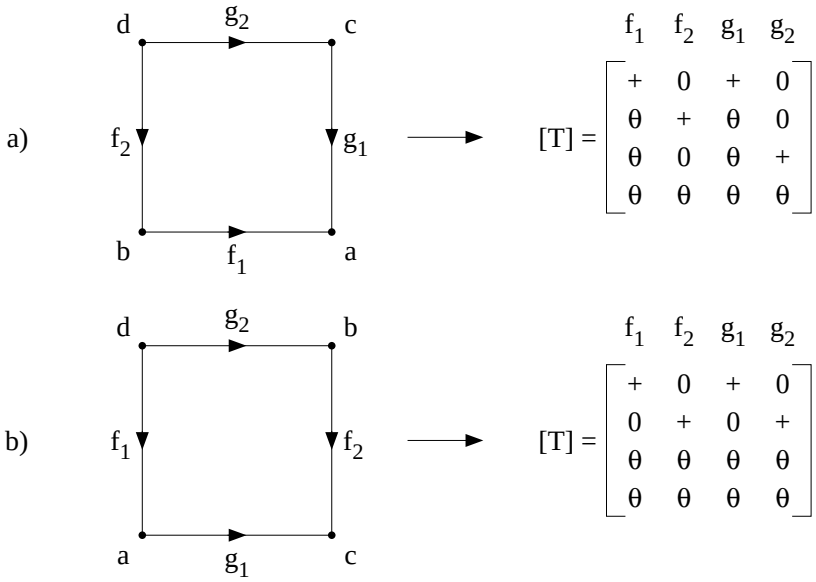

Figure 2.23: The two possible T matrices

According to the decomposed functions (2.35) and (2.36), the two TL networks shown in Fig. 2.24 appear to be feasible. The left one follows from the T matrix of the left part of Fig. 2.23 together with (2.35) whereas the right one follows from the T matrix of the right part of Fig. 2.23 together with (2.36) (Note that the right circuit low-voltage with symmetrical outputs, whereas the left circuit is not).

It will be clear that with all 26 T matrices the realization of numerous different TL networks providing many (approximated) transfers is feasible [4].

2.5 Recent and future developments

Most developments of TL circuits took place from 1968 to, say, 1988. The resulting products were ICs suitable for one or more particular signal processing functions, e.g. four-quadrant multiplying. Much research was carried out to improve their accuracy and other qualities. To date they are/were mainly used as building blocks in electronic systems containing many discrete ICs and other discrete components. Recently a revival of the interest in TL circuits has grown. However, the application areas are different now. First, TL circuits are often used together with other circuits on one chip. This often makes the designs of the available building blocks useless. Some of their characteristics exceed the demands, e.g. accuracy, whereas other characteristics are not

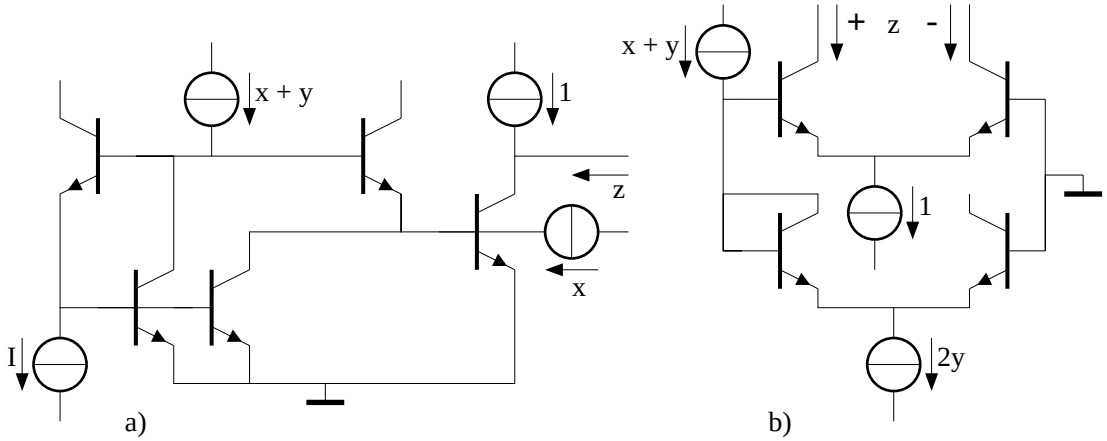

Figure 2.24: Two possible TL-circuits for a two quadrant divider

good enough, i.e. they have too large chip area or they need too much supply voltage/power. Second, TL circuits are recently used for new purposes such as neural networks, which asks for classes of TL circuits with extremely large circuit density and which have entirely different characteristics than the available building blocks. Summarizing, it may be stated that there exists a need for new generations of TL circuits for *(extremely) low-voltage/low-power applications* and with *minimal chip occupation.* Recently a research program, where the possibilities of using the backgate of MOSTs in weak inversion for true translinear circuits are investigated, has been started, i.e. the MOST is considered as a four terminal device, where the backgate is intentionally used as a signal electrode. In the Appendix one of the first results is reported. A brand-new branch of research in translinear circuits concerns their application for dynamic signal processing, e.g. in filters.

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Appendix: Translinear sin(x)-circuit in MOS technology using the back gate

J. Mulder, A.C. van der Woerd, W.A. Serdijn, A.H.M. van Roermund

Abstract

Though the MOS transistor is a four-terminal device, it is most often regarded as being a three-terminal device. Therefore, many possible MOS circuits are overlooked. In this paper, the four-terminal point of view is elaborated with respect to MOS weak inversion translinear circuits. It is shown that, by using the back gate, translinear networks can be derived which cannot be realized with bipolar transistors. These networks increase the possibilities offered by translinear technology. A sin(x)-circuit, which is one of the possible applications of the new network, was measured. The circuit can operate at supply voltages of less than 2 V and with a total bias current of only 14 nA.

I. Introduction

The first translinear circuits, published in '68 by Gilbert [1], were designed using bipolar transistors. However, MOS transistors in weak inversion are also suitable for this type of circuit because of the almost exponential relation between the gate-source voltage and the drain current in this region [2]. In contrast with the bipolar transistor, the MOST is a four-terminal device. In subthreshold, the relation between the bulk-source voltage and the drain current is also exponential. A sufficiently accurate model for the drain current of a MOST in saturation is given by [3]:

$$I_{DS} = I_0 \mathrm{e}^{V_{GS}/\kappa U_T} \mathrm{e}^{V_{BS}/\eta U_T} \tag{2.1}$$

where I_0 is the zero-bias current, V_{GS} and V_{BS} are the gate-source and bulk-source voltage, $U_T = kT/q$ is the thermal voltage and κ and η are the inverses of the subthreshold slopes, which are constant in this model.

A simple way to design a MOS translinear circuit is to translate a bipolar circuit directly to its MOS equivalent, replacing the base-emitter junctions by gate-source voltages and connecting the substrate terminal of each MOS transistor to its source. Using this approach, the functionality of the substrate terminal as a second gate, or back gate, is not recognized and therefore a class of new circuits is ruled out in advance. As shown in this paper, the use of the back gate enables us to design translinear circuits that are not possible when using bipolar transistors. As an example, a sin(x)-circuit is presented. Measurements of a breadboard version of the circuit are shown.

II. Translinear topology

The new translinear circuit topology is depicted in Fig. 2.1. The circuitry necessary to bias the MOSTs at the proper drain currents is not shown. For an NMOS implementation, as shown

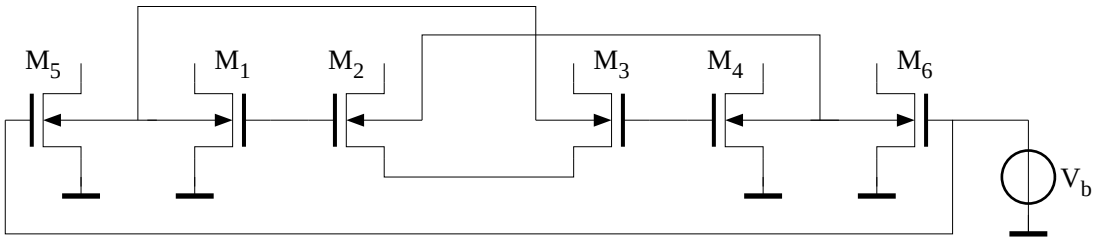

Figure 2.1: Topology described by $\frac{I_1 I_3}{I_2 I_4} = \frac{I_5^2}{I_6^2}$

in Fig. 2.1, a double well process will be necessary. Of course, if the circuit is implemented in PMOS, only n-wells will be needed.

The circuit topology consists of a four-transistor gate-source loop in the up-down topology and two additional MOSTs biased at the same gate voltage. Of course, MOSTs with different back gate voltages have to be integrated in separate wells. Thus, M_1, M_3 and M_5 in the first well, and M_2, M_4 and M_6 in the second well. The back gates of M_1 and M_3 are connected together and the same applies for M_2 and M_4. The back gate voltages of M_1 and M_2 are determined by connecting their back gates to the back gates of M_5 and M_6. These two transistors have to be biased at the same gate voltage to obtain a theoretically process- and temperature-independent transfer function. Using the simple drain current model (2.1), the topology is described by an equation containing two squared currents:

$$\frac{I_1 I_3}{I_2 I_4} = \frac{I_5^2}{I_6^2} \tag{2.2}$$

The two squared currents result from the connection of the back gates of M_1 and M_3 and of M_2 and M_4. Because of this connection, the back gate voltages of M_1 and M_3 and of M_2 and M_4 are added, resulting in two factors 2. These factors 2 are the two exponents on the right-hand side of (2.2).

Equation structure (2.2) is different from the four different equations that can be realized with bipolar translinear networks [4]. Thus, this topology increases the number of possible translinear solutions for the realization of a given function. As this equation structure is more complex than the four mentioned 'bipolar' equation structures, in some cases, a higher functional density and thus area-efficiency can be obtained.

The topology shown in Fig. 2.1 can also be regarded in another way; the circuit consists of two loops of gate-bulk voltages. The first loop is formed by M_1, M_2, M_6 and M_5. The second by M_3, M_4, M_6 and M_5. The sources of M_1, M_4, M_5 and M_6 are connected to ground. The sources of M_2 and M_3 are tied together. Since no gate-source voltages are connected in series, the circuit is suitable for low-voltage applications.

III. Sin(x) circuit

As an example of the use of the new topology, a differential sin(x)-circuit was designed. Since the transfer function of a translinear circuit is always a rational function, an approximation for

the sine function has to be used. According to [5], the sine function can be approximated by:

$$z = \sin \pi x \approx \frac{x - x^3}{1 + x^2} \tag{2.3}$$

where x and z represent the normalized input and output current, respectively. Another way of writing this approximation is the implicit decomposition [4]:

$$\frac{1 + z + x}{1 - z - x} = \frac{(1 + x)^2}{(1 - x)^2} \tag{2.4}$$

This decomposition can easily be fitted on equation structure (2.2) by choosing $I_2 = I_{bias} - I_{out} - I_{in}$, $I_3 = I_{bias} + I_{out} + I_{in}$, $I_5 = I_{bias} + I_{in}$, $I_6 = I_{bias} - I_{in}$ and $I_1 = I_4$. The sine shaped output current is obtained from $I_3 - I_2 - 2I_{in} = 2I_{out}$.

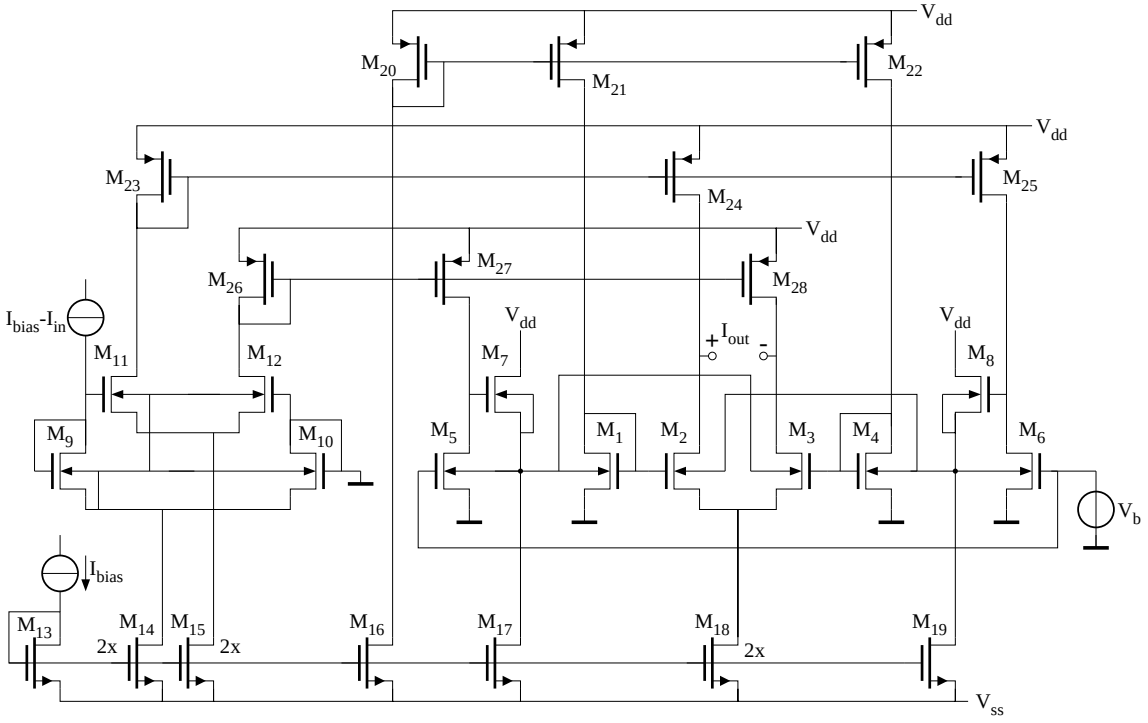

Figure 2.2: Sin(x)-circuit

The complete circuit is depicted in Fig. 2.2. M_7 and M_8 are two simple floating voltage sources, which are used to keep M_5 and M_6 in saturation for bulk voltages of less than about 100 mV. Since the circuit is differential, a gain cell M_9 to M_{12} [1] is used to convert the input signal into a differential signal. Current mirrors are used to supply the currents to the actual sin(x)-circuit.

The applications of the general topology shown in Fig. 2.1 are not restricted to the example treated in this paper. Many other functions will fit on the topology, which in fact is the main strength of translinear technology.

IV. Measurement results

A trivial application of (2.2) is the construction of a $\sqrt{x}$-circuit. To verify the new equation structure (2.2), a breadboard verion of the $\sqrt{x}$-circuit was measured. The drain currents through M_2, M_3, M_4 and M_6, shown in Fig. 2.1, are all biased at 1 nA. The drain currents of M_1 and M_5 are the input and output current, respectively. The gates of M_5 and M_6 are biased at 550 mV. The aspect ratios of the used NMOSTs are 108/7 $\mu\mathrm{m}/\mu\mathrm{m}$.

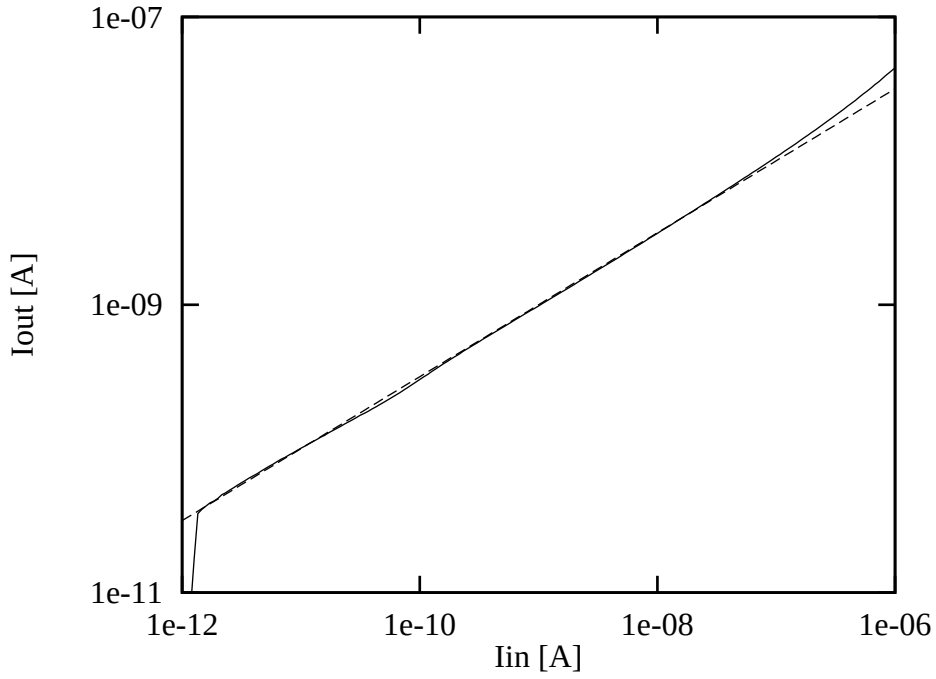

Figure 2.3: Output current of the square root circuit

Measurements were performed using an HP4142B Modular DC Source / Monitor. In Fig. 2.3, the measured output current is compared with the theoretical curve. Clearly, the output current is proportional to the square root of the input current. The large errors at low and high values of the input current are caused by leakage currents of the measurement set-up and by the transition into the moderate inversion region, respectively. The main cause of error for intermediate current values is mismatch; the mismatch was quite large due to the breadboard realization. The average mismatch between the drain currents of two transistors at the same gate-source voltage was about 9%.

Next the sin(x)-circuit, shown in Fig. 2.2, was measured. The measured output current is shown in Fig. 2.4. The gates of M_5 and M_6 are biased at 350 mV. The supply voltages V_{dd} and V_{ss} are $\pm$1V and can even be lower, in principle. The bias current I_{bias} is 1nA, resulting in a total bias current of only 14 nA. The input current I_{in} ranges from 0 to 2 nA. The drains of M_2 and M_3 are loaded by two 500 mV voltage sources. Despite the rather large mismatch, due to the breadboard realization, which causes offset, asymmetry, amplitude, phase and frequency errors, the result is quite reasonable, as is shown by the comparison of the measured output current with

a fitted sine function, see Fig. 2.4.

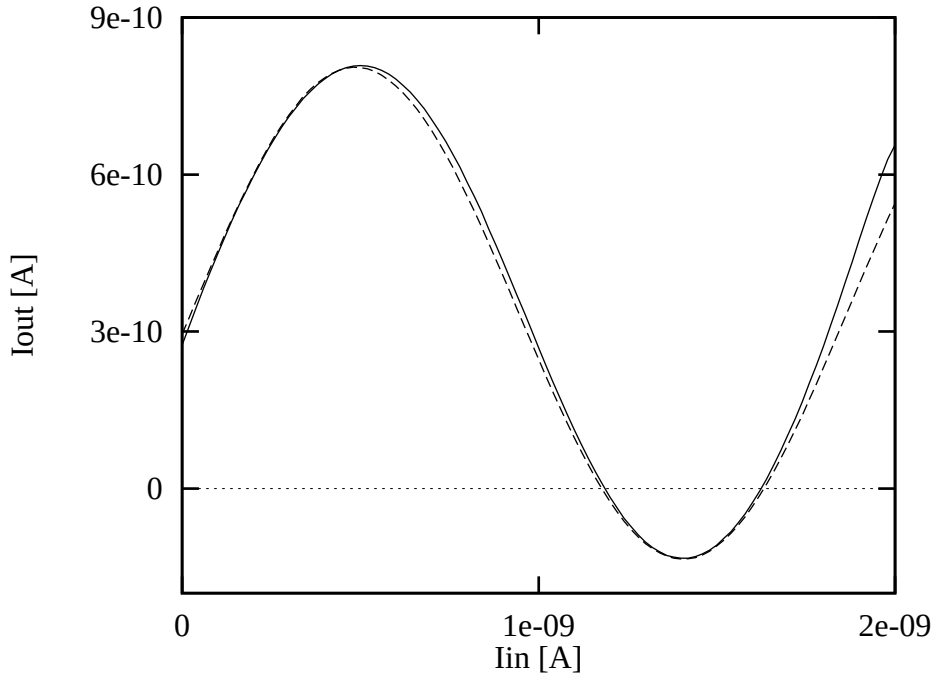

Figure 2.4: Measured output current (—) of the sin(x)-circuit and a fitted sine function (– –)

V. Conclusions

Regarding the MOS transistor as a four-terminal device with a front and a back gate, a new translinear circuit topology was derived. This equation structure increases the number of possible designs for a certain function to be realized in translinear technology, and might result in more area-efficient implementations. As an example of the new topology, a sin(x)-circuit was designed. The circuit operates at supply voltages of less than 2 V, with a total bias current of only 14 nA. Measurements were performed which verify the theory, although they suffer from rather large mismatch of the MOSTs due to the breadboard realization.

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Chapter 3

Dynamic Translinear Circuits

Wouter Serdijn

3.1 Abstract

A promising new approach to shorten the design trajectory of analog integrated circuits without giving up functionality is formed by the class of dynamic translinear circuits. This chapter presents a structured design method for this young, yet rapidly developing, circuit paradigm. As a design example, a 1-V 1.6-μA class-AB translinear sinh integrator for audio filter applications, is presented.

3.2 Introduction

Electronics design can be considered to be the mapping of a set of mathematical functions onto silicon. For discrete-time signal-processing systems, of which the digital signal processors (DSPs) today are by far the most popular, this comes down to the implementation of a number of difference equations, whereas for continuous-time signal-processing systems, often denoted by the term analog, differential equations are the starting points. In mixed analog-digital systems, the analog parts, however, often occupy less than ten percent of the complete, i.e., the mixed analog-digital circuitry, whereas their design trajectory is often substantially longer and therefore more expensive than of their digital counterparts. Where does this discrepancy arise from? This can be partially explained by the fact that, at circuit level, for analog circuits far more components play an important role; various types of transistors, diodes, resistors and capacitors, to mention a few; sometimes also inductors, resonators, and others. Whereas for digital circuits, the complete functionality is covered by transistors only[1].

From the above, it automatically follows that, if we restrict ourselves to the use of as few different types of components as possible, without giving up functionality, we can shorten the analog design trajectory considerably, in the same way as this is done for digital circuits. One successful approach, as we will see in this paper, is given by the class of circuits called *dynamic translinear circuits.*

[1]It must be noted that, for higher frequencies or bit rates, also the interconnects come into play. However, their influence is considered to be equally important for analog as well as digital systems.

Dynamic translinear (DTL) circuits, of which recently an all-encompassing current-mode analysis and synthesis theory has been developed in Delft [1–3], are based on the DTL principle, which can be regarded as a generalization of the well-known 'static' translinear principle, formulated by Gilbert in 1975 [4]. The first DTL circuit was originally introduced by Adams in 1979 [5], being a first-order lowpass filter. Although not recognized then, this was actually the first time a first-order linear differential equation was implemented using translinear (TL) circuit techniques. In 1990, Seevinck introduced a 'companding current-mode integrator' [6] and since then the principle of TL filtering has been extensively studied by Frey [7–16], Punzenberger and Enz [17–31], Toumazou et al. [32–51], Roberts et al. [52–57], Tsividis [58–62], Mulder and Serdijn [63–84] and others [85, 86].

However, the DTL principle is not limited to filters, i.e. linear differential equations. By using the DTL principle, it is possible to implement linear *and* nonlinear differential equations, using transistors and capacitors only. Hence, a high functional density can be obtained, and the absence of large resistors makes them especially interesting for ultra-low-power applications [76].

DTL circuits are inherently companding (the voltage swings are logarithmically related to the currents), which is beneficial with respect to the dynamic range in low-voltage environments [87, 88]. In addition, DTL circuits are easily implemented in class AB, which entails a larger dynamic range and a reduced average current consumption. Further, owing to the small voltage swings, DTL circuits facilitate relatively wide bandwidth operation. At high frequencies though, considerable care has to be taken regarding the influence of parasitic capacitances and resistances, which affect the exponential behavior of the transistor.

DTL circuits are excellently tunable across a wide range of several parameters, such as cut-off frequency, quality factor and gain, which increases their designability and makes them attractive to be used as standard cells or programmable building blocks.

The DTL principle can be applied to the structured design of both linear differential equations, i.e. filters, and non-linear differential equations, e.g., RMS-DC converters [89–91], oscillators [92–103], phaselock loops (PLLs) [80–82] and even chaos. In fact, the DTL principle facilitates a direct mapping of any function, described by differential equations, onto silicon.

Application areas where DTL circuits can be successfully used include audio filters, high-frequency filters, high-frequency oscillators, demodulators, infra-red front-ends and low-voltage ultra-low-power applications.

This paper aims to present a structured design method for DTL circuits. The static and dynamic TL principles are reviewed in Section 2. The general class of DTL circuits contains several different types. In Section 3, the correspondences and differences of log-domain, tanh and sinh circuits are treated. Finally, Section 4 presents the design method, applied to the design of a DTL integrator, starting from a dimensionless differential equation that describes the integrator behavior in the time domain. After four hierarchical design steps, being dimension transformation, the introduction of capacitance currents, TL decomposition and circuit implementation, a complete circuit diagram results. Measurement results of the thus obtained DTL integrator, are presented.

3.3 Design principles

TL circuits can be divided into two major groups: static and dynamic TL circuits. The first group can be applied to realize a wide variety of linear and non-linear static transfer functions. All kinds of frequency-dependent functions can be implemented by circuits of the second group. The underlying principles of static and dynamic TL circuits are reviewed in this section.

3.3.1 Static translinear principle

TL circuits are based on the exponential relation between voltage and current, characteristic for the bipolar transistor and the MOS transistor in the weak inversion region. In the following discussion, bipolar transistors are assumed. The collector current I_C of a bipolar transistor in the active region is given by:

$$I_C = I_S \mathrm{e}^{V_{BE}/V_T}, \tag{3.1}$$

where all symbols have their usual meaning.

The TL principle applies to loops of semiconductor junctions. A TL loop is characterized by an even number of junctions [4]. The number of devices with a clockwise orientation equals the number of counter-clockwise oriented devices. An example of a four-transistor TL loop is shown in Figure 3.1. It is assumed that the transistors are somehow biased at the collector currents I_1 through I_4. When all devices are equivalent and operate at the same temperature, this yields the

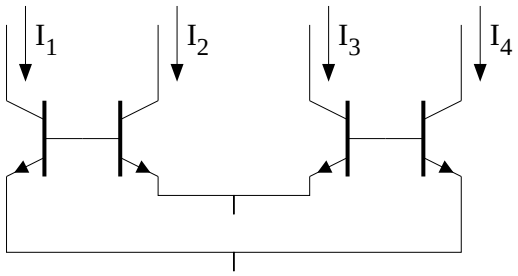

Figure 3.1: A four-transistor translinear loop.

familiar representation of TL loops in terms of products of currents:

$$I_1 I_3 = I_2 I_4. \tag{3.2}$$

This generic TL equation is the basis for a wide variety of static electronic functions, which are theoretically temperature and process independent.

3.3.2 Dynamic translinear principle

The static TL principle is limited to frequency-independent transfer functions. By admitting capacitors in the TL loops, the TL principle can be generalized to include frequency-dependent transfer functions. The term 'Dynamic Translinear' was coined in [89] to describe the resulting

class of circuits. In contrast to other names proposed in literature, such as 'log-domain' [5], 'companding current-mode' [6], 'exponential state-space' [7], this term emphasizes the TL nature of these circuits, which is a distinct advantage with respect to structured analysis and synthesis.

The DTL principle can be explained with reference to the sub-circuit shown in Figure 3.2. Using a current-mode approach, this circuit is described in terms of the collector current I_C and the capacitance $I_{\rm cap}$ flowing through the capacitance C. Note that the dc voltage source $V_{\rm const}$ does not affect $I_{\rm cap}$. An expression for $I_{\rm cap}$ can be derived from the time derivative of (3.1) [6,89]:

$$I_{\rm cap} = CV_T \frac{\dot{I}_C}{I_C}, \tag{3.3}$$

where the dot represents differentiation with respect to time.

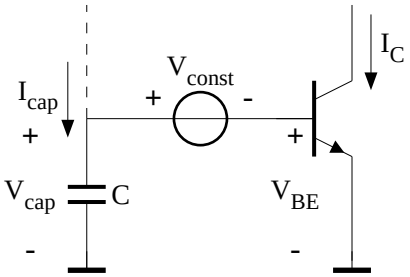

Figure 3.2: Principle of dynamic translinear circuits.

Equation (3.3) shows that $I_{\rm cap}$ is a non-linear function of I_C and its time derivative $\dot{I}_C$. More insight in (3.3) is obtained by slightly rewriting it:

$$CV_T \dot{I}_C = I_{\rm cap} I_C. \tag{3.4}$$

This equation directly states the DTL principle: *A time derivative of a current can be mapped onto a product of currents*. At this point, the conventional TL principle comes into play, since the product of currents on the right-hand side (RHS) of (3.4) can be realized very elegantly by means of this principle. Thus, the implementation of (part of) a differential equation (DE) becomes equivalent to the implementation of a product of currents.

The DTL principle can be used to implement a wide variety of DEs, describing signal processing functions. For example, filters are described by linear DEs. Examples of non-linear DEs are harmonic and chaotic oscillators, PLLs and RMS-DC converters.

3.4 Classes of dynamic translinear circuits

In all DTL circuits, the voltages are logarithmically related to the currents. Therefore, these circuits are in some way instantaneous companding. Figure 3.3 shows the general block schematic of an instantaneous companding integrator [6]. In DTL circuits, the internal integrator is a linear capacitance. The expander E expands the output voltage of this integrator into a current, exploiting the exponential V-I transistor transfer function. Several types of DTL circuits can be

distinguished within the general class of DTL circuits based on the particular implementation of E. Next to the most prevalent class of log-domain circuits, the two classes of tanh and sinh circuits have been proposed by Frey [12]. In this section, we describe their characteristics, which can be derived from the generic output structures, depicted in Figure 3.4.

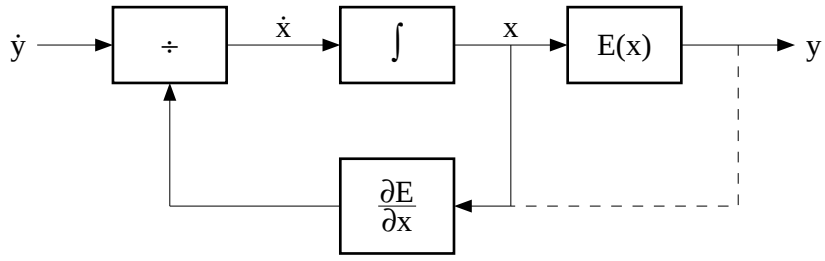

Figure 3.3: General block schematic of an instantaneous companding integrator.

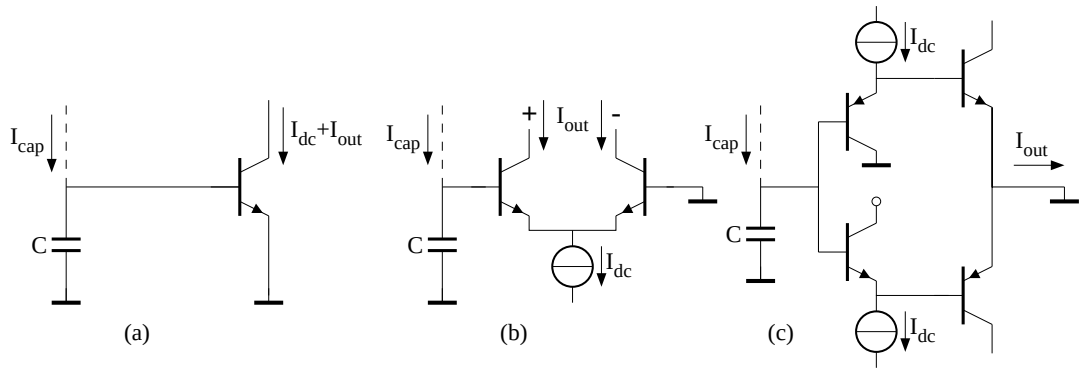

Figure 3.4: Generic output structures of (a) log-domain, (b) tanh, and (c) sinh circuits.

3.4.1 log-domain circuits

Most published DTL circuits are based on the common-emitter (CE) output stage shown in Figure 3.4(a), characteristic for the class of log-domain circuits. The transfer function from the capacitance voltage V_{cap} to the output current I_{out} is given by the well-known exponential law (3.1). In other words, E equals $\exp x$. The companding characteristics of a DTL circuit can be derived from the second order derivative of E with respect to x, denoted by E''. Without loss of generality, $x = 0$ is considered to be the quiescent point of the integrator shown in Figure 3.3. Figure 3.5 displays E'' for the output stages shown in Figure 3.4. Applying a strict definition of companding, E'' should be strictly positive for $x > 0$ and strictly negative for $x < 0$. For log-domain circuits, a comparison of $E'' = \exp x$ with the strict definition of companding reveals that these circuits are indeed companding for $x > 0$; however, for $x < 0$ the exponential function constitutes a compression instead of an expansion. For a symmetrical output current, the overall behaviour of the CE output stage implies a compression rather than an expansion of the peak-to-peak signal swings [86].

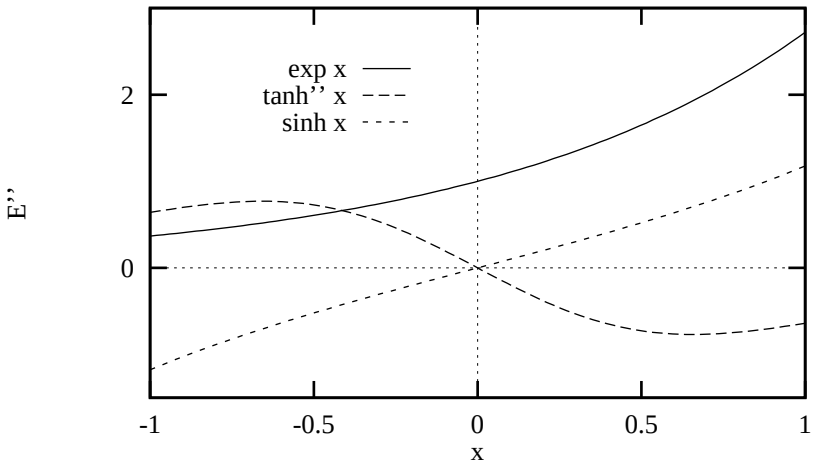

Figure 3.5: The second-order derivatives of the V-I transfer functions of the output stages shown in Figure 3.4.

From a current-mode point of view, the most important characteristic of a DTL output structure is the current-mode expression for the capacitance current $I_{\rm cap}$. For $\log$-domain filters, $I_{\rm cap}$ is given by Equation (3.3), where $I_C = I_{\rm dc} + I_{\rm out}$. As shown in Section 2, a linear derivative $\dot{I}_{\rm out}$ is obtained by multiplying $I_{\rm cap}$ by $I_{\rm dc} + I_{\rm out}$.

A favorable property of $\log$-domain circuits is that a linear damping term can be implemented by the connection of a dc current source I_o in parallel to a capacitance. This can be explained from Equation (3.4). If instead of $I_{\rm cap}$, $I_{\rm cap} + I_o$ is multiplied by $I_{\rm dc} + I_{\rm out}$, an additional term $I_o \cdot (I_{\rm dc} + I_{\rm out})$ is generated. The first term $I_o I_{\rm dc}$ represents a dc offset current. The second term $I_o I_{\rm out}$ results in a finite negative pole.

Typically, $\log$-domain circuits operate in class A. The actual ac signal $I_{\rm out}$ is superposed on a dc bias current $I_{\rm dc}$. As a consequence, the output signal swing is limited to $I_{\rm out} > -I_{\rm dc}$. Note that this limitation is single sided, which is advantageous if a-symmetrical input wave-forms have to be processed. This characteristic can be exploited to enable class AB operation [6, 9]. Using a class AB set-up, see Figure 3.6, the dynamic range can be enlarged without increasing the quiescent power consumption. Using a current splitter, the input current $I_{\rm in}$ is divided into two currents $I_{\rm in1}$ and $I_{\rm in2}$, which are both strictly positive, and related to $I_{\rm in}$ by: $I_{\rm in} = I_{\rm in1} - I_{\rm in2}$. The current splitter impresses a constant geometric or harmonic mean on $I_{\rm in1}$ and $I_{\rm in2}$. Next, $I_{\rm in1}$ and $I_{\rm in2}$ can be processed by two class A $\log$-domain circuits. It is important to note that class AB operated $\log$-domain circuits do satisfy the strict definition of companding due to the fact that only positive currents are processed, i.e., x is never negative.

3.4.2 $\tanh$ circuits

Instead of a single transistor in CE configuration, the class of $\tanh$ circuits is characterized by a differential pair output structure [12], see Figure 3.4(b). The name of this class of circuits is derived from the well-known hyperbolic tangent V-I transfer function. The second-order

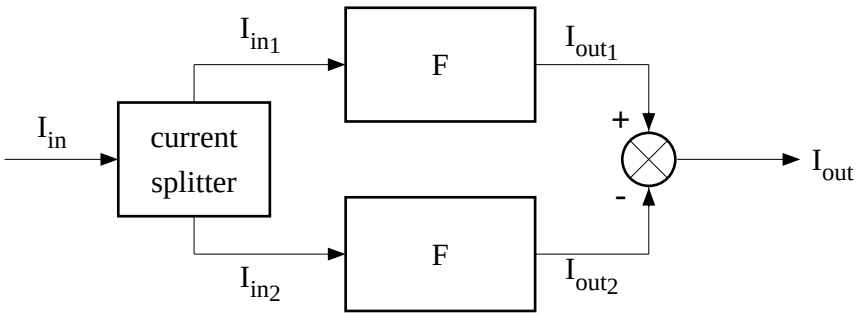

Figure 3.6: Set-up for class AB operation.

derivative E'' is shown in Figure 3.5 and demonstrates that $\tanh$ circuits are not companding at all [48]. The differential pair implements a *compression* function.

The tail current of the differential pair is a dc current $I_{\rm dc}$, and therefore, $\tanh$ circuits also operate in class A. The output current $I_{\rm out}$ is the difference of the two collector currents. The output swing is limited to $-I_{\rm dc} < I_{\rm out} < I_{\rm dc}$. Since this interval is symmetrical, the class AB set-up shown in Figure 3.6 cannot be applied to $\tanh$ circuits.

From Figure 3.4(b), the capacitance current $I_{\rm cap}$ is found to be:

$$I_{\rm cap} = CV_T \left(\frac{\dot{I}_{\rm out}}{I_{\rm dc} + I_{\rm out}} - \frac{-\dot{I}_{\rm out}}{I_{\rm dc} - I_{\rm out}} \right). \tag{3.5}$$

A linear derivative $\dot{I}_{\rm out}$ is obtained by multiplying this equation by $(I_{\rm dc} + I_{\rm out})(I_{\rm dc} - I_{\rm out})$:

$$2CV_T I_{\rm dc} \dot{I}_{\rm out} = I_{\rm cap}(I_{\rm dc} + I_{\rm out})(I_{\rm dc} - I_{\rm out}). \tag{3.6}$$

Comparing Equations (3.4) and (3.6), we can see that the RHS of (3.6) is third-order, whereas the RHS of (3.4) is only second-order. Consequently, in general, TL loops of a higher order are required to implement a $\tanh$ circuit, resulting in a more complex circuit. In addition, a linear loss cannot be implemented by a dc current source connected in parallel to a capacitance. This leads us to the conclusion that $\tanh$ circuits do not seem to have any advantages over $\log$-domain circuits.

3.4.3 $\sinh$ circuits

The third class of DTL circuits proposed in literature is formed by the $\sinh$ circuits [12]. The output structure, shown in Figure 3.4(c), is a complete second-order TL loop. It implements the geometric mean function $I_{\rm dc}^2 = I_{\rm out1} I_{\rm out2}$. The actual output current $I_{\rm out}$ is the difference of $I_{\rm out1}$ and $I_{\rm out2}$. Since both $I_{\rm out1}$ and $I_{\rm out2}$ are always positive, the $\sinh$ output structure operates in class AB, which is beneficial with respect to the dynamic range. The V-I transfer function of the output structure is a hyperbolic sine function. Figure 3.5 displays $E'' = \sinh x$ and shows that the $\sinh$ output stage implements a genuine expansion function.

The current-mode expression for the capacitance current $I_{\rm cap}$ is given by:

$$\begin{aligned} I_{\rm cap} &= CV_T\frac{\dot{I}_{\rm out_1}}{I_{\rm out_1}}, && (3.7)\\ &= -CV_T\frac{\dot{I}_{\rm out_2}}{I_{\rm out_2}}, && (3.8)\\ &= CV_T\frac{\dot{I}_{\rm out}}{\sqrt{4I_{\rm dc}^2+I_{\rm out}^2}}, && (3.9)\\ &= CV_T\frac{\dot{I}_{\rm out}}{I_{\rm out_1}+I_{\rm out_2}}. && (3.10) \end{aligned}$$

A linear derivative $\dot{I}_{\rm out}$ is obtained by multiplying $I_{\rm cap}$ by the sum $I_{\rm out1}+I_{\rm out2}$. It is interesting to note that the voltage $V_{\rm cap}$ and the current $I_{\rm out1}+I_{\rm out2}$ are related through a hyperbolic cosine function; the first-order derivative of E with respect to x.

3.5 Structured design of a class-AB dynamic translinear integrator

Synthesis of a dynamic circuit, be it linear or non-linear, starts with a DE or with a set of DEs describing its function. Often, it is more convenient to use a state-space description, which is mathematically equivalent. The structured synthesis method for DTL circuits is illustrated here by the design of a first-order integrator, described in the time domain by:

$$\frac{dy}{d\tau}-x=0 \tag{3.11}$$

This equation describes the integrator output signal y as a function of the input signal x. τ is the dimensionless time of the integrator.

3.5.1 Transformations

In the pure mathematical domain, equations are dimensionless. However, as soon as we enter the electronics domain to find an implementation of the equation, we are bound to quantities having dimensions. In the case of TL circuits, all time-varying signals in the DEs, i.e., the input signals, the output signals and the tunable parameters, have to be transformed into currents. For the above expression, x and y can be transformed into the currents $I_{\rm in}=x\cdot I_o$ and $I_{\rm out}=y\cdot I_o$, I_o being the DC bias current that determines the absolute current swings.

Subsequently, the dimensionless time τ, can be transformed into the time t with its usual dimension $[s]$, using the equivalence relation given by:

$$d/d\tau = CV_T/I_o\cdot d/dt. \tag{3.12}$$

From this expression it can be deduced that the integrator will be linearly frequency tunable by means of control current I_o.

Applying the mentioned transformations, the resulting differential equation becomes:

$$CV_T\dot{I}_{\rm out} - I_o I_{\rm in} = 0 \tag{3.13}$$

3.5.2 Definition of the capacitance current

Conventional TL circuits are described by multivariable polynomials, in which all variables are currents. The gap between these current-mode polynomials and the DEs can be bridged by the introduction of capacitance currents, since the DTL principle states that a derivative can be replaced by a product of currents.

The capacitance currents can be introduced simply by defining them. To this end, several equivalent expressions for the capacitance current $I_{\rm cap}$ associated with the generic output stage of (class-AB) sinh circuits, depicted in Figure 3.4(c), can were obtained in Section 3. These equations all have two important characteristics in common. First, the denominators on the RHS are collector currents. This implies that these currents have to be strictly positive. Second, the numerators on the RHS are the time derivatives of the denominators.

With these characteristics in mind, we can define the capacitance current for the sinh integrator. As the capacitance current will be used to eliminate the derivative from the DE, in the definition of this current, the derivative present in the DE has to be used. Using (3.10), the differential equation transforms into:

$$I_{\rm cap}\left(I_{\rm out_1} + I_{\rm out_2}\right) = I_{\rm o} I_{\rm in}. \tag{3.14}$$

The current $I_{\rm cap}$ to be supplied to the capacitance C is thus given by:

$$I_{\rm cap} = \frac{I_{\rm o} I_{\rm in}}{I_{\rm out_1} + I_{\rm out_2}}. \tag{3.15}$$

From this point on, the synthesis theory for static TL circuits can be used [104], since both sides of the above DEs are now described by current-mode multivariable polynomials.

3.5.3 Translinear decomposition

The next synthesis step is translinear decomposition. That is, the current-mode polynomial has to be mapped onto one or more TL loop equations that are characterized by the general equation:

$$\prod_{\rm CW} J_{C,i} = \prod_{\rm CCW} J_{C,i} \tag{3.16}$$

$J_{C,i}$ being the transistor collector current densities in clockwise (CW) or counter-clockwise (CCW) direction.

A two-quadrant multiplier/divider is required to implement the Right-Hand Side (RHS) of Equation (3.15). Since a class-AB implementation is pursued, this two-quadrant multiplier/divider

has to be realized by two one-quadrant multiplier/dividers. This is realized by splitting the input current into two strictly positive signals I_{in_1} and I_{in_2}, the difference of which equals I_{in}. Rewriting Equation (3.15) yields:

$$I_{\mathrm{cap}} = \frac{I_{\mathrm{o}} I_{\mathrm{in}_1}}{I_{\mathrm{out}_1} + I_{\mathrm{out}_2}} - \frac{I_{\mathrm{o}} I_{\mathrm{in}_2}}{I_{\mathrm{out}_1} + I_{\mathrm{out}_2}}. \tag{3.17}$$

Equation (3.17) is the basis for the block schematic of the $\sinh$ integrator depicted in Figure 3.7. At the input, a current splitter generates I_{in_1} and I_{in_2} from I_{in}. Subsequently, the currents I_{in_1} and I_{in_2} are divided by $I_{\mathrm{out}_1} + I_{\mathrm{out}_2}$ in two separate circuits. The current $I_{\mathrm{out}_1} + I_{\mathrm{out}_2}$ is obtained from the $\sinh$ output stage. The output currents of the two multiplier/dividers are denoted by I_{cap1} and I_{cap2} and are respectively equal to the first and the second term on the RHS of Equation (3.17). Hence, the current supplied to the capacitance equals $I_{\mathrm{cap1}} - I_{\mathrm{cap2}}$. The use of a single capacitor is an advantage over the class-AB integrator proposed in [6] as it eliminates the necessity of matched capacitors. Finally, the capacitance voltage V_{cap} is applied to the $\sinh$ output stage via a voltage buffer to prevent interaction between the capacitance and the output stage.

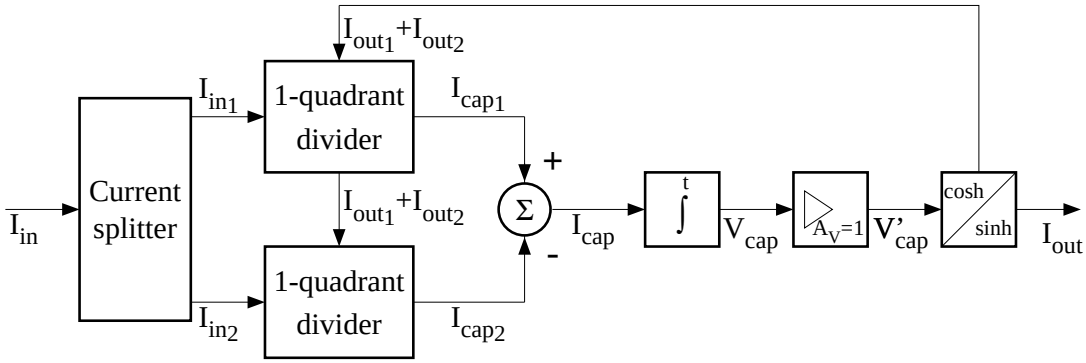

Figure 3.7: Block schematic of the class-AB translinear integrator.

3.5.4 Circuit implementation

The last synthesis step is the circuit implementation. The TL decomposition has to be mapped onto a TL circuit topology and the correct collector currents have to be forced through the transistors. Biasing methods for bipolar all-NPN TL topologies are presented in [104]. Additional implementation methods include the use of (vertical) PNPs, compound transistors or (simple) nullor implementations. If subthreshold MOSTs are used, some additional possibilities are the application of the back gate [105] and operation in the triode region [106].

The system blocks can be implemented by TL circuits, except of course the voltage buffer. To facilitate low-voltage operation, only folded TL loop topologies are allowed. A bipolar IC technology is used to implement the individual blocks.

Design of the input current splitter

A current splitter generates the currents I_{in_1} and I_{in_2} at the input of the integrator. In principle, the type of current splitter to be used at the input is not dictated by Equation (3.17). As the output stage is a geometric mean current splitter, the same function was chosen for the input current splitter.

The TL loop equation to be implemented is $I_{\mathrm{dc}}^2 = I_{\mathrm{in}_1} I_{\mathrm{in}_2}$. Figure 3.8 depicts a 1 volt realization of this equation. The core of the circuit is the TL loop formed by Q_1 through Q_4. Transistors Q_1 and Q_3 are biased at a dc current I_{dc_1}. Transistor Q_2 conducts I_{in_2}. This current is inverted by a PNP current mirror and added to I_{in}. The resulting current I_{in_1} is conducted by Q_4, which is enforced by the Common-Collector (CC) stage Q_5. Biasing of Q_5 by means of a dc tail current source of the differential pair Q_2-Q_3 requires a relatively high dc current. This is disadvantageous with respect to the quiescent current consumption. A solution is dynamic biasing. The tail current of Q_2-Q_3 is generated by Q_6, Q_7 and Q_9, and equals $3I_{\mathrm{dc}_1} + I_{\mathrm{in}_2}$. Hence, Q_5 is biased at a dc current equal to only $2I_{\mathrm{dc}_1}$.

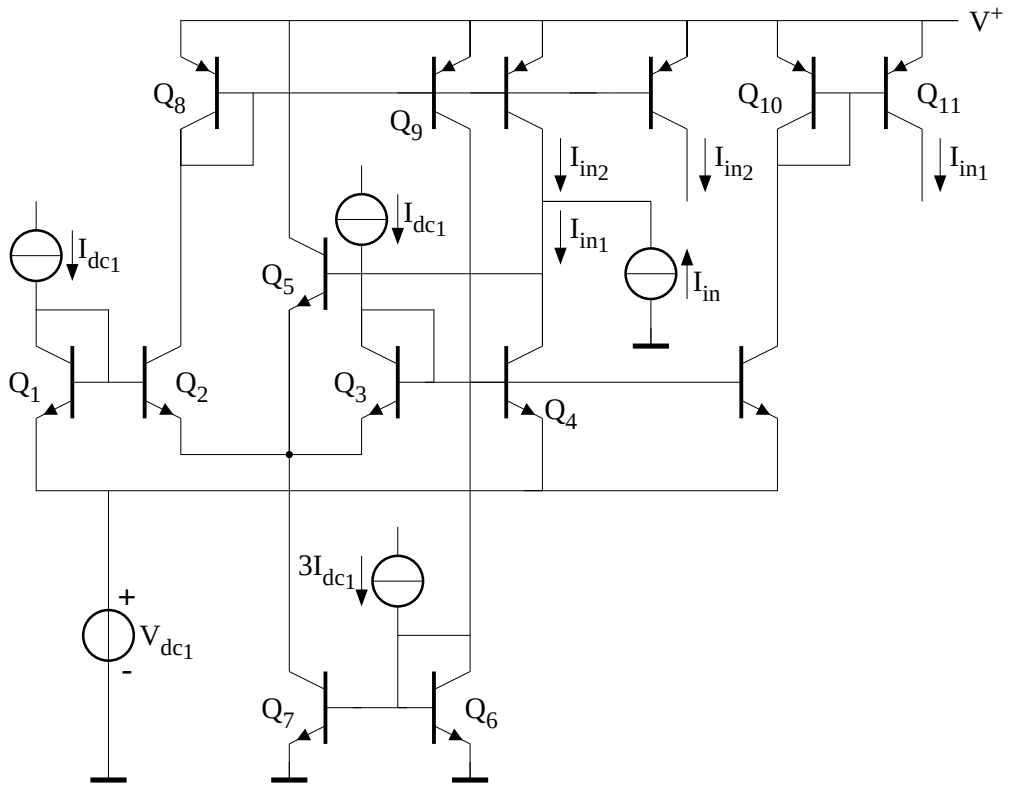

Figure 3.8: Implementation of the input current splitter.

The voltage source V_{dc_1} is necessary to ensure that the Q_7 does not saturate. Note that this voltage source has no effect on the TL loop. A convenient value for V_{dc_1} is 200 mV.

Design of the multiplier/divider

Once the bipolar input current $I_{\rm in}$ is decomposed into two positive currents $I_{\rm in_{1,2}}$, such that the difference of these currents equals $I_{\rm in}$, the two-quadrant multiplication of $I_{\rm in}$ can now be performed by the individual division of $I_{\rm in_1}$ and $I_{\rm in_2}$ by $I_{\rm out_1} + I_{\rm out_2}$, by means of two one-quadrant multiplier/dividers. The output currents of the one-quadrant multiplier/dividers satisfy:

$$I_{\rm cap_{1,2}} = \frac{I_o I_{\rm in_{1,2}}}{I_{\rm out_1} + I_{\rm out_2}}. \tag{3.18}$$

As all linear factors in Equation (3.18) are strictly positive, it is a valid TL decomposition.

The 1 volt implementation of Equation (3.18) is shown in Figure 3.9. The second-order TL loop comprises Q_{12}–Q_{15}. Transistors Q_{13} and Q_{14} are biased by supplying respectively the currents $I_{\rm out_1} + I_{\rm out_2}$ and $I_{\rm in_{1,2}}$ to the emitters of these devices. The collector current I_o of Q_{12} is enforced by the CC stage Q_{16}, which is biased by a dc current $I_{\rm bias1}$.

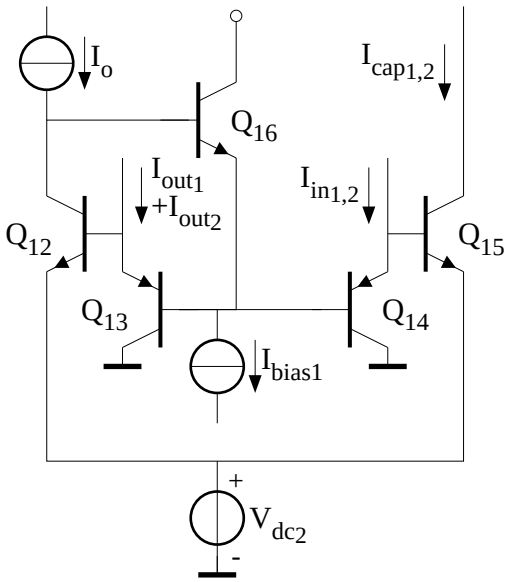

Figure 3.9: Implementation of the one-quadrant multiplier/divider.

A voltage source $V_{\rm dc_2}$ is necessary to ensure that the base voltages of Q_{13} and Q_{14} are always positive. Again, 200 mV is a convenient value.

The output of the multiplier/divider is the collector current of Q_{15}. Subtraction of $I_{\rm cap_1}$ and $I_{\rm cap_2}$ is performed by a PNP current mirror inverting $I_{\rm cap_2}$.

Design of the voltage buffer

The current $I_{\rm cap_1} - I_{\rm cap_2}$ is supplied to the capacitor resulting in the voltage $V_{\rm cap}$. A voltage buffer is used to minimize the interaction between the capacitor and the $\sinh$ output stage. The principle of the buffer amplifier is depicted in Figure 3.10(a). Ideally, the buffering is performed by the nullor. A level-shift between the input and the output of the buffer, represented by the

voltage source V_{dc_3}, is necessary to avoid saturation of Q_{15} in the first multiplier/divider circuit. The output voltage is denoted by V'_{cap}.

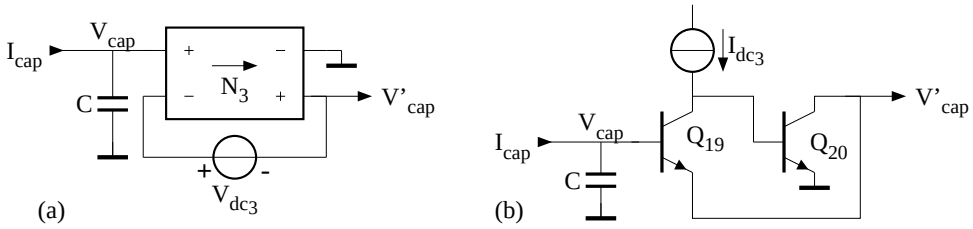

Figure 3.10: (**a**) Principle and (**b**) implementation of the voltage buffer.

The practical implementation of the nullor and the voltage source V_{dc_3} is shown in Figure 3.10(b). The nullor is implemented by two Common-Emitter (CE) stages, Q_{19} and Q_{20}. The level-shift is realized by the base-emitter voltage of Q_{19}. The output transistor Q_{20} must be able to sink the input current of the $\sinh$ output stage.

Design of the $\sinh$ output stage

The output stage has two functions. First, it enforces a geometric mean relation between the two output currents I_{out_1} and I_{out_2}. Secondly, it must provide the current $I_{\mathrm{out}_1} + I_{\mathrm{out}_2}$ to each of the multiplier/dividers, as shown in Figure 3.7.

The 1 volt realization of the output stage is depicted in Figure 3.11. The TL loop comprising Q_{21}–Q_{24} implements the $\sinh$ function given by:

$$I_{\mathrm{out}} = 2I_{\mathrm{dc}_2} \sinh \frac{V'_{\mathrm{cap}} - V_{\mathrm{dc}_4}}{V_T}, \tag{3.19}$$

where I_{dc_2} is a dc current. Note that Equation (3.19) is equivalent to the geometric mean function $I^2_{\mathrm{dc}_2} = I_{\mathrm{out}_1} I_{\mathrm{out}_2}$.

The current $I_{\mathrm{out}_1} + I_{\mathrm{out}_2}$ is supplied to the multiplier/dividers by means of PNP current mirrors. The output current I_{out} is generated by additional NPN current mirrors. The inverted output current $-I_{\mathrm{out}}$ is added to easily enclose the integrator in a unity-feedback configuration by connecting $-I_{\mathrm{out}}$ to the input of the integrator, which results in a first-order low-pass filter.

The voltage source V_{dc_4} is necessary to ensure that the emitter voltages of Q_{22} and Q_{23} are always positive. Once again, 200 mV is a convenient value.

3.5.5 Measurement results

Now that all the individual system blocks have been designed at circuit level, the sub-circuits can be linked together to form the integrator as depicted in Figure 3.7. For biasing purposes, the integrator is enclosed in a unity-feedback configuration, as discussed previously. This results in a first-order low-pass filter. Application of this filter in a hearing instrument was pursued. This leads to the required filter specifications shown in Table 3.1 [107]. For measurement purposes,

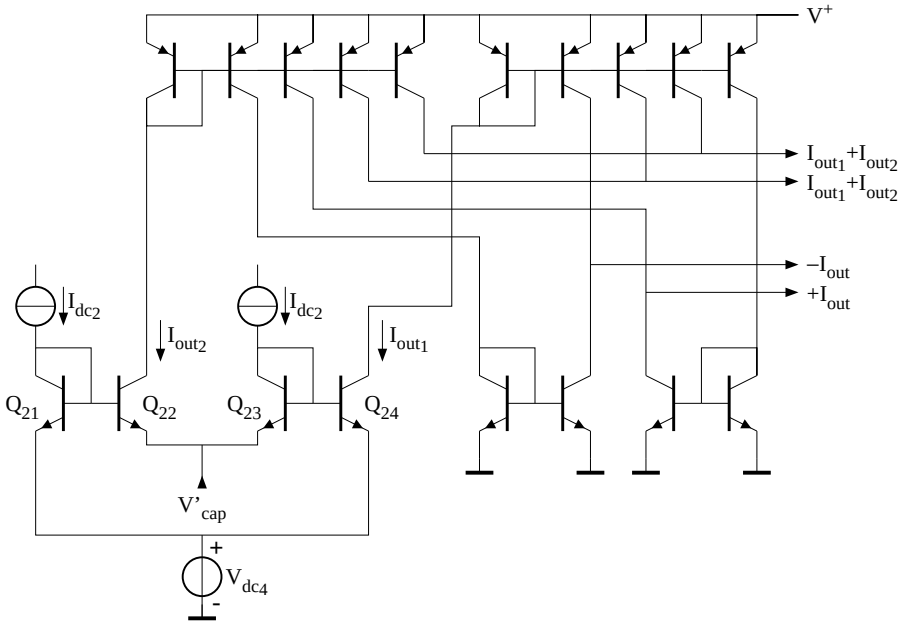

Figure 3.11: Implementation of the sinh output stage.

Table 3.1: Filter requirements.

Quantity	Value	Comment
Supply voltage	down to 1 V	
Current consumption	$< 5\ \mu$A	$I_{\mathrm{in,max}} = 180$ nA$_\mathrm{p}$
Cut-off frequency (f_c) range	1.6–8 kHz	controllable
Dynamic range	68 dB	100 Hz–8 kHz
Total harmonic distortion	< 2 %	$f = 1$ kHz, $f_\mathrm{c} = 1.6$ kHz, $I_\mathrm{in} < 130$ nA$_\mathrm{p}$
	< 7 %	$f = 1$ kHz, $f_\mathrm{c} = 1.6$ kHz, $I_\mathrm{in} > 130$ nA$_\mathrm{p}$

the biasing current sources I_{dc_1}, I_{dc_2}, I_{dc_3} and I_{bias1} are realized by simple current mirrors and high-valued resistors. The frequency control current I_o is realized with a PTAT current source.

To verify the integrator operation in practice, a semi-custom version of the active circuitry of the complete filter has been integrated in a standard 2-μm, 7-GHz process, fabricated at the Delft Institute of Microelectronics and Submicron Technology. Typical transistor parameters are: $h_{\mathrm{fe,NPN}} \approx 100$, $f_{T,\mathrm{NPN}} \approx 7$ GHz, $h_{\mathrm{fe,LPNP}} \approx 80$ and $f_{T,\mathrm{LPNP}} \approx 40$ MHz. The dc currents are set to $I_{\mathrm{dc}_1} = I_{\mathrm{dc}_2} = I_{\mathrm{dc}_3} = 45$ nA, and $I_{\mathrm{bias1}} = 135$ nA.

The capacitor has a value of 100 pF and is connected externally. The voltage sources $V_{\mathrm{dc}_{1,2,4}}$ equal 200 mV and are implemented by a resistive voltage divider.

The measurement results are summarized in Table 3.2 and are in good agreement with the expectations.

Table 3.2: Filter specifications.

Quantity	Value	Comment
Minimal supply voltage	0.95 V	
Supply current	1.9 μA	$I_{\rm in}$ = 180 $\rm nA_p$
Quiescent supply current	1.6 μA	
Cut-off frequency range	1– $>$ 8 kHz	
Maximal signal-to-noise ratio	63 dB	100 Hz–8 kHz
Dynamic range	73 dB	100 Hz–8 kHz
Max. total harmonic distortion	2.7 %	$f_{\rm in} = 1$ kHz, $f_{\rm c} = 1.6$ kHz, $I_{\rm in} = 180$ $\rm nA_p$

3.6 Conclusions

In this chapter, it was shown that dynamic translinear circuits constitute an exciting new approach to the structured design of analog signal processing functions, using transistors and capacitors only. The presented design methodology was elaborated into the design of a class-AB translinear sinh integrator for audio filter applications. Measurements on a semi-custom version of the integrator illustrate the attractive properties of dynamic translinear circuits for low-power and low-voltage applications.

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