Exam Analog Integrated Circuit Design (ET 4252)
August 30, 2007
14:00-17:00h

This exam consists of three main questions. Please start on a new sheet of paper for each main question.

You are allowed to use a calculator and one piece of A4-sized paper with hand-written, non-copied personal notes.

Prefixes:

Giga	(G)	$= 10^{9}$
Mega	(M)	$= 10^{6}$
kilo	(k)	$= 10^{3}$
milli	(m)	$= 10^{-3}$
micro	(μ)	$= 10^{-6}$
nano	(n)	$= 10^{-9}$
pico	(p)	$= 10^{-12}$
femto	(f)	$= 10^{-15}$
atto	(a)	$= 10^{-18}$

$k = 1.38 \cdot 10^{-23}$ J/K (Boltzmann's constant)

$q = 1.60 \cdot 10^{-19}$ C (elementary charge)

$V_T = \frac{kT}{q} = 25.9\text{mV at } T = 300K$

Do not forget to put your name and study number on all material you hand in. And please turn off your mobile phone.

Good luck!

Dr.ir. Wouter A. Serdijn
Dr.ir. Aleksandar Tasic

Question 1: Design of a Voltage-Controlled Oscillator (VCO) for an Impulse-Radio Ultra-Wideband (UWB) Quadrature Downconverter

A negative resistance LC voltage-controlled oscillator is shown in Fig. 1.

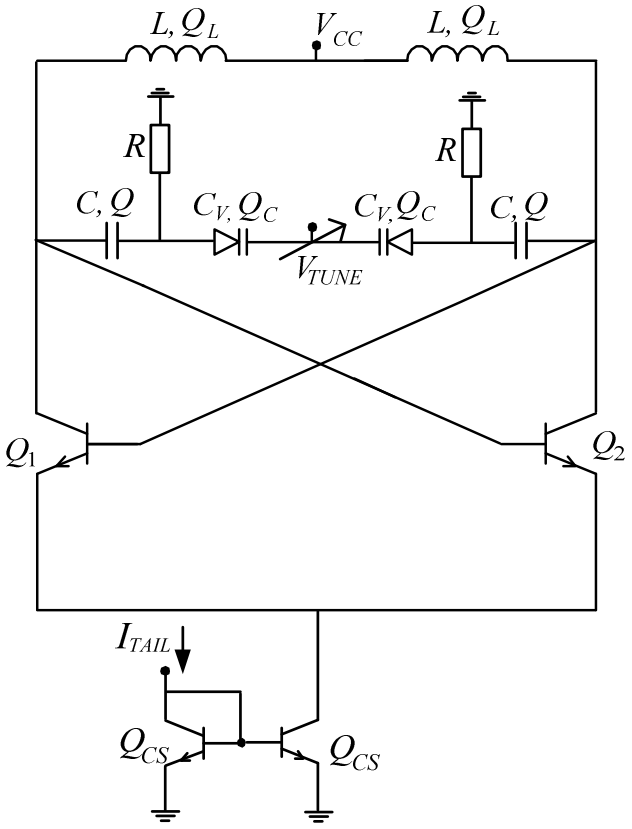


Figure 1: LC voltage-controlled oscillator.

The oscillator consists of a resonating LC tank, a cross-coupled transconductance amplifier (Q_1 and Q_2), and a bias current source (Q_{CS}). L stands for the tank inductance, Q_L for its quality factor, C_V for the varactor capacitance, Q_C for its quality factor, C for the additional tank capacitance (C=C_V at the oscillation central frequency) with a quality factor Q=2Q_C, and I_{TAIL} for the bias tail current. For the bias resistor R it holds: R>>1.

Determine the circuit parameter values of this oscillator in order to meet the requirements of the impulse-radio UWB quadrature downconverter.

The oscillator requirements for the impulse-radio UWB quadrature downconverter are:

- oscillation central frequency of 5.7GHz
- phase noise better than –80dBc/Hz at 1MHz offset from the oscillation central frequency
- peak amplitude of a differential oscillation voltage signal across the LC-tank around 400 mV
- power consumption drawn from a supply voltage of V_{CC}=1.8V as low as possible

For a silicon technology chosen, inductors with quality factors of 30 and varactors with quality factors of 40 are available. The noise factor of the oscillator active part equals A=4.

Provide the following:

a) (5%) Derived expression for the LC-tank impedance (Z) at an offset angular frequency ($\Delta\omega$) from the oscillation angular frequency without considering inductor and capacitor losses.

b) (15%) Derived expression for the LC-tank conductance (G_{TK}) at the oscillation frequency (f_0).

c) (5%) Expression for the oscillation frequency and oscillation condition.

d) (10%) Derived expression for the phase noise of the oscillator. Model the noise contribution of the LC-tank to the phase noise by its loss resistance (R_{TK}), and the active part noise contribution by a factor AG_{TK}, A being its noise factor.

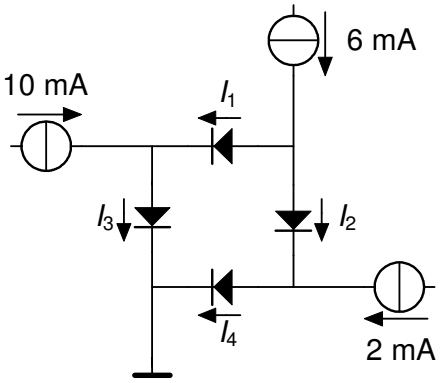
e) (35%) Values of inductance L, varactor capacitance C_V, and tail current I_{TAIL} for the oscillator requirements at the central oscillation frequency, using the results obtained in a)-d).

f) (15%) Values of minimum ($C_{V,MIN}$) and maximum ($C_{V,MAX}$) varactor capacitances to overcome the effects of 10% absolute tolerance on the inductors, varactors and capacitors used.

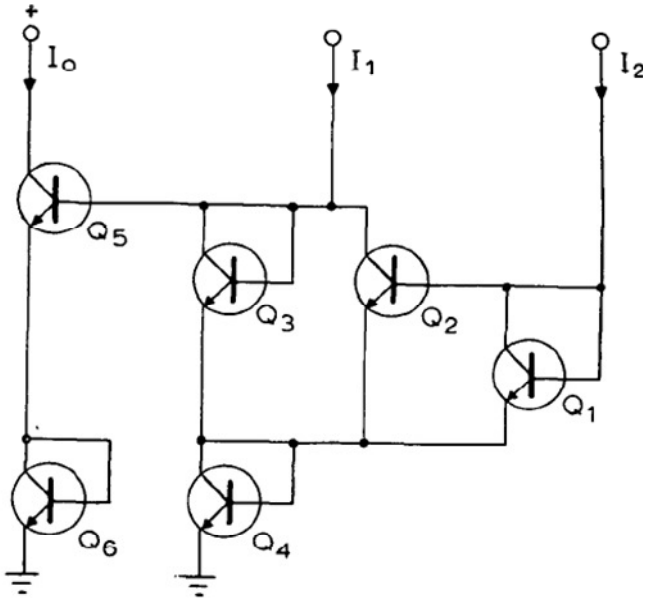
g) (15%) Ways to reduce the power consumption (at the expense of phase noise, which is acceptable in this application) by changing the active circuit (not the LC-tank configuration).

Question 2: Translinear and biasing circuits

a) A bridge rectifier can be viewed as a translinear loop. Assuming identical diodes, what are the four diode current values I_1, I_2, I_3 and I_4 in the figure below?



b) Analyze the output current I_o in terms of the input currents I_1 and I_2 for the circuit below. All transistors are equivalent.



c) What restrictions hold for the magnitudes of the input currents I_1, I_2 and I_o in the above circuit? Write them in the form of inequalities, such as $I_y > 0$.

We will now concentrate on the design of a current source that delivers I_1. Assume its output current to be constant and equal to 2mA. Also, assume I_2 to be equal to 1mA.

d) What is the load impedance of the current source, i.e., what is the value of the (low-frequency) impedance seen by the current source that delivers I_1?

e) Design a single-transistor (i.e., having one transistor only and possibly a few passive components, such as resistors, capacitors, etc.) current source to implement I_1.

f) What is the value of its (low-frequency) output impedance?

g) Give two possible ways to improve the power-supply rejection of your current source implementation.

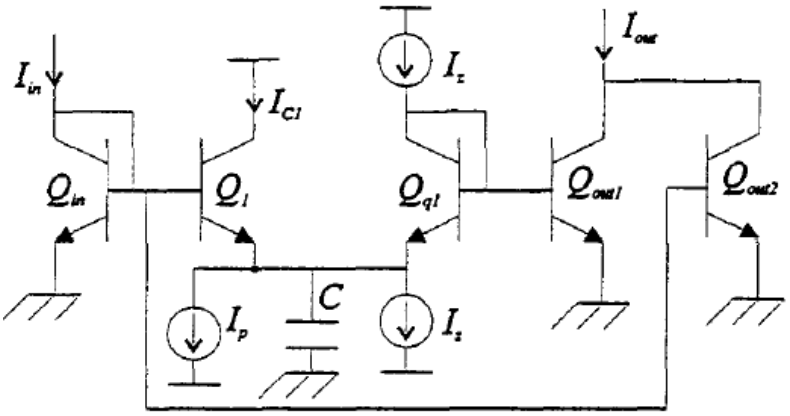
h) Now redesign the above translinear circuit, having the same input-output relation, employing PNP ánd NPN (thus not only NPN or only PNP) transistors, for operation from a 2-V supply. The parameters $I_{S,PNP}$ and $I_{S,NPN}$ are different and subject to absolute tolerances. The transistor's current-gain factor BF is large, but finite (i.e., not infinite).

i. First choose a correct translinear loop topology.
ii. Subsequently assign the correct collector currents (i.e., choose which current flows through which transistor).
iii. Finally, take care of appropriate biasing. Assume ideal biasing and input sources.

Question 3: Dynamic translinear and biasing circuits

Consider the dynamic translinear circuit (DTL) below. The circuit behaves as a non-ideal integrator.

a) Analyze its input-output relation in terms of I_z, I_p, C, I_{in} and I_{out}. All NPN transistors are identical.



b) Now redesign the above non-ideal integrator in such a way that its input-output relation becomes that of an ideal integrator:

$$I_{in} = \frac{CU_T}{I_z}\frac{dI_{out}}{dt}, \text{ or } I_{out} = \frac{I_z}{CU_T}\int I_{in}dt$$

NB. The (quiescent) current through Q_1 should be always positive.

c) If we wish to make the above integrator temperature independent what type of current source I_z do we need?

- A resistor
- A peaking current source
- A proportional-to-absolute-temperature current source
- A bandgap current reference

Give also a motivation for this.

d) Design the chosen current source at transistor level, using BJT (NPN and/or PNP) transistors and resistors, operating from a 2-V supply and delivering 1mA at room temperature.

e) **Bonus question.** If the output resistance (due to the Early effect) of the transistors in the current source designed above is low, give ways (the more the better) to reduce the dependence of I_z on the supply voltage.