Exam Analog Integrated Circuit Design (ET 4252)
August 28, 2008
14:00-17:00h

Delft University of Technology
Faculty of Electrical Engineering, M&CS
Dept. of Microelectronics
Section Electronic Circuit Design

This exam consists of three main questions. Please start on a new sheet of paper for each main question.

You are allowed to use a calculator and one piece of A4-sized paper with hand-written, non-copied personal notes.

Prefixes:

Giga	(G)	$= 10^{9}$
Mega	(M)	$= 10^{6}$
kilo	(k)	$= 10^{3}$
milli	(m)	$= 10^{-3}$
micro	(μ)	$= 10^{-6}$
nano	(n)	$= 10^{-9}$
pico	(p)	$= 10^{-12}$
femto	(f)	$= 10^{-15}$
atto	(a)	$= 10^{-18}$

$k = 1.38 \cdot 10^{-23}$ J/K (Boltzmann's constant)

$q = 1.60 \cdot 10^{-19}$ C (elementary charge)

$V_T = \frac{kT}{q} = 25.9\text{mV at } T = 300K$

Do not forget to put your name and study number on all material you hand in. And please turn off your mobile phone.

Good luck!

Dr.ir. Wouter A. Serdijn

Question 1: Design of a Voltage-Controlled Oscillator (VCO) for an Impulse-Radio Ultra-Wideband (UWB) Quadrature Downconverter in CMOS technology

A MOS negative resistance LC voltage-controlled oscillator is shown in Fig. 1.

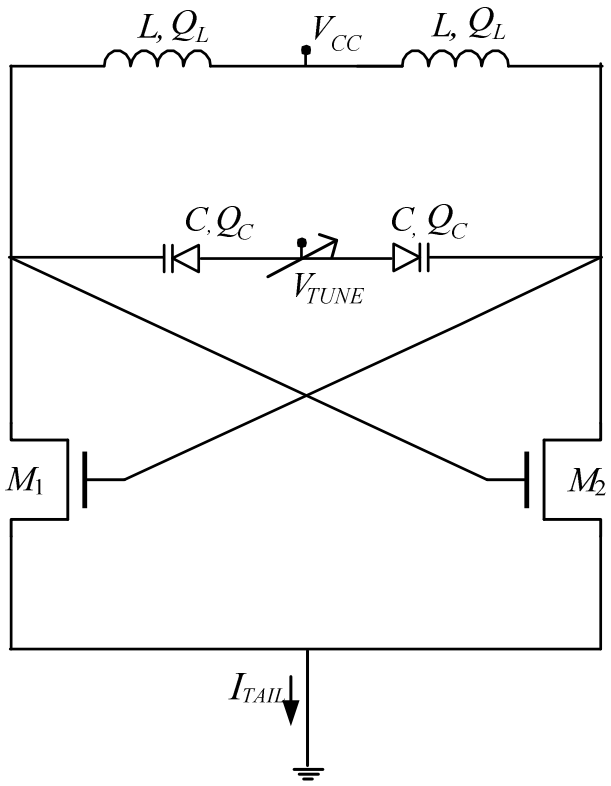


Figure 1: (simple) MOS LC voltage-controlled oscillator.

The oscillator consists of a resonating LC tank and a cross-coupled MOS transconductance amplifier (M_1 and M_2). L stands for the tank inductance, Q_L for its quality factor, C for the varactor capacitance, Q_C for its quality factor, and I_{TAIL} for the tail current.

Determine the circuit parameter values of this oscillator in order to meet the requirements of the impulse-radio UWB quadrature downconverter.

The oscillator requirements for the impulse-radio UWB quadrature downconverter are:

- oscillation central frequency of 7.2 GHz
- phase noise better than –120 dBc/Hz at 10MHz offset from the oscillation central frequency
- peak amplitude of a differential oscillation voltage signal across the LC-tank around 400 mV
- power consumption drawn from a supply voltage of V_{CC} = 1.2V as low as possible

For a silicon technology chosen, inductors with quality factors of 15 and varactors with quality factors of 30 are available. The noise factor of the oscillator active part equals A=7.

Provide the following:

a) Derived expression for the LC-tank impedance (Z) at an offset angular frequency ($\Delta\omega$) from the oscillation angular frequency without considering inductor and capacitor losses.

b) Derived expression for the LC-tank conductance (G_{TK}) at the oscillation frequency (f_0).

c) Expression for the oscillation frequency and oscillation condition.

d) Derived expression for the phase noise of the oscillator. Model the noise contribution of the LC-tank to the phase noise by its loss resistance (R_{TK}), and the active part noise contribution by a factor AG_{TK}, A being its noise factor.

e) Possible values of inductance L, varactor capacitance C, and tail current I_{TAIL} for the oscillator requirements at the central oscillation frequency, using the results obtained in a)-d).

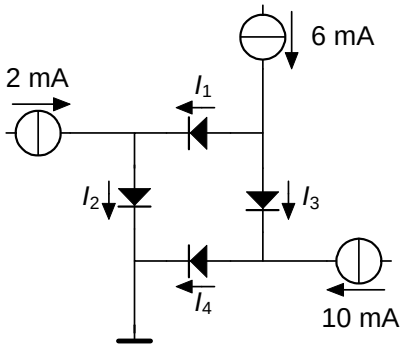
f) Values of minimum (C_{MIN}) and maximum (C_{MAX}) varactor capacitances to overcome the effects of 10% absolute tolerance on the inductors, varactors and transistors used.

g) Ways to reduce the power consumption (at the expense of phase noise, which is acceptable in this application) by *changing the LC-tank configuration* (not the active circuit).

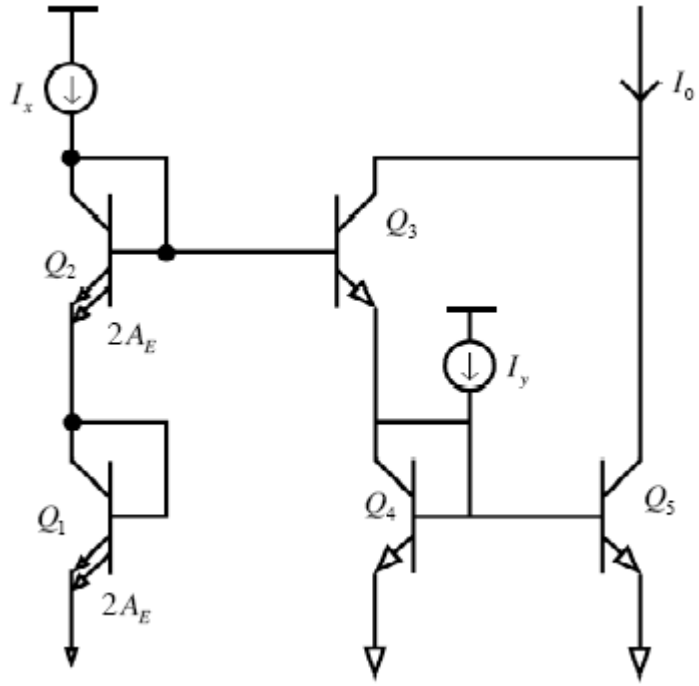
h) Ways to reduce the noise factor of the oscillator active part, while keeping the bias current the same, *by changing the size of M1 and M2* (not the LC tank). Also explain how the minimum noise factor is restricted by the supply voltage.

Question 2: Translinear and biasing circuits

a) A bridge rectifier can be viewed as a translinear loop. Assuming identical diodes, what are the four diode current values I_1, I_2, I_3 and I_4 in the figure below?



b) Analyze the output current I_o in terms of the input currents I_x and I_y for the circuit below. All transistors are equivalent; only Q_1 and Q_2 have a doubled emitter area.



c) What restrictions hold for the magnitudes of the input currents I_x and I_y in the above circuit? Write them in the form of inequalities, such as $I_y > 0$.

We will now concentrate on the design of the lower current source I_y. Assume its output current to be constant and equal to 1 mA. Also assume I_x to be equal to 1 mA.

d) What is the load impedance of the current source, i.e., what is the value of the (low-frequency) impedance seen by current source I_y?

e) Design a single-transistor (i.e., having one transistor only and possibly a few passive components, such as resistors, capacitors, etc.) current source to implement I_y.

f) What is the value of its (low-frequency) output impedance?

g) Give two possible ways to improve the power-supply rejection of your current source implementation.

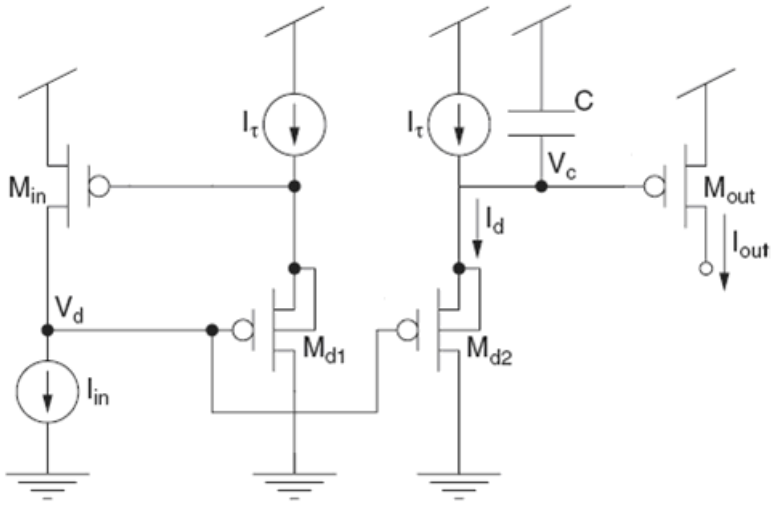
h) Now redesign the above translinear circuit, having the same input-output relation, employing PNP and NPN transistors, for operation from a 1-V supply. The parameters $I_{S,PNP}$ and $I_{S,NPN}$ are different and subject to absolute tolerances. The transistor's current-gain factor *BF* is large, but finite (i.e., not infinite).

   i. First choose a correct translinear loop topology.
   ii. Subsequently assign the correct collector currents (i.e., choose which current flows through which transistor).
   iii. Finally, take care of appropriate biasing. Assume ideal biasing and input sources.

Question 3: Dynamic translinear and biasing circuits

Consider the dynamic translinear circuit (DTL) below. The circuit behaves as a non-ideal integrator.

a) Analyze its input-output relation in terms of I_τ, C, I_{in} and I_{out}. All PMOS transistors are identical and operate in weak inversion (i.e., follow an exponential input-output relation: $I_d = I_s \exp(V_{gs}/V_T)$, I_d being the drain current, I_s being a technology and size dependent specific current, V_{gs} being the gate-source voltage and V_T being the thermal voltage kT/q, approximately 26 mV at room temperature).



b) Now redesign the above non-ideal integrator in such a way that its input-output relation becomes that of an ideal integrator:

$$I_{in} = \frac{CU_T}{I_\tau}\frac{dI_{out}}{dt}, \text{ or } I_{out} = \frac{I_\tau}{CU_T}\int I_{in}dt$$

NB: the drain currents should always remain positive. Capacitance currents are bipolar, i.e., positive and negative, as the average current equals zero.

c) If we wish to make the above integrator temperature independent what type of current source I_τ do we need and why?

- A resistor
- A peaking current source
- A proportional-to-absolute-temperature current source
- A bandgap current reference

d) Design the chosen current source at transistor level, using MOS (NMOS and/or PMOS) transistors and resistors, operating from a 2-V supply and delivering 1mA at room temperature.

e) **Bonus question.** If the output resistance (due to channel length modulation) of the transistors in the current source designed above is low, give ways (the more the better) to reduce the dependence of I_τ on the supply voltage.