Exam Analog Integrated Circuit Design (ET 4252)
January 21, 2009
14:00-17:00h

This exam consists of three main questions. Please start on a new sheet of paper for each main question.

You are allowed to use a calculator and one piece of A4-sized paper with hand-written, non-copied personal notes.

Prefixes:

Giga	(G)	$= 10^{9}$
Mega	(M)	$= 10^{6}$
kilo	(k)	$= 10^{3}$
milli	(m)	$= 10^{-3}$
micro	(μ)	$= 10^{-6}$
nano	(n)	$= 10^{-9}$
pico	(p)	$= 10^{-12}$
femto	(f)	$= 10^{-15}$
atto	(a)	$= 10^{-18}$

$k = 1.38 \cdot 10^{-23}$ J/K (Boltzmann's constant)

$q = 1.60 \cdot 10^{-19}$ C (elementary charge)

$V_T = \frac{kT}{q} = 25.9\text{mV at } T = 300K$

Do not forget to put your name and study number on all material you hand in. And please turn off your mobile phone.

Good luck!

Dr.ir. Wouter A. Serdijn

Question 1: Design of a Voltage-Controlled Oscillator (VCO) for an Impulse-Radio Ultra-Wideband (UWB) Quadrature Downconverter

A negative resistance LC voltage-controlled oscillator is shown in Fig. 1.

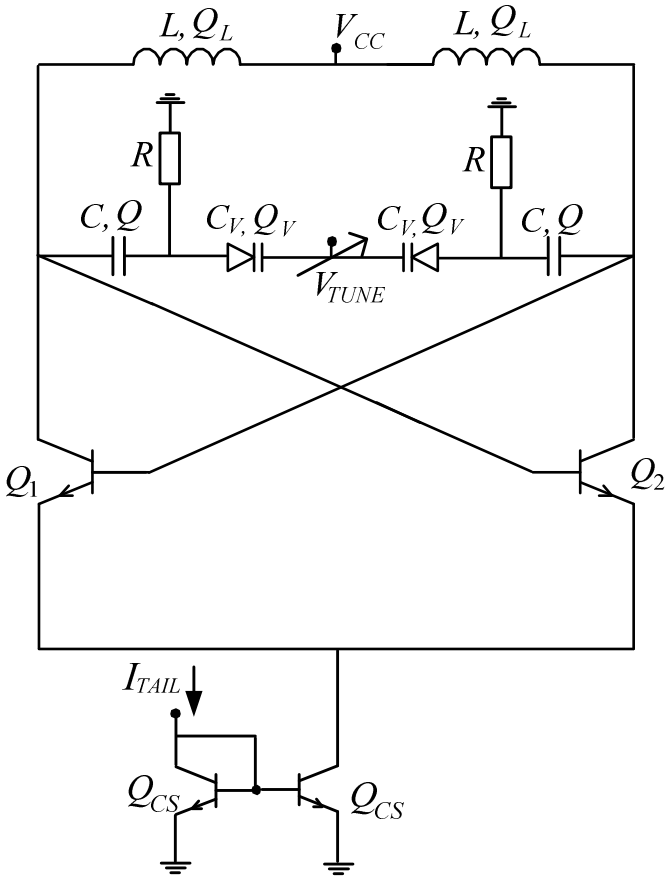


Figure 1: (simple) LC voltage-controlled oscillator.

The oscillator consists of a resonating LC tank, a cross-coupled transconductance amplifier (Q_1 and Q_2), and a bias current source (Q_{CS}). L stands for the tank inductance, Q_L for its quality factor, C for the additional tank capacitance, Q for its quality factor, C_V for the varactor capacitance (C=C_V at the oscillation central frequency), Q_V for its quality factor, and I_{TAIL} for the bias tail current. The resistors R are for biasing purposes only, are very large and thus negligible.

Determine the circuit parameter values of this oscillator in order to meet the requirements of the impulse-radio UWB quadrature downconverter.

The oscillator requirements for the impulse-radio UWB quadrature downconverter are:

- oscillation central frequency of 1.8 GHz
- phase noise better than –120 dBc/Hz at 10MHz offset from the oscillation central frequency
- peak amplitude of a differential oscillation voltage signal across the LC-tank around 400 mV
- power consumption drawn from a supply voltage of V_{CC} = 1.2V as low as possible

For a silicon technology chosen, inductors with quality factors of 15, varactors with quality factors of 30 and capacitors with quality factors 40 are available. The noise factor of the oscillator active part equals A=5.

Provide the following:

a) (5%) Derived expression for the LC-tank impedance (Z) at an offset angular frequency ($\Delta\omega$) from the oscillation angular frequency without considering inductor and capacitor losses.

b) (15%) Derived expression for the LC-tank conductance (G_{TK}) at the oscillation frequency (f_0).

c) (5%) Expression for the oscillation frequency and oscillation condition.

d) (10%) Derived expression for the phase noise of the oscillator. Model the noise contribution of the LC-tank to the phase noise by its loss resistance (R_{TK}), and the active part noise contribution by a factor AG_{TK}, A being its noise factor.

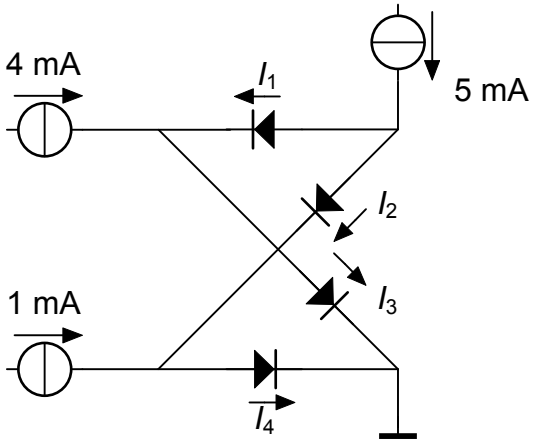
e) (35%) Possible values of inductance L, capacitance C, varactor capacitance C_V, and tail current I_{TAIL} for the oscillator requirements at the central oscillation frequency, using the results obtained in a)-d).

f) (15%) Values of minimum (C_{MIN}) and maximum (C_{MAX}) varactor capacitances to overcome the effects of 10% absolute tolerance on the inductors, capacitors, varactors and transistors used.

g) (15%) Ways to reduce the power consumption (at the expense of phase noise, which is acceptable in this application) by *changing the LC-tank configuration* (not the active circuit).

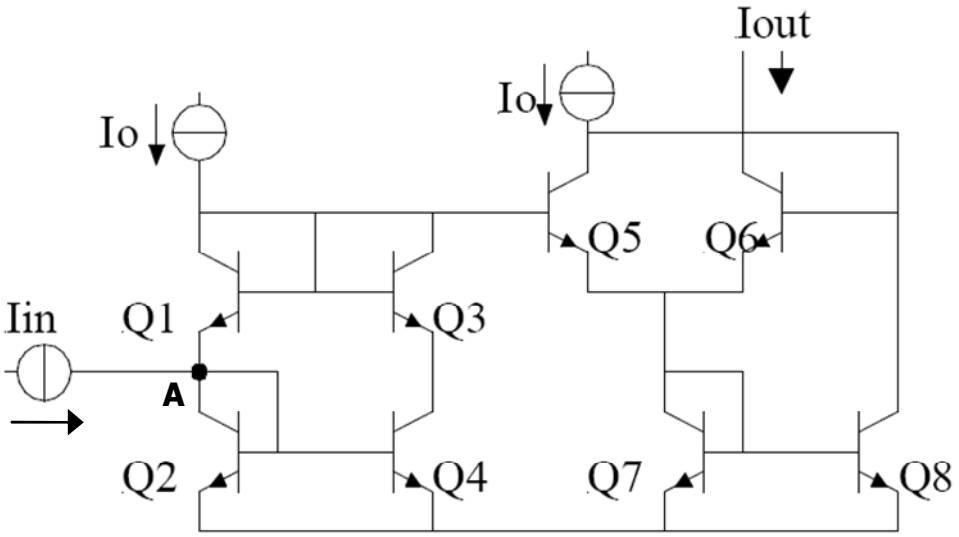
Question 2: Translinear and biasing circuits

a) A double-sided rectifier can be viewed as a translinear loop. Assuming identical diodes, what are the four diode current values I_1, I_2, I_3 and I_4 in the figure below?



b) Analyze the output current I_{out} in terms of the input currents I_{in} and I_O for the circuit below. All transistors are identical.

1. Write down the translinear loop equation(s)
2. Write down the nodal equations
3. Solve the (set of) equation(s)



c) What restrictions hold for the magnitudes of currents I_O, I_{in} and I_{OUT} in the above circuit? Write them in the form of inequalities, such as $I_x > 0$.

d) What do you think is the role of transistor Q3?

We will now concentrate on the design of a current source that delivers I_{in}. Assume its output current to be constant and equal to 2mA. Also assume I_O to be equal to 4mA.

e) What is the load impedance of the current source, i.e., what is the value of the (low-frequency) impedance seen by the current source that delivers I_{in}?

f) Design a single-transistor (i.e., having one transistor only and possibly a few passive components, such as resistors, capacitors, etc.) current source to implement I_{in}. Make sure the current source is compliant with the voltage at node **A**. Assume I_{in} to be positive and that the (positive) supply voltage equals 2V.

g) What is the value of its (low-frequency) output impedance?

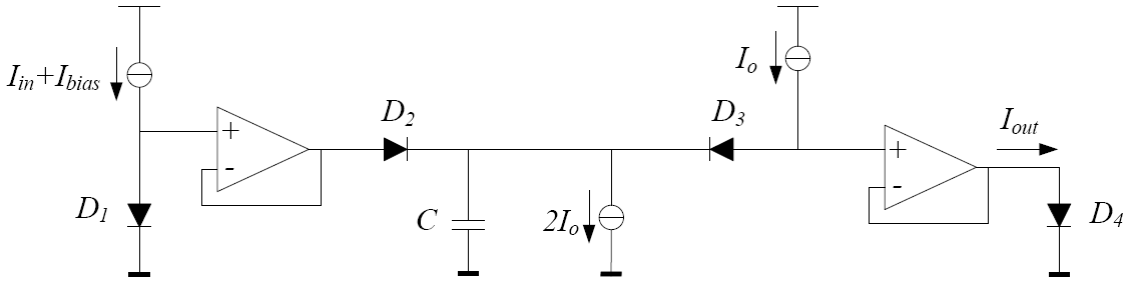
h) Give two possible ways to improve the power-supply rejection of your current source implementation.

Redesign of the entire translinear circuit.

i) Now redesign the above translinear circuit, having the same input-output relation, employing (more than one) PNP ánd (multiple) NPN (thus not only NPN or only PNP) transistors, for operation from the same 2V supply. The parameters $I_{S,PNP}$ and $I_{S,NPN}$ are different and subject to absolute tolerances. The transistor's current-gain factor *BF* is large, but finite (i.e., not infinite).

Question 3: Dynamic translinear and biasing circuits

Consider the 1-V dynamic translinear circuit (DTL) for high-frequency operation below, designed by Haddad and Serdijn, in line with the original idea of Adams (Picture taken from the upcoming book of Haddad and Serdijn, to appear with Springer, March 2009).



a) Analyze its input-output relation in terms of I_o, I_{bias}, C, I_{in} and I_{out}. All diodes are identical.

b) 1. In what configuration are the operational amplifiers connected in the circuit? 2. What do you think is the purpose of the operational amplifiers in the circuit?

c) How would you choose the value of I_{bias} with respect to I_{in}, I_o and I_{out}? Write this in the form of inequalities.

d) Now redesign the above circuit in such a way that its input-output relation becomes that of an ideal integrator:

$$I_{in} = \frac{CU_T}{I_O}\frac{dI_{out}}{dt}$$

NB1. The (quiescent) current through *all the diodes* should be always positive (> 0).
NB2. Assume that, apart from the diodes, also NPN transistors are present that exhibit an identical exponential input-output relation. These may be included in the design.

e) If we wish to make the above integrator temperature independent what type of current source I_o do we need?

- A resistor
- A peaking current source
- A proportional-to-absolute-temperature current source
- A bandgap current reference

Give also a motivation for this.

f) **Bonus question.** If the output resistance of (closed-loop) operational amplifiers in the dynamic translinear circuit above is too high for correct circuit operation, give ways (the more the better) to reduce it.