LC VCO Design Procedure

UMTS VCO

VCO design parameters	*Design requirement*
Oscillating frequency	2.1GHz
Tuning range	400MHz
Voltage swing	0.7V
Phase noise	-110dBc@1MHz
Supply voltage	3V
Power consumption	10mW

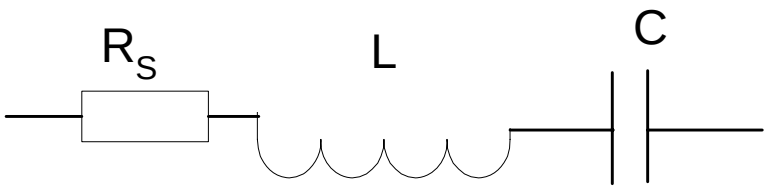
Technology parameters	*Values*
Technology	BiCMOS
Number of metals	4
Transit frequency	50GHz
MIM capacitors	available
Varactors	available

WCDMA Specs	*Value*
Receiving Band (GHz)	2.11-2.17
Channel Spacing (MHz)	5 (3.84)
Multiplex / Modulation	FDD / QPSK
MDSeff (dBm)	-99
SNR (dB) / BER	7 / 1E-3
Processing Gain (dB)	25
Tx-Rx Isolation (dB)	50
Blocker @ 8MHz (dB)	-46

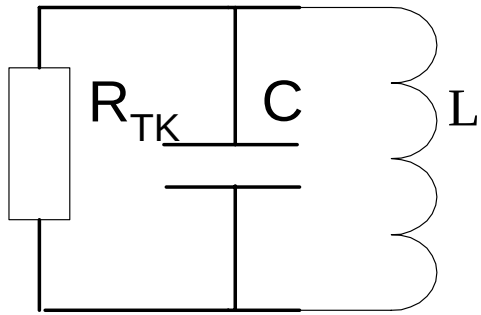
$$\mathcal{L}(8\text{MHz})=-99-(-46)-10\log(3.84e6)-7=-129\text{dBc/Hz}$$

Series vs. Parallel Resonator

- frequency f_0=2.1GHz
- desired signal power P=10mW



Q_L=20



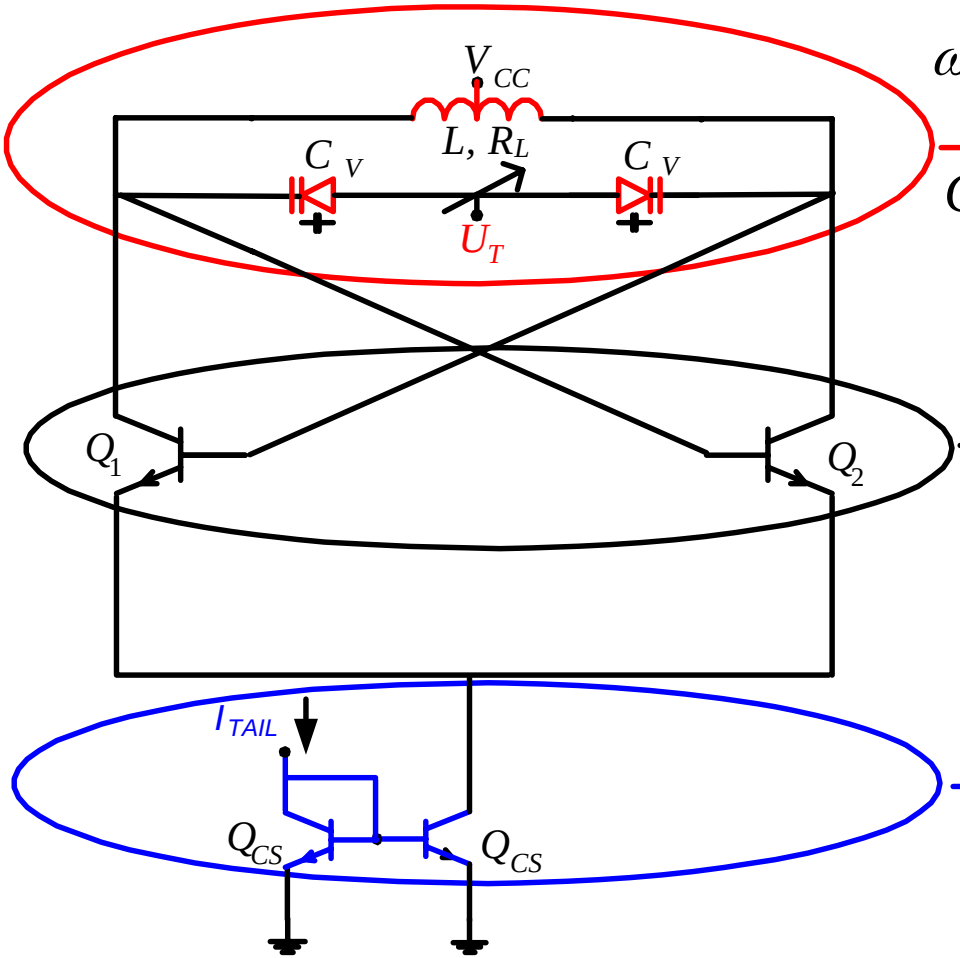
- L=3nH, C=1.9pF, R_S=2Ω
- fundamental current and voltage i=100mA, v=0.2V

- very large current

- L=3nH, C=1.9pF, R_{TK}=800Ω
- fundamental current and voltage i=5mA, v=4V

- moderate current and voltage
- realistic choice

Negative Resistance Oscillator



$$\omega_0 = \frac{1}{\sqrt{LC}}$$

resonating LC tank

$$C = C_V / 2$$

$$-g_m / 2$$

active part

$$I_C = \frac{I_T}{2}$$

biasing current source

LC Tank Design

- oscillation frequency

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \qquad C = C_V / 2$$

- determine *L* and *C*

- tuning range

$$\frac{f_{MAX}}{f_{MIN}} = \sqrt{\frac{\frac{C_{V,MAX}}{C_{V,MIN}} + 2\frac{C_{PAR}}{C_{V,MIN}}}{1 + 2\frac{C_{PAR}}{C_{V,MIN}}}}$$

- parasitics impose larger capacitive tuning range

$$\frac{C_{V,MAX}}{C_{V,MIN}} = \left(\frac{f_{MAX}}{f_{MIN}}\right)^2 + 2\left[\left(\frac{f_{MAX}}{f_{MIN}}\right)^2 - 1\right]\frac{C_{PAR}}{C_{V,MIN}}$$

- determine C_{MAX} and C_{MIN}

How to Choose L?

- tank conductance

$$G_{TK} = \frac{1}{\omega_0 L}\left(\frac{1}{Q_L} + \frac{1}{Q_C}\right)$$

- phase noise

$$\mathcal{L}(\Delta\omega) \cong KT\frac{R_L + 2R_C}{V_S^2} \cdot F\left(\frac{\omega_0}{\Delta\omega}\right)^2$$

- choice of *L*
  - larger *L* => larger Q_L
  - larger *L* => lower G_{TK}
  - larger *L* => larger R_L
  - larger *L* => poorer $\mathcal{L}$
- larger *L* => lower power consumption
- larger *L* => lower f_{RES}, $f_{Q\text{-}PEAK}$
- larger *L* => lower tuning range
- choose for the largest *L* having peak *Q* close to the operating frequency

How to Choose C?

- tank conductance

$$G_{TK} = \frac{R_L}{(\omega_0 L)^2} + 2R_C(\omega_0 C)^2$$

- phase noise

$$\mathcal{L}(\Delta\omega) \cong KT \frac{R_L + 2R_C}{V_S^2} \cdot F\left(\frac{\omega_0}{\Delta\omega}\right)^2$$

- choice of *C*
  - larger *C* => lower *Q*
  - larger *C* => larger G_{TK}
  - larger *C* => larger power consumption
  - larger *C* => larger R_C
  - larger *C* => slightly better $\mathcal{L}$
  - larger *C* => larger tuning range

- choose for *C* providing not more than the required frequency tuning range

Active Part Design

- chosen LC tank parameters determine losses to be compensated

$$G_{TK} = \frac{R_L}{(\omega_0 L)^2} + 2R_C(\omega_0 C)^2$$

- cross-coupled pair conductance

$$g_M = g_m / 2$$

- oscillation condition $g_M > G_{TK}$ determines the very minimum compensating active-devices current

$$I_C = g_m V_T > 2G_{TK} V_T = 2\left(\frac{R_L}{(\omega_0 L)^2} + 2R_C(\omega_0 C)^2\right) V_T$$

- choose for the transistors having enough f_T (~$10f_0$) for the determined collector current

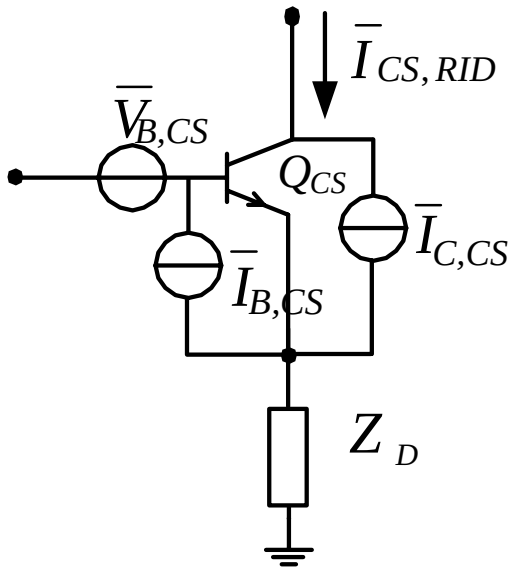
What About Phase Noise?

- there is nothing better than the best LC-tank
- the best LC tank chosen determines power consumption and accordingly active devices operating current
  - shot noise is directly determined by operating current, i.e., LC tank
  - the larger the transistor the lower the base resistance thermal noise (but more parasitics)

- choose for as large transistors as possible having enough f_T (~$10f_0$) for the determined collector current

Tail Current Source

- Tail current noise around even multiples of the oscillating frequency is transformed into the phase noise of the VCO
- Tail current noise contribution larger than all other contributions together
- Reducing the output noise power of the current source, its contribution to the phase noise is reduced as well
  - emitter degeneration reduces the tail-current source noise transfer functions
  - resistive degeneration effective at all frequencies but requires voltage headroom
  - inductive degeneration effective in narrow frequency band but requires no voltage headroom



So Far

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Simulations/ Layout/ Measurements

Design Procedure

- Calculations
  - estimation of design parameters
- Simulations
- Layout
- Measurements

Simulations

- Simulation with estimated idealized components
  - adjustment of estimated design parameters
- Simulation with components' models provided by technology
  - adjustment of estimated design parameters

Layout

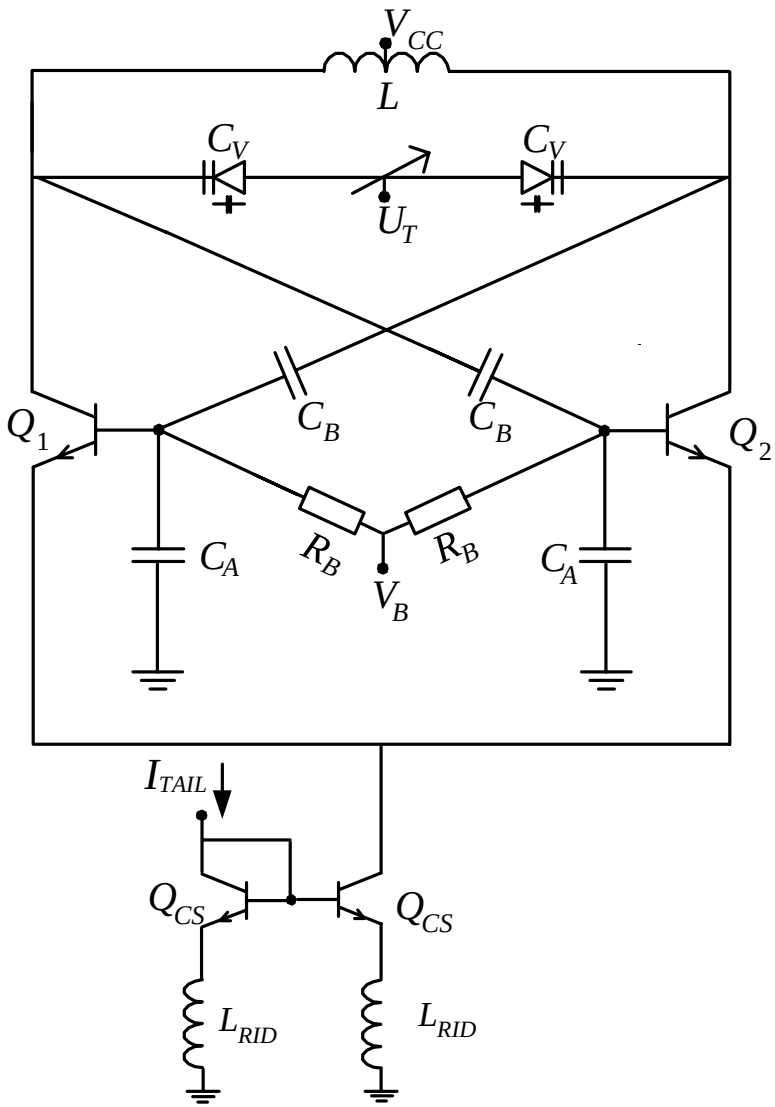
- Layout design
- Layout extraction
- Postlayout simulation
    - adjustment of circuit and layout parameters
- Layout verification
    - design rules check
    - layout versus schematic check

Measurements (Design Verification)

- Chip packaging
- Printed Circuit Board design
- Measurement setup
- Simulation of measurement setup
  - IC-package-PCB
- Interpretation of measured results

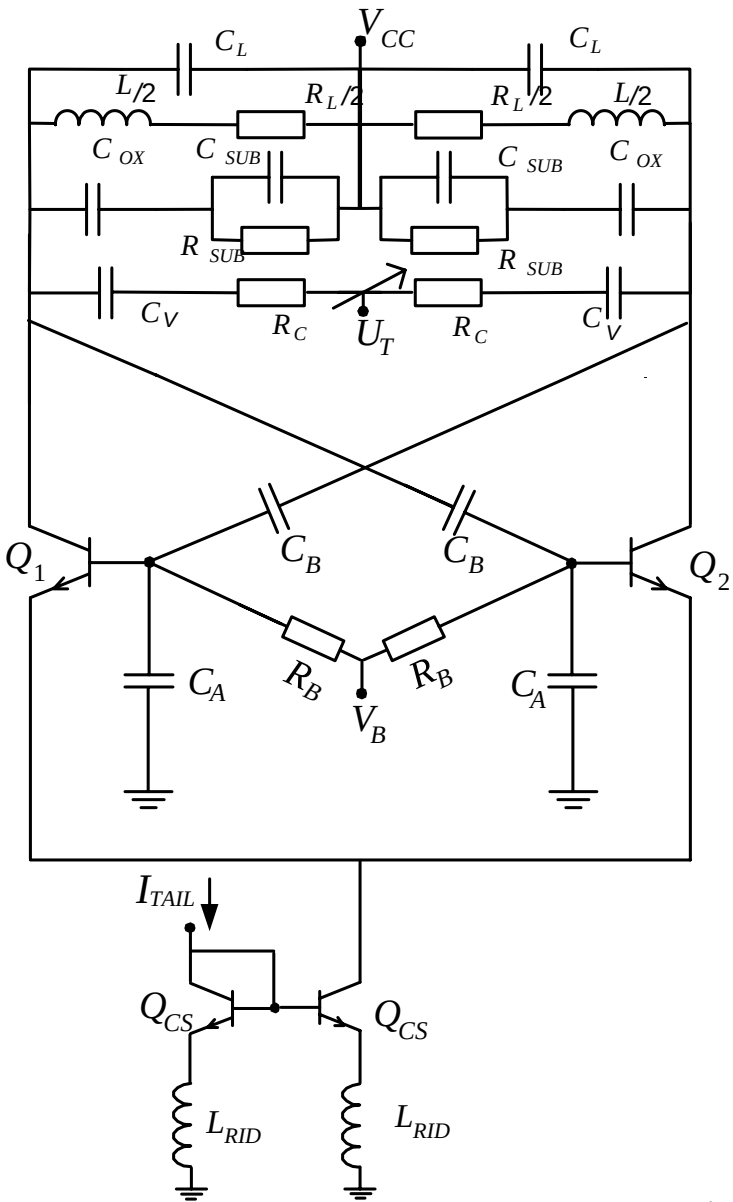
VCO Design Example - Simulations

Idealized VCO Schematic



- L=3nH, Q_L=25, C_{V0}=3.8pF
- C_A=150fF, C_B=600fF
- collector current (0.2mA, 3mA)
- transistor dimensions 0.5x10um^2
- tail current (0.4mA, 6mA)
- TCS transistor dimensions 0.5x20um^2
- L_{RID}=3.4nH

VCO Schematic with Inductor Model



- L=3nH
- n=3, w=20um
- d_{OUT}=320um, s=5um

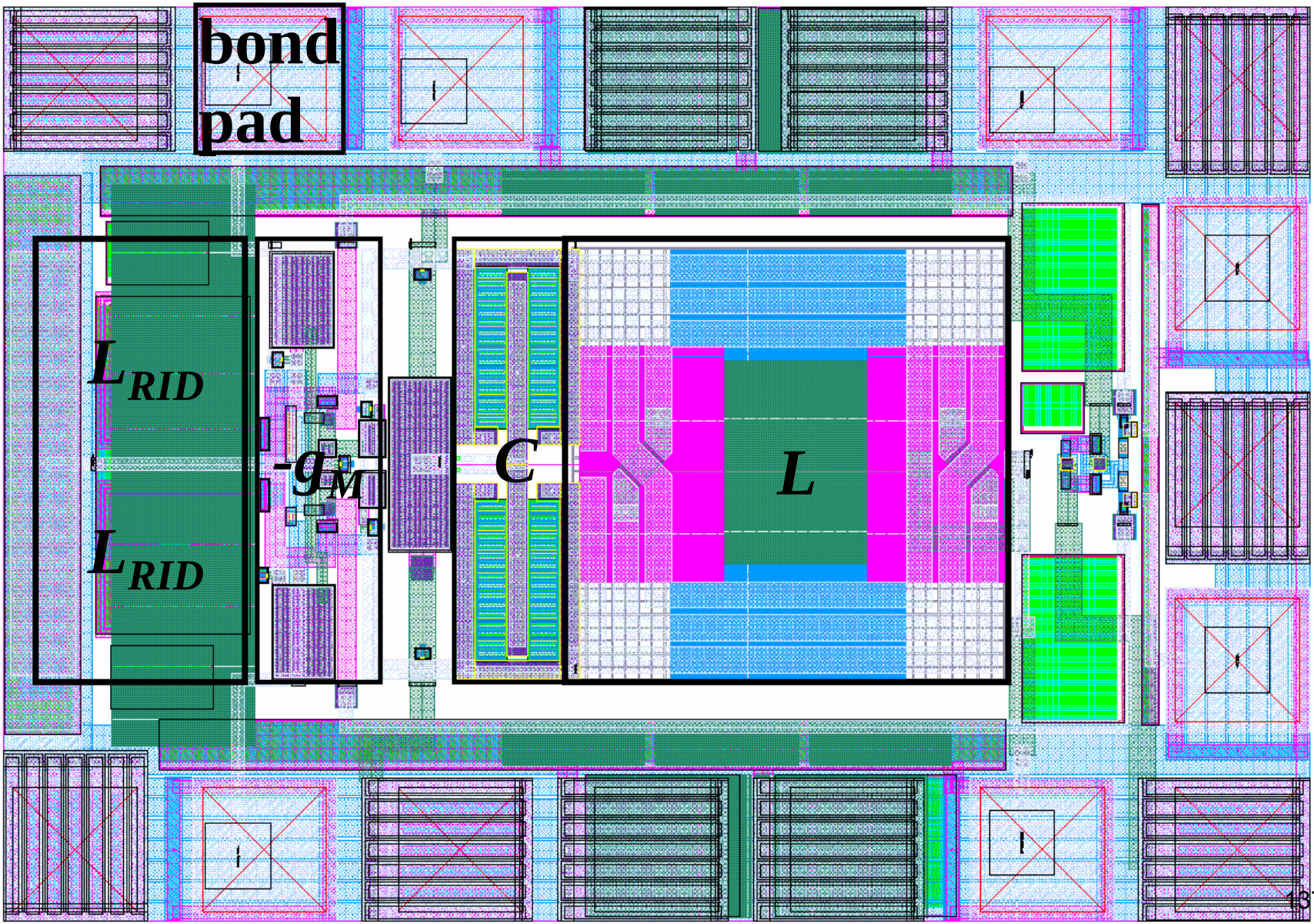
- L_{RID}=3.4nH
- n=6, w=7um
- d_{OUT}=120um, s=1um

VCO Design Example - Layout

Layouting

- Components placement and routing
- Chip padding
- Isolation
    - guard rings
- Protection
    - Electrostatic Discharge (ESD)
- Substrate contacts, metal distribution

VCO Layout – Top View



Placement

- Generation of component layouts
- Component Separation
  - sensitive I/O nodes (RF/LO)
  - sensitive circuits (power amplifiers/oscillator)
  - sensitive sub-systems (analog/digital)
- Component coupling
  - substrate, interconnects, bondwires

Routing

- Track width/length
  - thick(wide)/long/top
  - thin(narrow)/short/bottom
- Current density
  - wide ground/supply lines
- Bottom metal component interconnect
- Top metal circuit/system interconnect

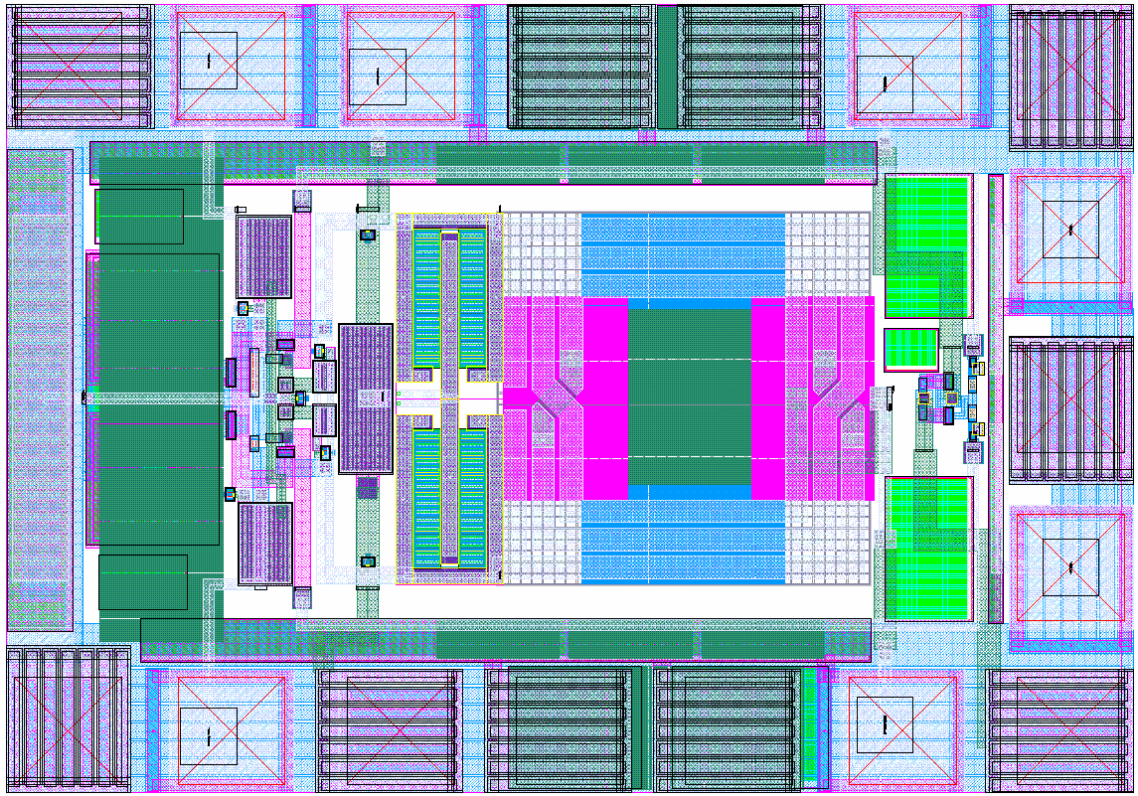
Padding

- IC interface
  - inputs/outputs – information signal lines
  - bias lines – supply, ground
- Area increase
  - size 100x100um^2
  - distance 100um
- ESD for sensitive nodes
- HF circuit performance degradation
  - capacitance added

Design Rules (Layout Verification)

- Component size (width/length)
- Component spacing
- Track width
- Track spacing
- Metal density
- Geometry
- Grid

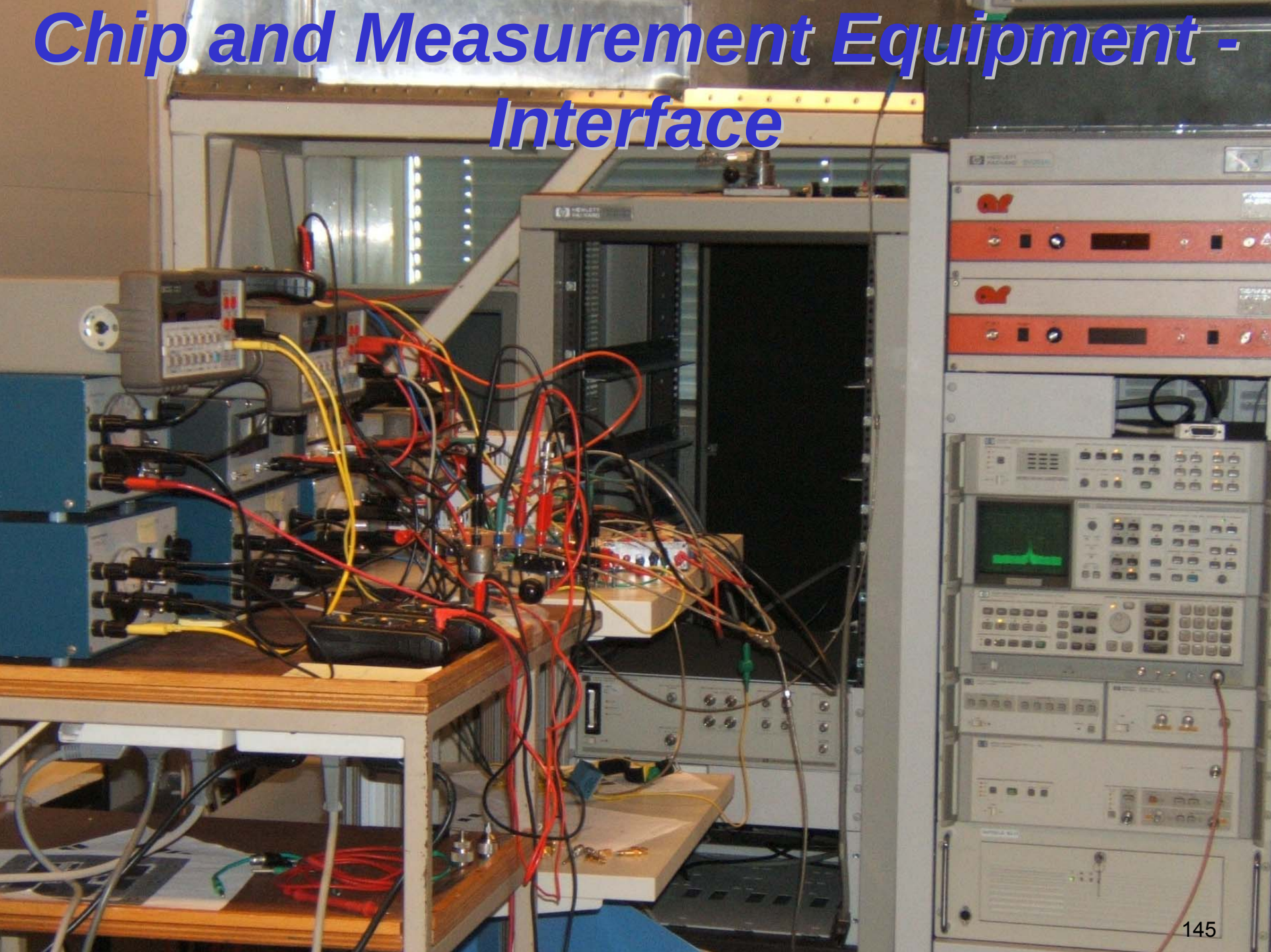
Design Rule Compliant VCO Layout



- Design Rule Check (DRC)
- Comparison of layout and schematic (LVS)
- Generation of output file for fabrication (GDSII)

VCO Design Example - Measurements

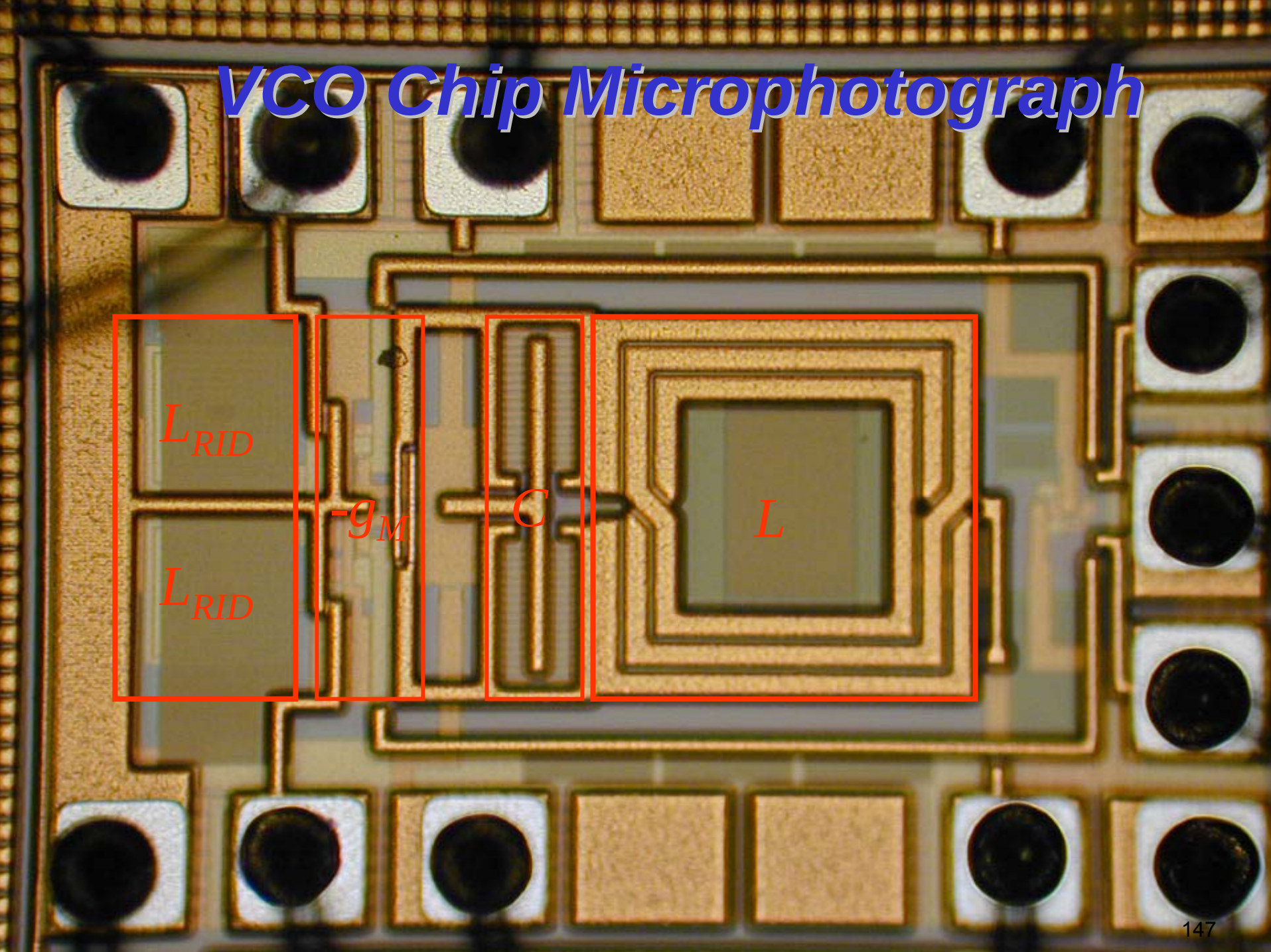
Chip and Measurement Equipment - Interface



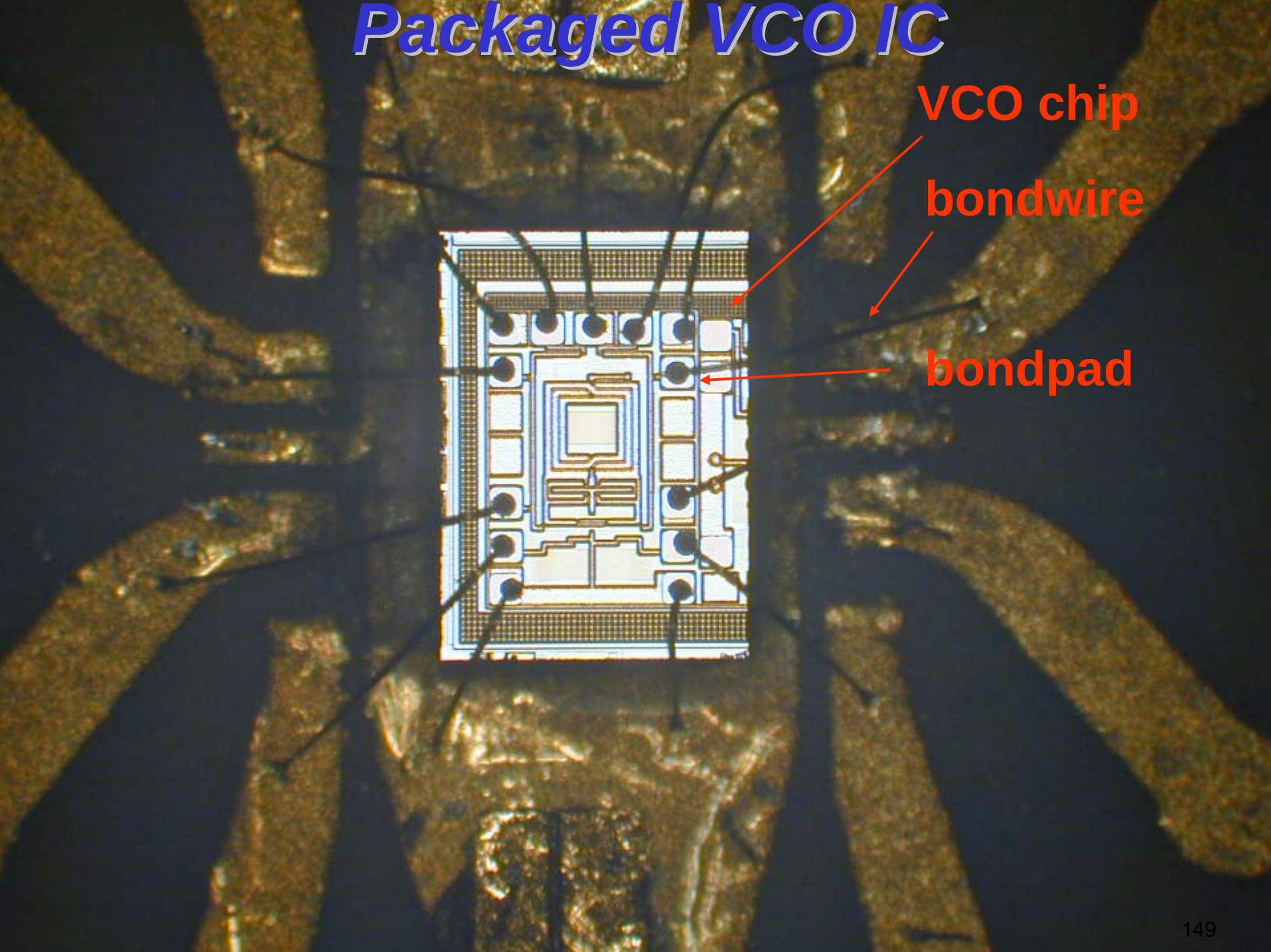
Verification Procedure

- Oscillator chip packaging
- Oscillator IC Printed Circuit Board design
- Measurement setup
- Interpretation of the results

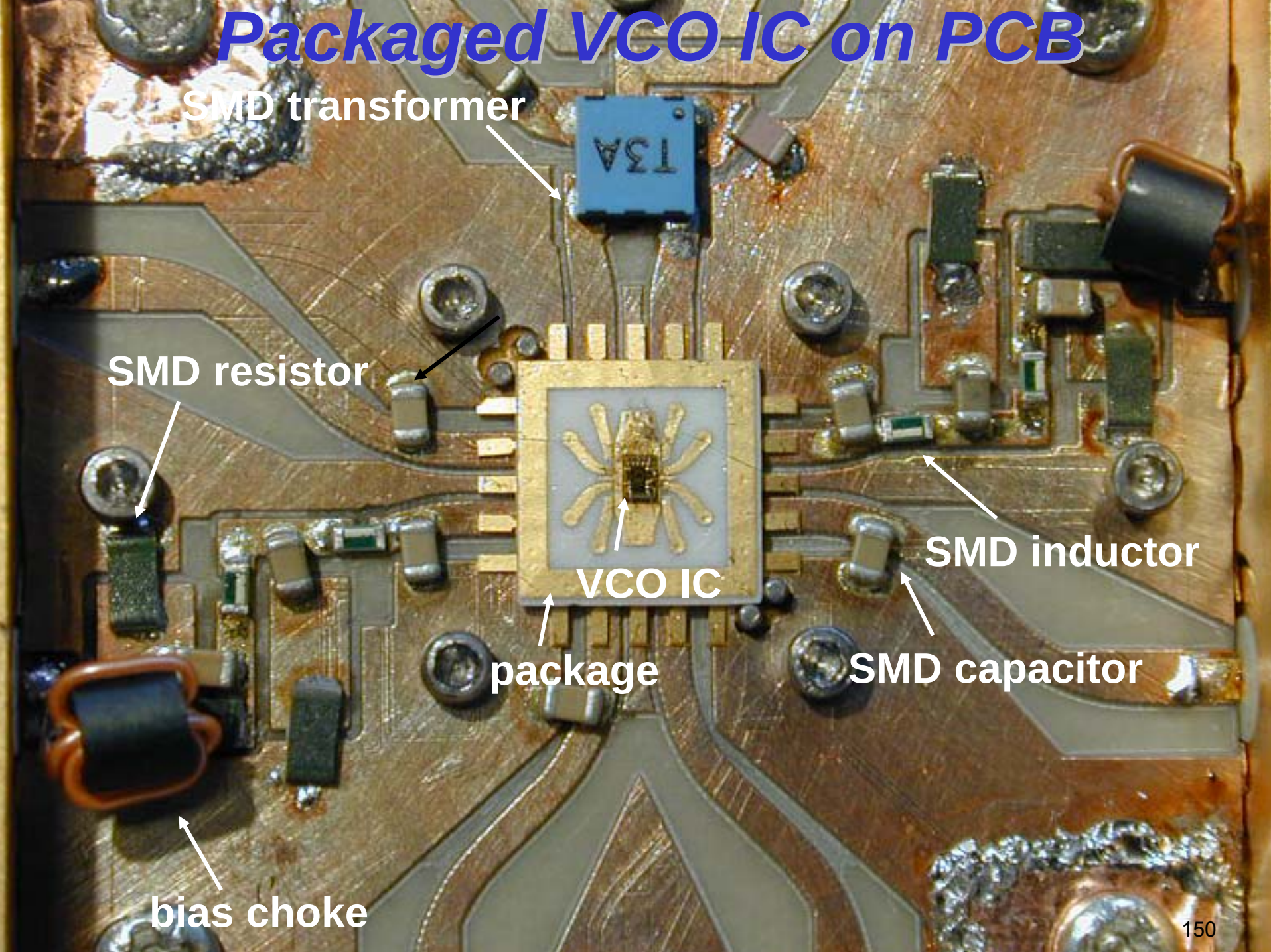
VCO Chip Microphotograph



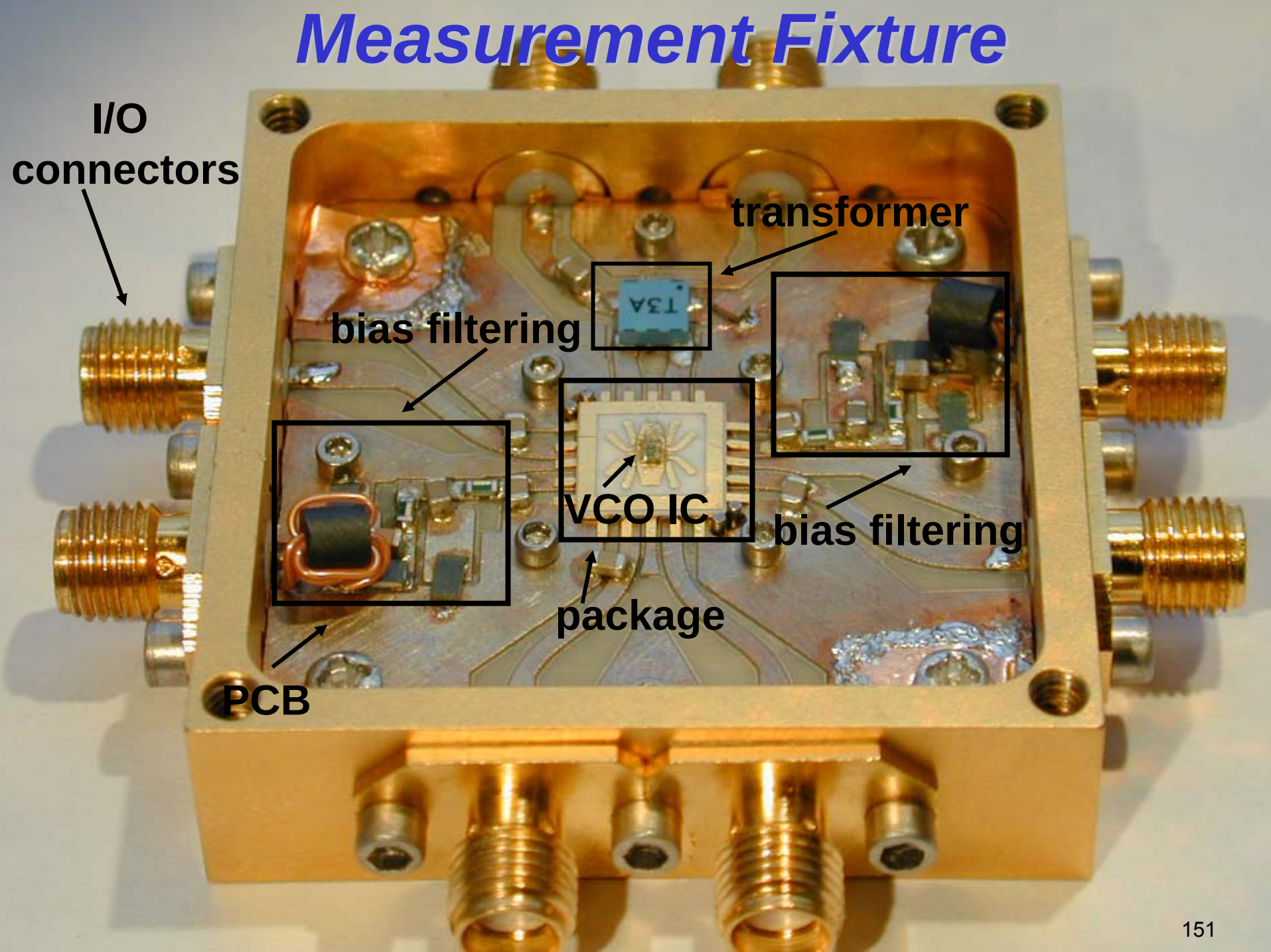
Packaged VCO IC



Packaged VCO IC on PCB

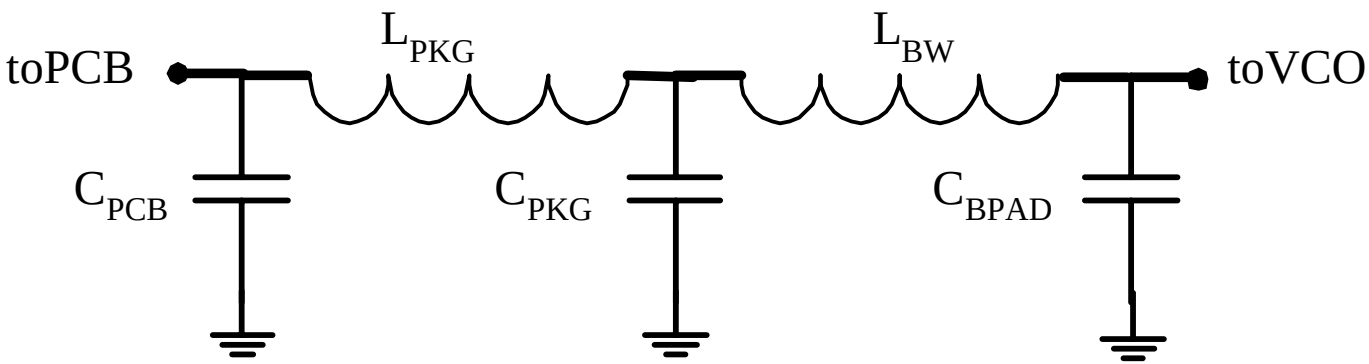


Measurement Fixture

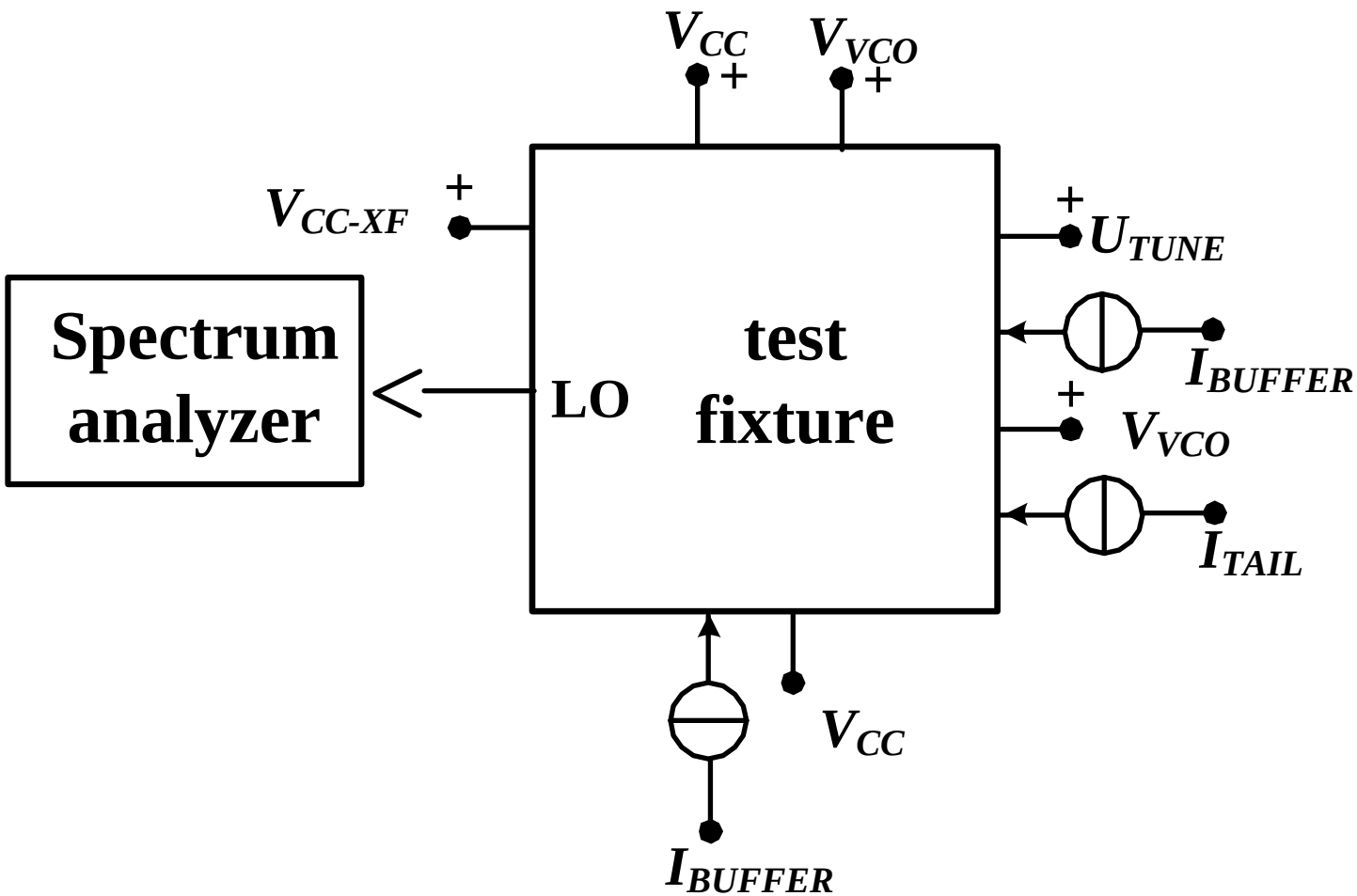


Package and PCB Effects

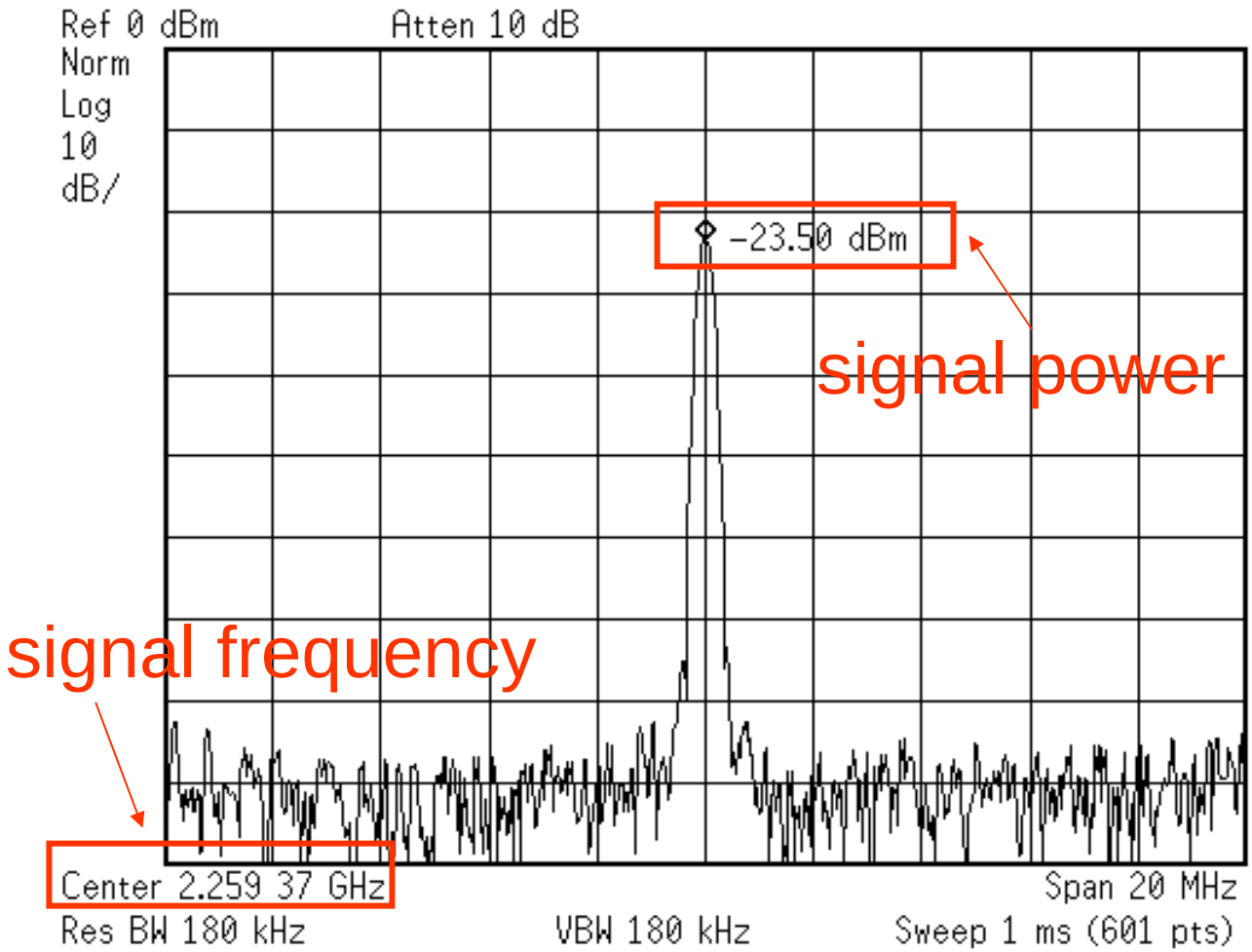
- Measured vs. simulated
- Include into simulations
  - bondwire inductance
  - package lead inductance
  - contact capacitances
  - SMD components on PCB
  - transmission lines on PCB



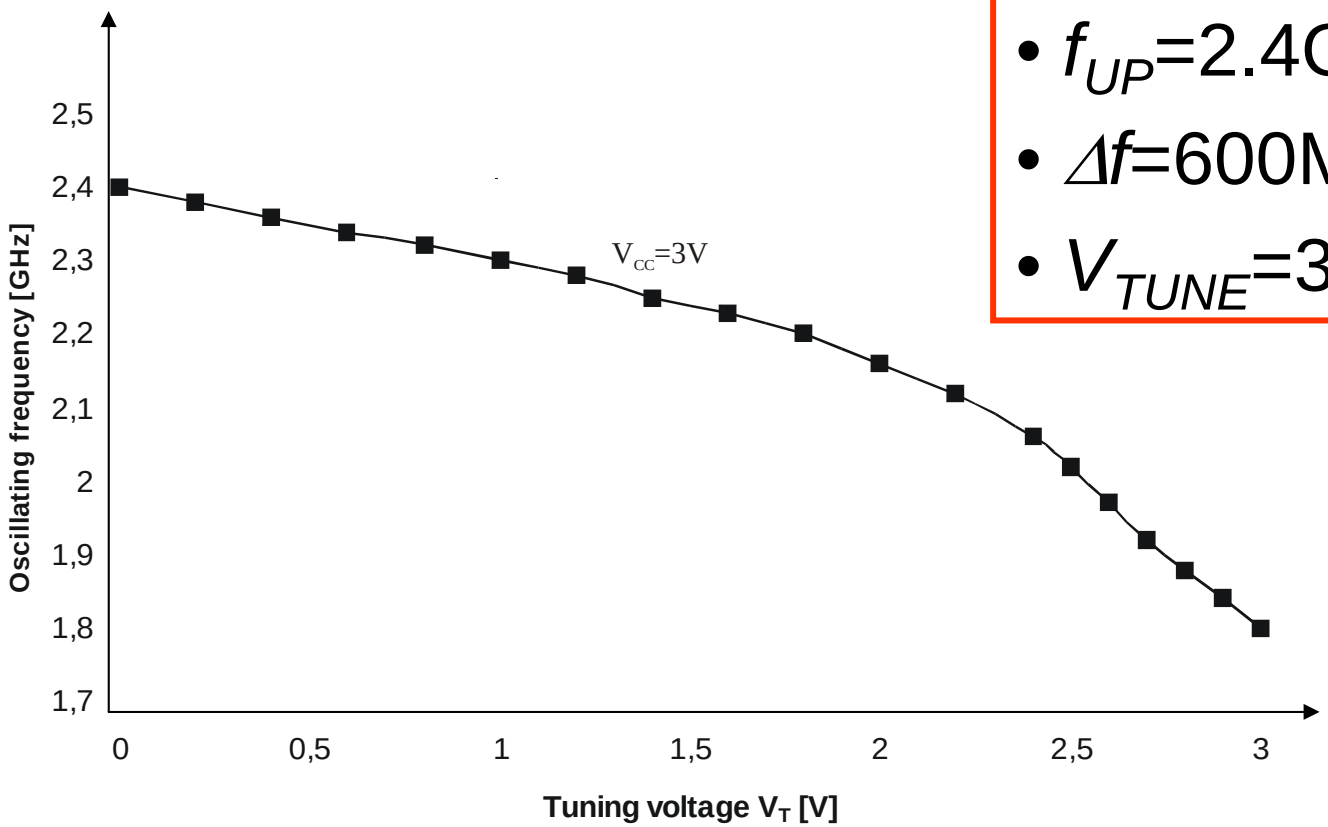
Measurement System



Measured Signal Spectrum

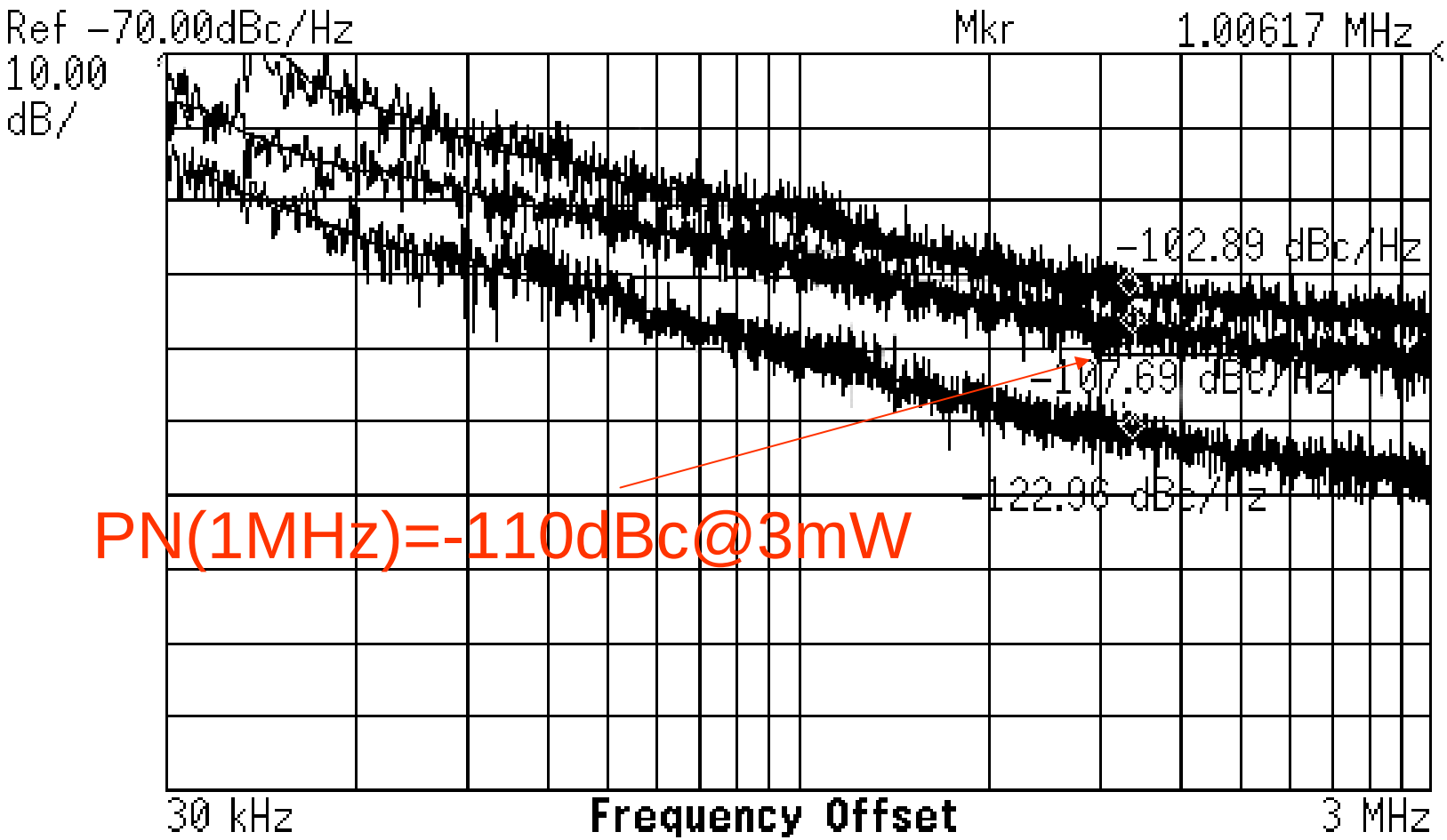


Measured Frequency Tuning Range



- f_{LOW}=1.8GHz
- f_{UP}=2.4GHz
- Δf=600MHz
- V_{TUNE}=3V

Measured Phase Noise



Measured VCO Performance

VCO design parameters	Measurement Results
Central frequency	2.1GHz
Tuning range	600MHz
Voltage swing	0.7V
Phase noise	-110dBc@1MHz
Supply voltage	3V
Power consumption	3mW

Conclusions

So far

- Oscillator classification
- Oscillation condition – frequency, amplitude
- Oscillator phase noise
- UMTS oscillator design – estimation, simulation, layout, measurements

Job Offer

- RF/analog circuits design experience
  - oscillators
- CAD design
  - Cadence, ADS
- Measurements and PCB design

- Salary 60.000