Et4054 Lab Session (1)

You start with a number (auto assigned) circuits:

.... using a dedicated MATLAB toolbox

investigate the circuits with respect to scheduling, retiming for minimum clock states, and resources i.e. a design space exploration

- Result => for each circuit a pareto points graph

Et4054 Lab Session (2)

For the to you assigned circuit (still with the aid of the MATLAB toolbox):

- For 3 different combinations of scheduling algorithms/resources/cycles do:
- generate and execute the MATLAB testbench,
- generate a VHDL testbench and simulate functional *and* timing behavior with Model*Sim*
- Check if simulations are successful
- Create a pareto point graph for the used resources and cycle and check cycle time
  (info available in two files: mapped.mrp and routed.twr

Optional : synthesize the VHDL design using Synplify_Pro.

Toolbox written in MATLAB

- …. for scheduling (various scheduling methods, with/without resource constraints, resource latencies, etc)
- …. for retiming for minimum clock states,
- …. for obtaining Pareto points,
- …. for creating a MATLAB testbench and user-definable input sequences,
- …. for creating a VHDL architecture description and testbench

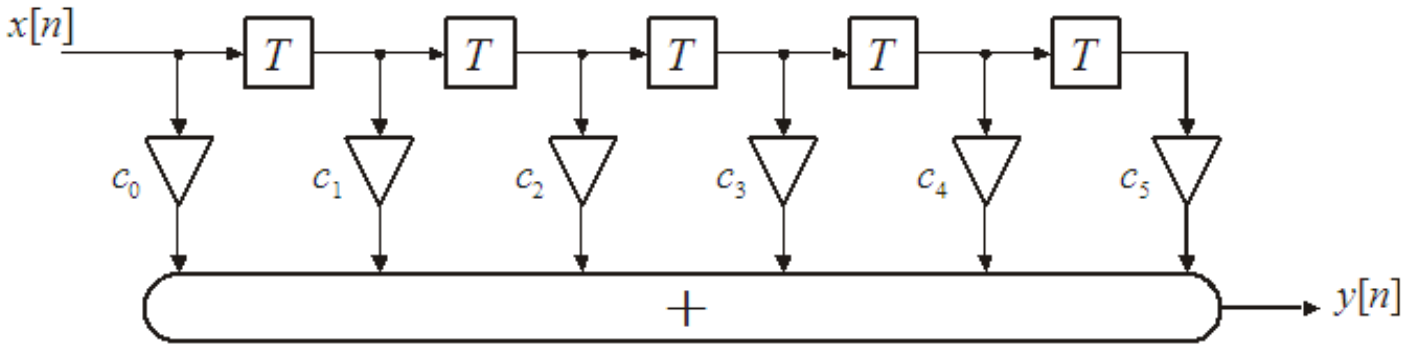

Figure 1.1 *Block diagram of a 5th order FIR filter.*

$$y[n] = \sum_{i=0}^{5} c_i \cdot x[n-i]$$

Table 1.1 *coefficients for the 5th order FIR filter*

c_0 =	-0.07556556070608
c_1 =	0.09129209297815
c_2 =	0.47697917208036
c_3 =	0.47697917208036
c_4 =	0.09129209297815
c_5 =	-0.07556556070608

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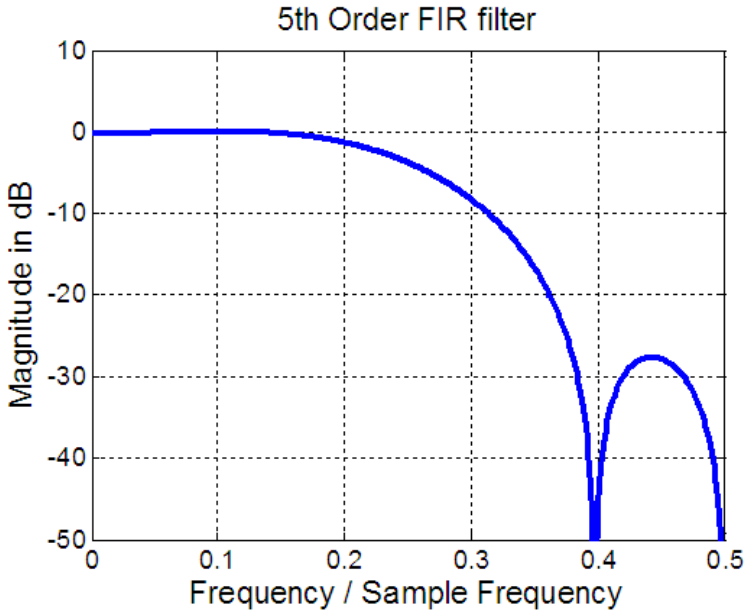
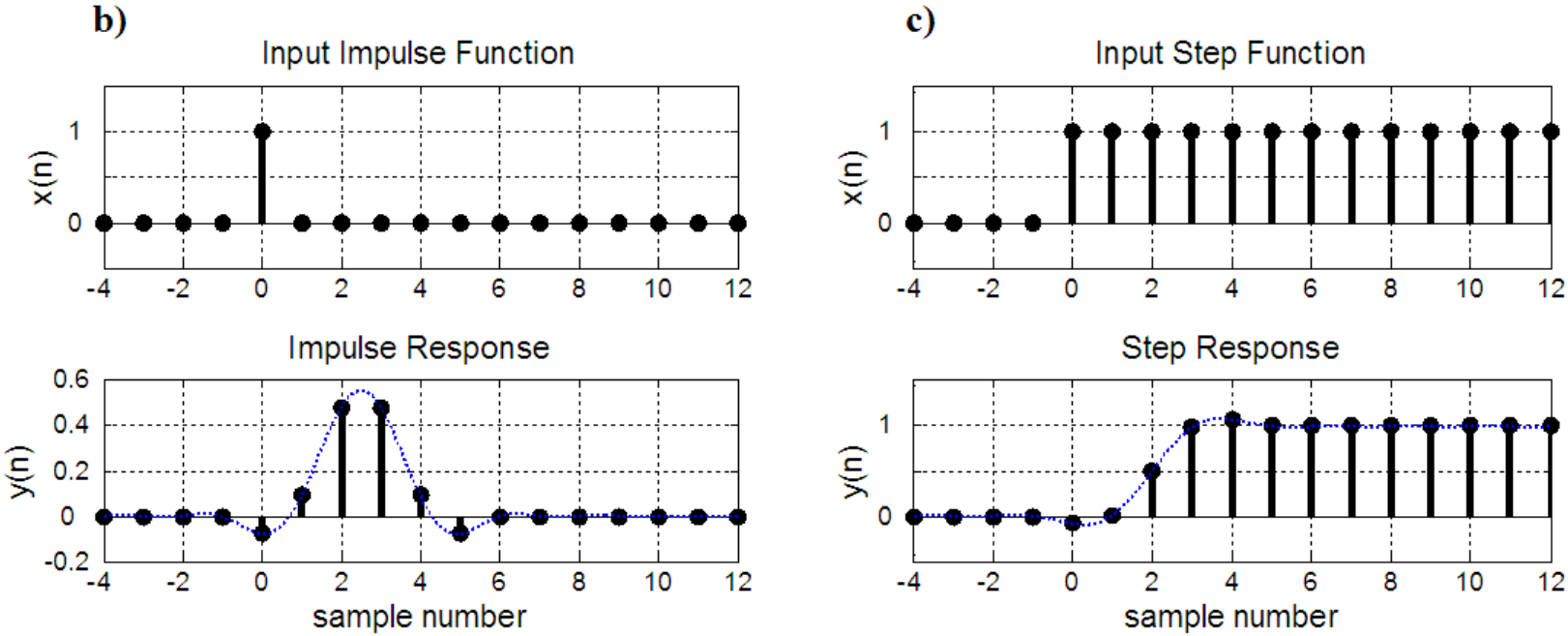


Figure 1.2a *Magnitude transfer function of the 5th order FIR filter.*



Figures 1.2 b and c. *Time response of the FIR filter with the magnitude transfer function given in Figure 2a. The lower plots show the output time samples* y[n] *for* **b)** *a unit impulse function as the input, and* **c)** *for a unit step function as input.*

- obtain a sequencing graph that can be scheduled,
- scheduling software to show the influence of a couple of different scheduling methods,
- retiming algorithm : schedule the resulting circuit description(s)
- MATLAB to verify the implementation which is derived from the scheduled graph (the SSG) in a fixed point environment,
- translate the scheduled circuit into a VHDL description,
- simulate this VHDL description using the Model*Sim* timing simulator

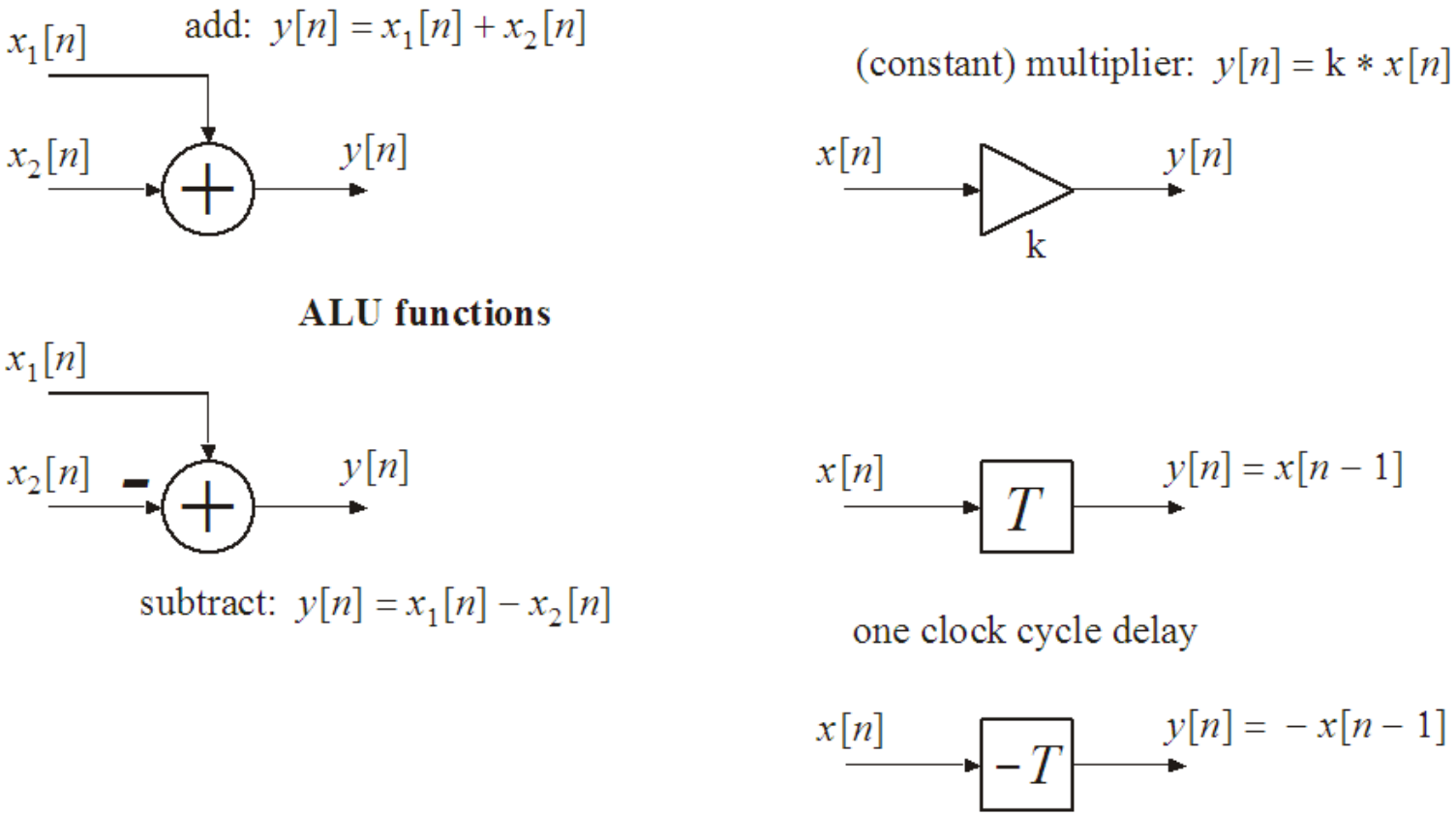
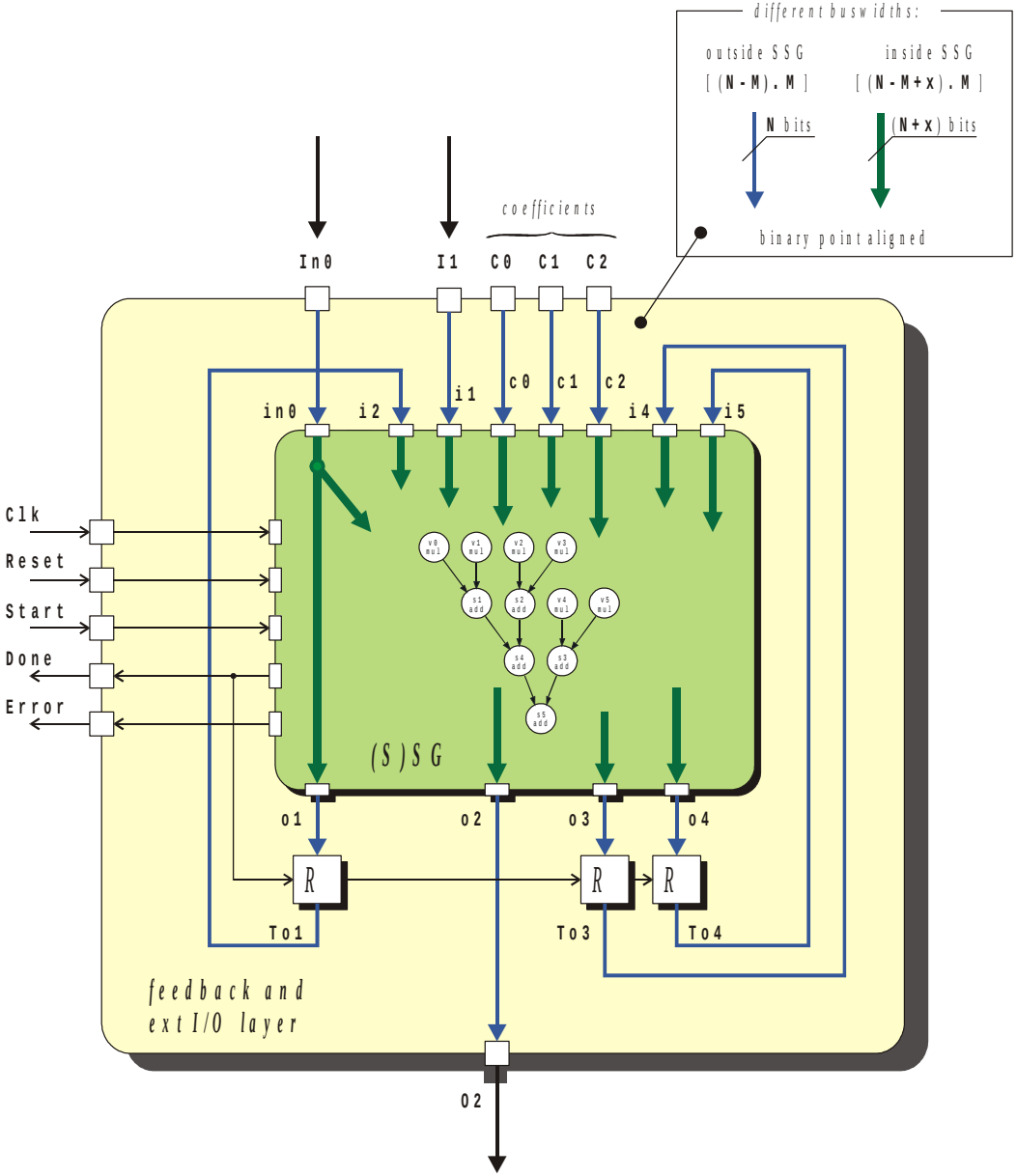


Figure 1.3 *Explanation of the available basis elements.*


different buswidths:
outside SSG
[(N-M).M]
inside SSG
[(N-M+x).M]
N bits
(N+x) bits
binary point aligned
coefficients
In0
I1
C0
C1
C2
in0
i2
i1
c0
c1
c2
i4
i5
Clk
Reset
Start
Done
Error
(S)SG
o1
o2
o3
o4
R
R
R
To1
To3
To4
feedback and
ext I/O layer
o2

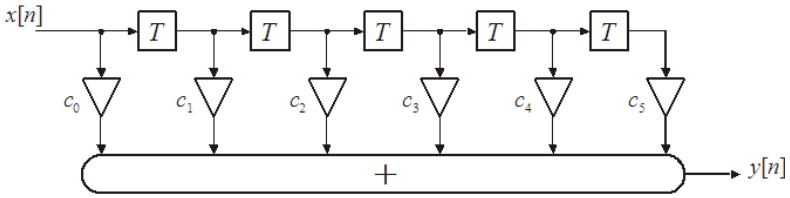


Figure 1.1 *Block diagram of a 5th order FIR filter.*

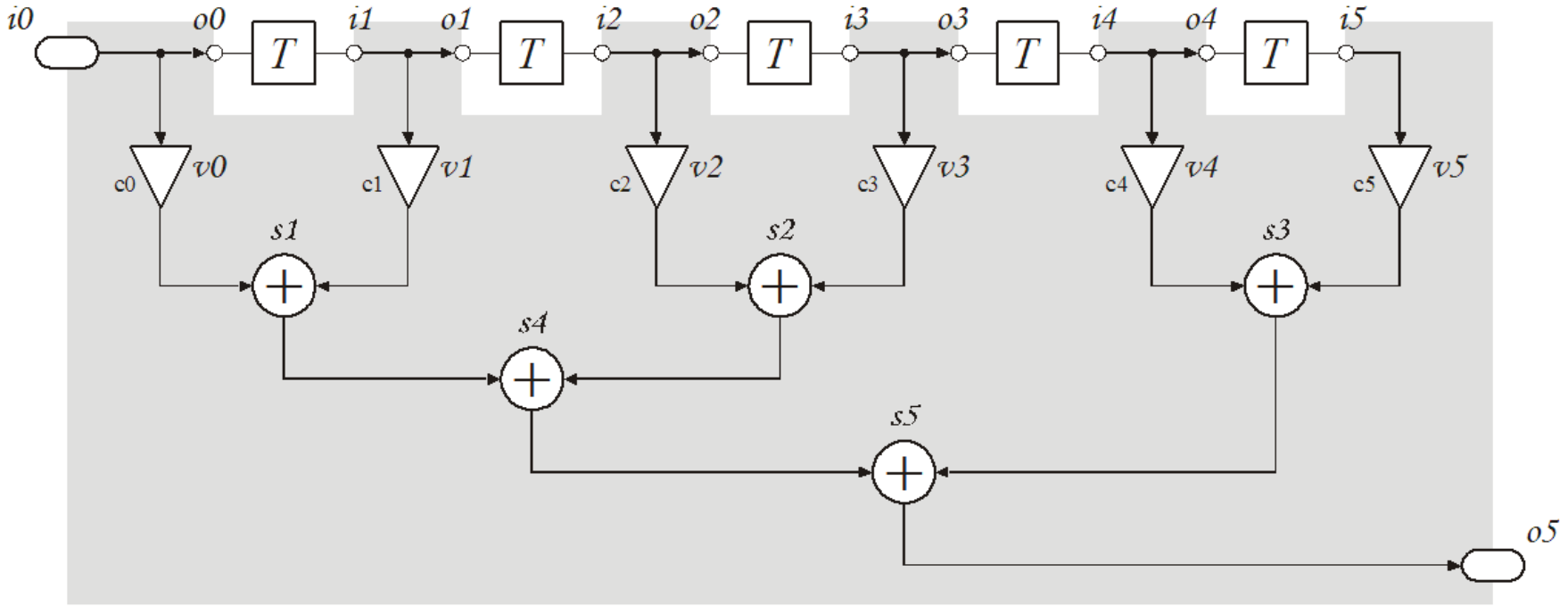


Figure 1.4 *Example of the labeling of the operations, inputs and outputs for the FIR5 filter.*

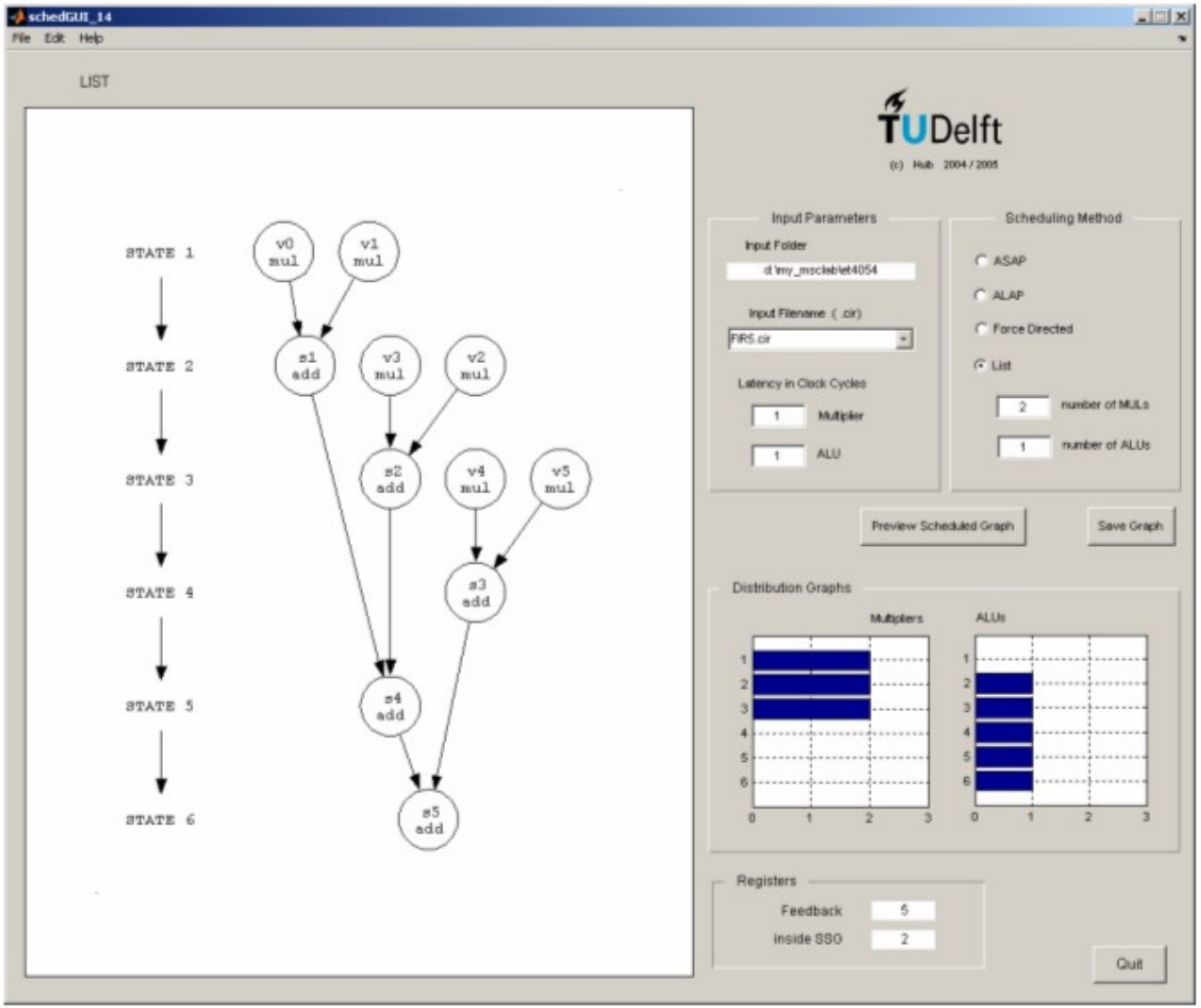


Figure 1.6 *Screenshot of schedGUI showing the Scheduled Sequencing Graph (SSG) for our FIR5 filter when a resource constrained List scheduling method has been applied.*

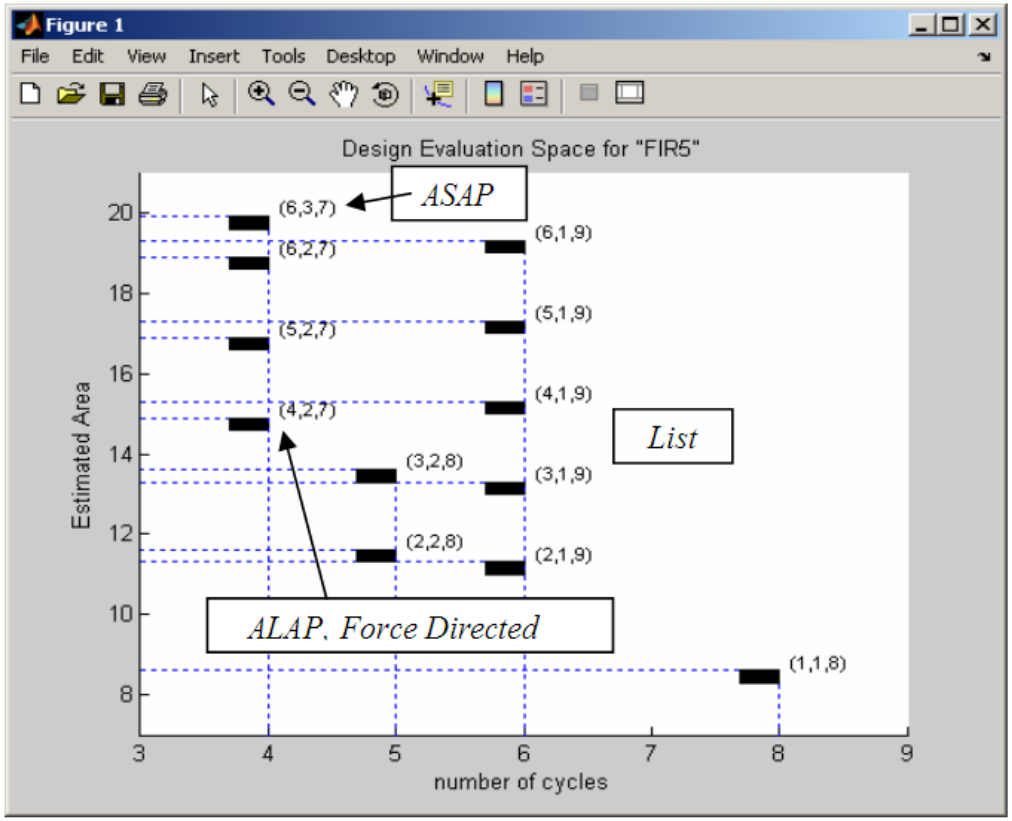
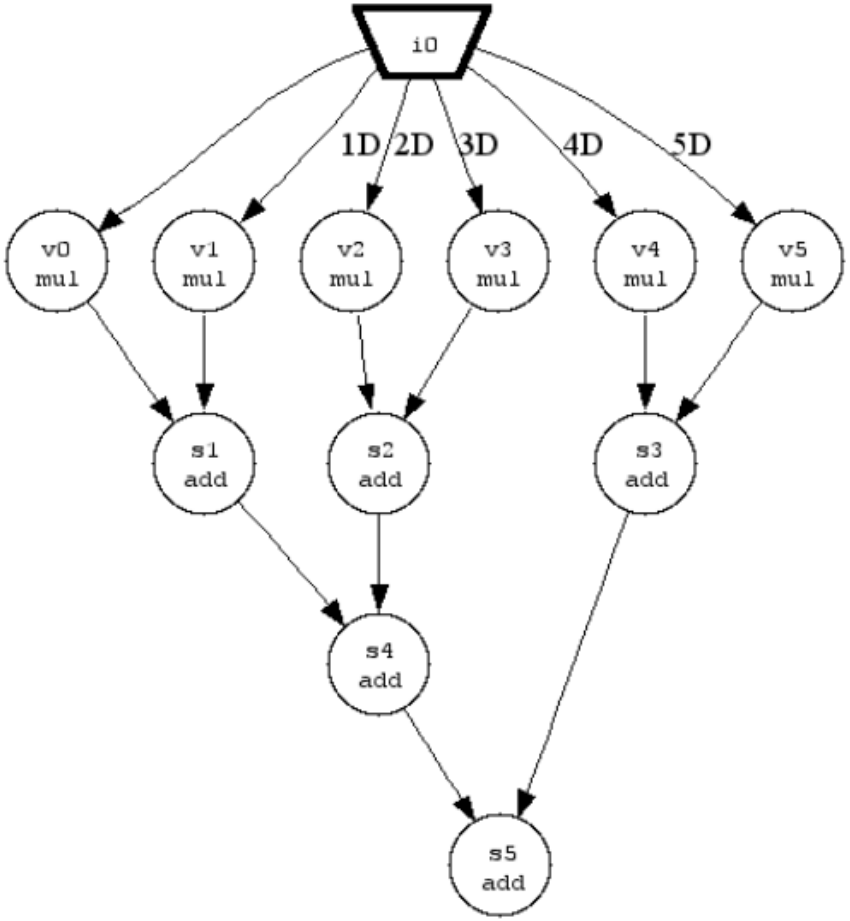
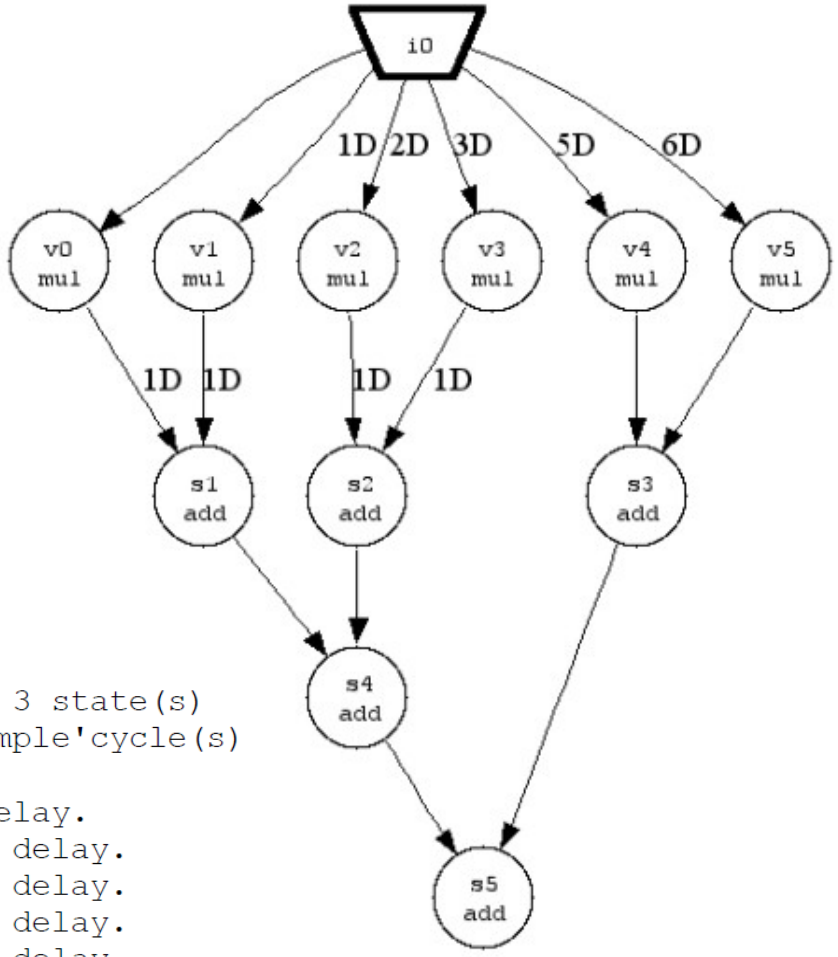


Figure 1.7 *Design space exploration for the FIR5 filter. It appears that –for this particular (, small) circuit– the schedules resulting from the ALAP and the Force Directed methods are exactly the same.*

Figure 1.7 shows the results of executing `xplore('FIR5.cir',[ 2; 1; 0.7 ])`.

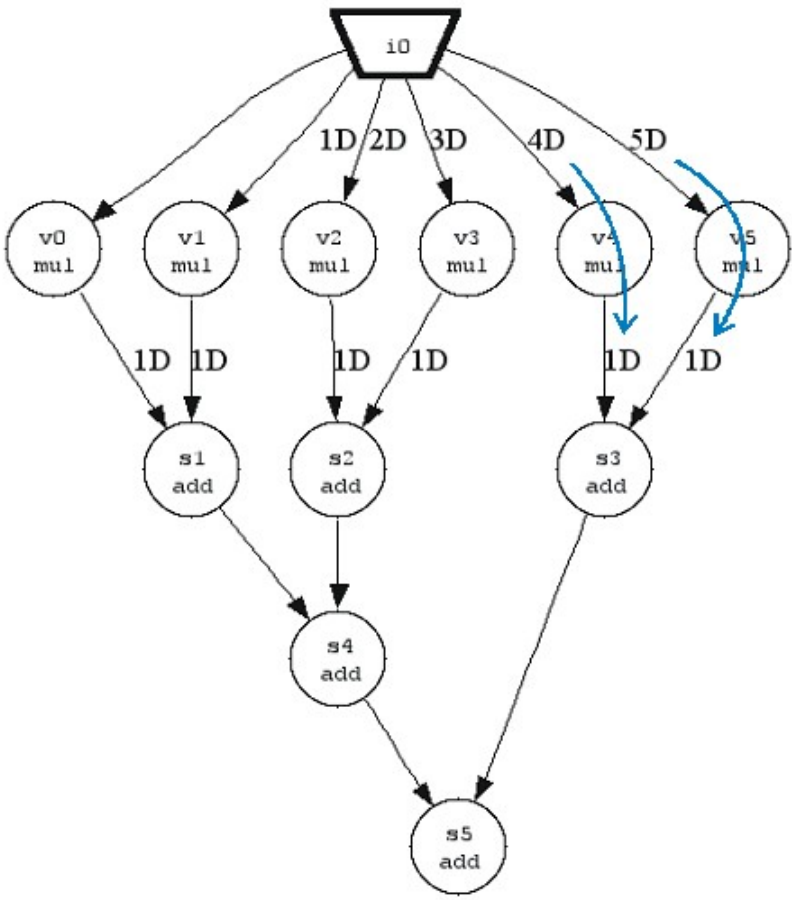
Data-flow graph obtained with `view_DFG('FIR5.cir')`.
*A '***D***' represents a Delay Element;* **5D** *means 5 consecutive delays.*






```
Retiming possible to decrease longest path to 3 state(s)
NOTE: Output will be delayed 1 additional 'sample'cycle(s)
Actions needed:
    Change 1T delay from i3 to v4 into a 2T delay.
    Change connection from v0 to s1 into a 1T delay.
    Change connection from v1 to s1 into a 1T delay.
    Change connection from v2 to s2 into a 1T delay.
    Change connection from v3 to s2 into a 1T delay.

Created file 'FIR5_3cyc.cir' for this retimed circuit ...
```


i0
1D
2D
3D
4D
5D
v0 mul
v1 mul
v2 mul
v3 mul
v4 mul
v5 mul
1D
1D
1D
1D
1D
1D
s1 add
s2 add
s3 add
s4 add
s5 add

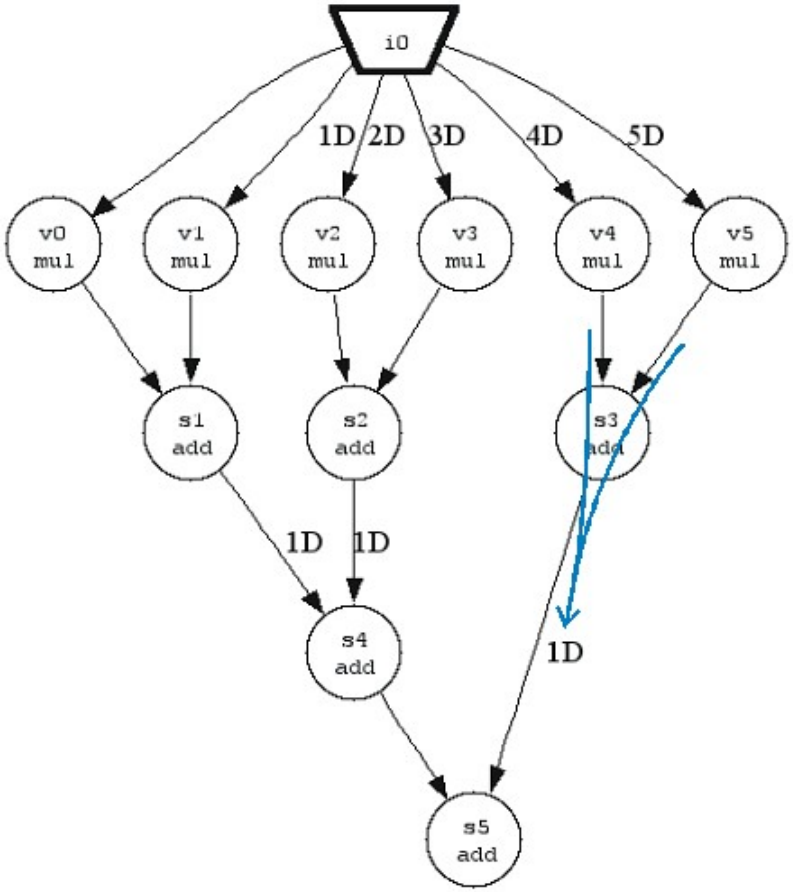

i0
1D
2D
3D
4D
5D
v0 mul
v1 mul
v2 mul
v3 mul
v4 mul
v5 mul
s1 add
s2 add
s3 add
1D
1D
1D
s4 add
s5 add

Table 1. *N-bits integer representations (2's complement for signed)*

	value	range
unsigned	$N_{UINT} = b_{N-1}2^{N-1} + b_{N-2}2^{N-2} + \cdots + b_1 s^1 + b_0 s^0$	$0 \le N_{UINT} \le 2^{N-1}$
signed	$N_{SINT} = -b_{N-1}2^{N-1} + b_{N-2}2^{N-2} + \cdots + b_1 s^1 + b_0 s^0$	$-2^{N-1} \le N_{SINT} \le \left(2^{N-1} - 1\right)$

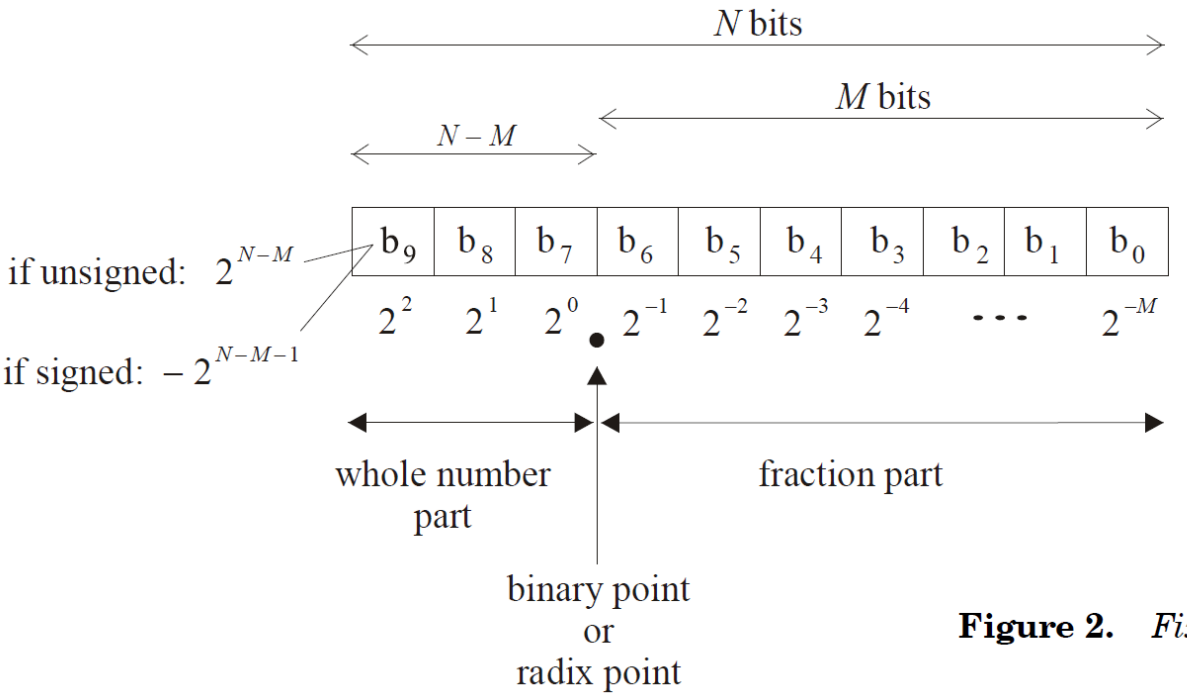
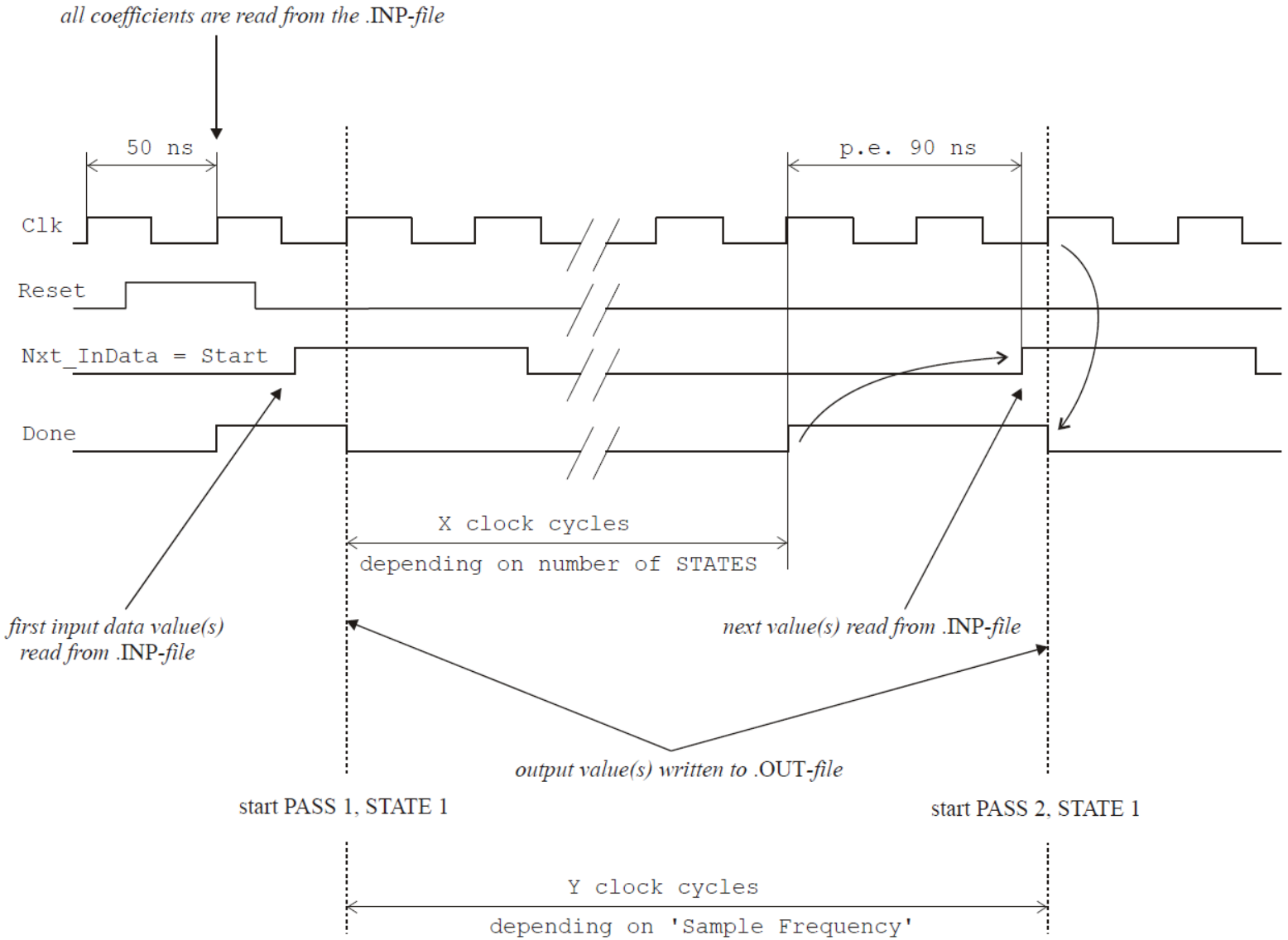
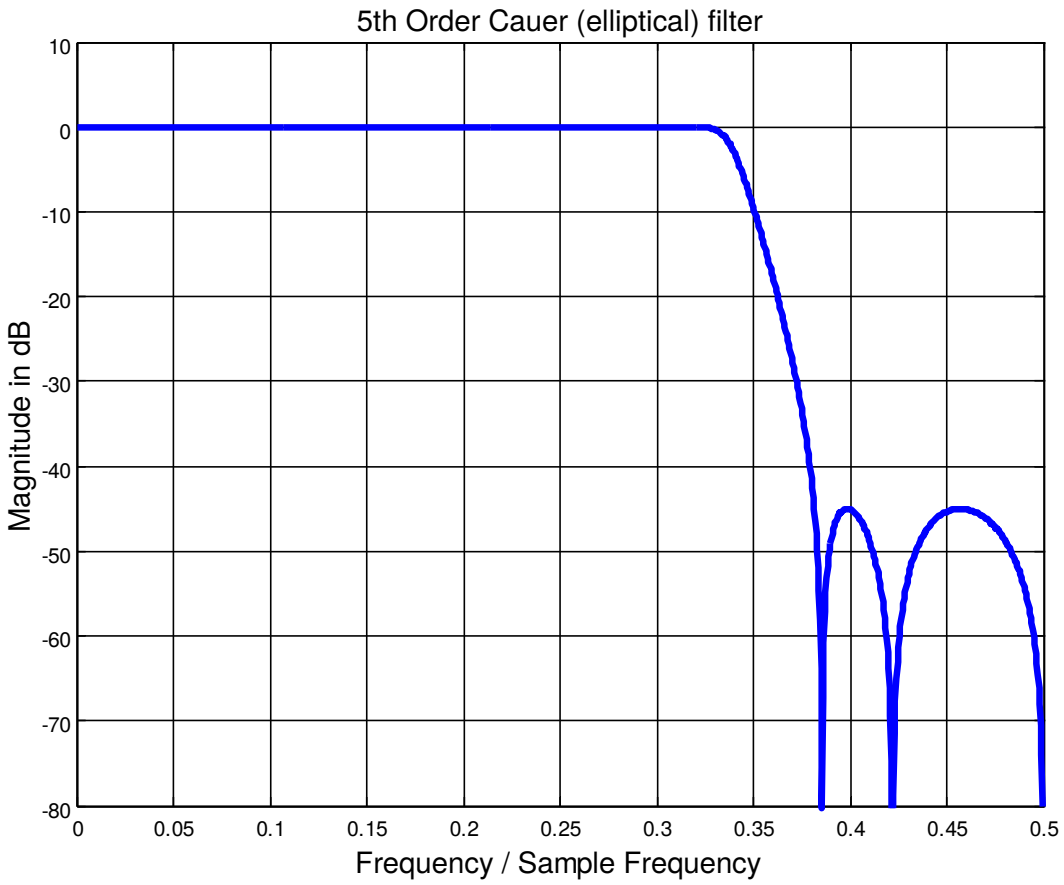
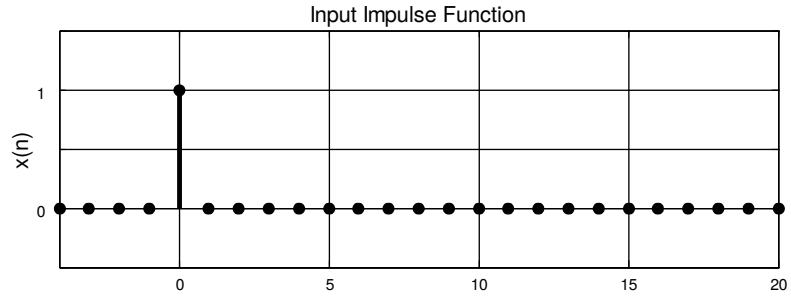
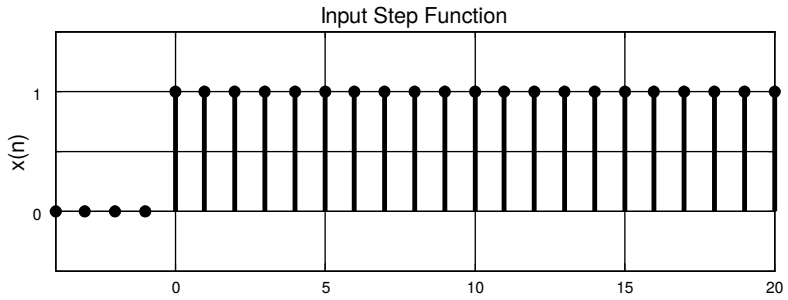


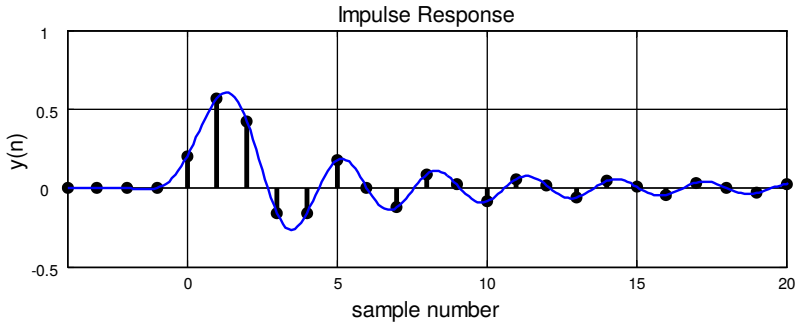
Figure 2. *Fixed-point notation.*

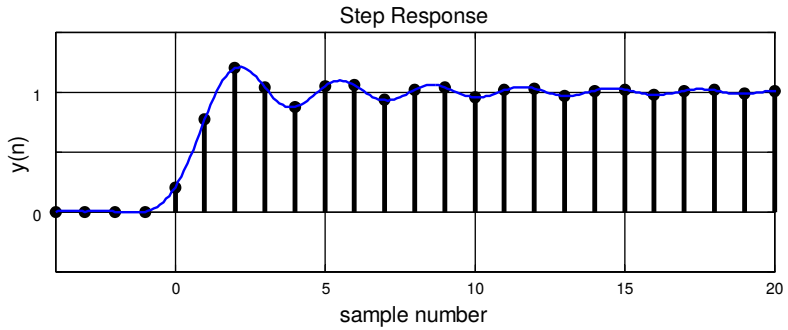

all coefficients are read from the .INP-file
50 ns
p.e. 90 ns
Clk
Reset
Nxt_InData = Start
Done
X clock cycles
depending on number of STATES
first input data value(s)
read from .INP-file
next value(s) read from .INP-file
output value(s) written to .OUT-file
start PASS 1, STATE 1
start PASS 2, STATE 1
Y clock cycles
depending on 'Sample Frequency'


5th Order Cauer (elliptical) filter
Magnitude in dB
Frequency / Sample Frequency
10
0
-10
-20
-30
-40
-50
-60
-70
-80
0
0.05
0.1
0.15
0.2
0.25
0.3
0.35
0.4
0.45
0.5


Input Impulse Function
x(n)
1
0
0
5
10
15
20


Input Step Function
x(n)
1
0
0
5
10
15
20


Impulse Response
y(n)
1
0.5
0
-0.5
0
5
10
15
20
sample number


Step Response
y(n)
1
0
0
5
10
15
20
sample number

Start-up

Login with your NetId

MATLAB, ModelSim, Xilinx ISE, Synplify_Pro

After starting MATLAB for the first time

folder ‘et4_054’ with all necessary data

file ‘ET4054_selection_for_<your NetId>’

(your personal selection for the assignment)

Note that you have to login and start/init MATLAB at least once to obtain your ‘personal selection’.

Start-up (2)

- 1) Desktop PC in lab:
  - After login, press start, select ‘matlab et4054’; you will find a icon in your desktop, called Et4054_selection _for….. that lists your 'personal assignment'.
- 2) Remote Desktop (commandline):
  - After command prompt type: % et4054_init, or % et4054_start