Lecture 8(2)

I_{DDQ} Current Testing

(Chapter 13)

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2009-2010

Learning aims

- Describe the concept of current testing IDDQ & its added value
- Describe the major faults and defects that can be detected by IDDQ
- Develop a vector for IDDQ
- State the major limitations of IDDQ and remedies

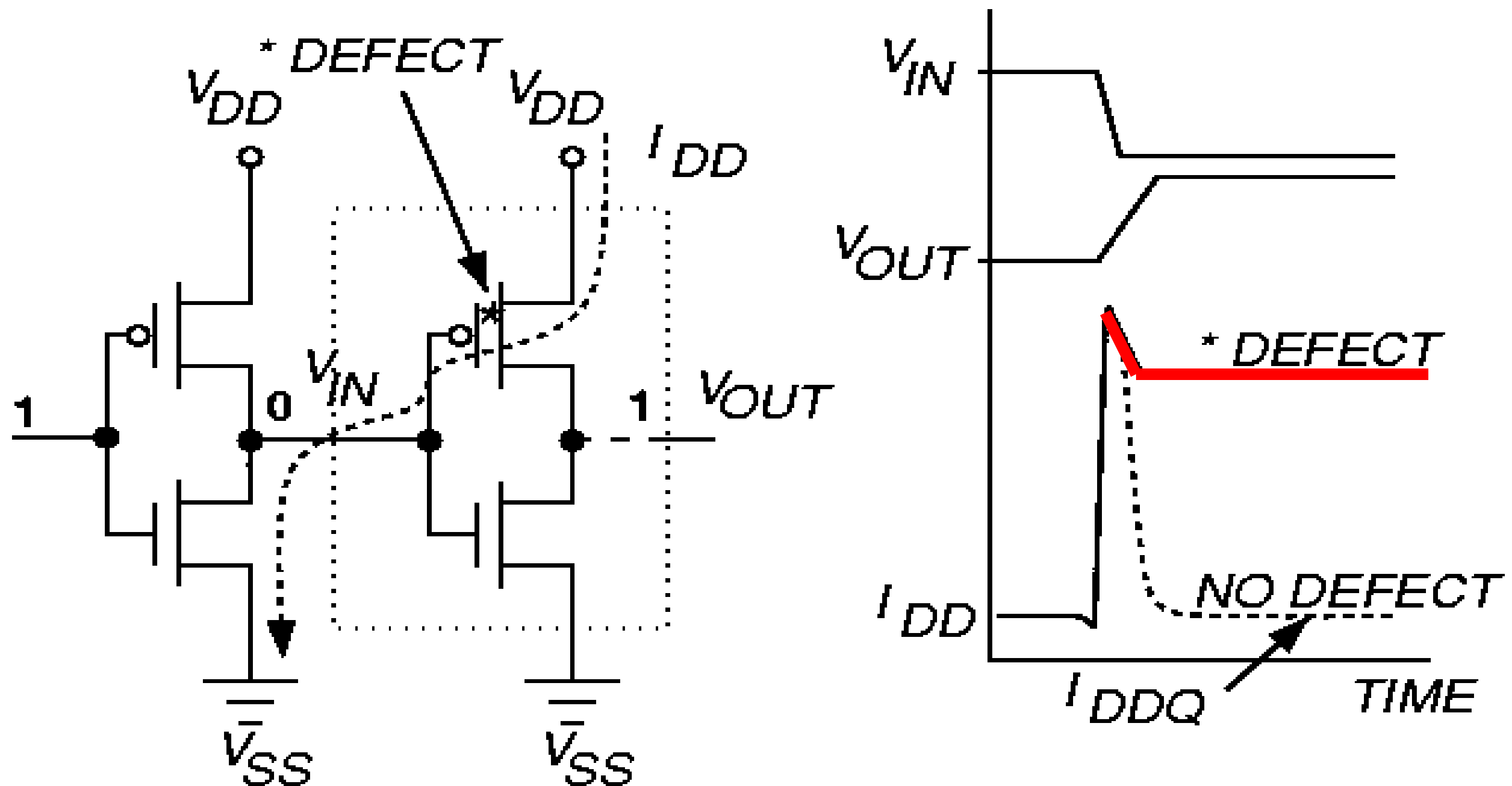
Contents

- Motivation
- IDDQ Test Concept
  - Pros and cons
  - Coverage
- Vector generation for *IDDQ* tests
- Instrumentation difficulties
- *IDDQ* testing effectiveness
- Limitations of *IDDQ* testing
- Delta IDDQ testing
- Built-in Current testing
- Summary

Motivation

- Early 1990's – Fabrication Line had 50 to 1000 *defects per million* (dpm) chips
  - IBM wants to get 3.4 *defects per million* (dpm) chips (0 defects, 6 σ)
- Conventional way to reduce defects:
  - Increasing test fault coverage
  - Increasing burn-in coverage
  - Increase *Electrostatic Discharge Damage* awareness
- New way to reduce defects:
  - I_{DDQ} Testing also useful for *Failure Analysis*

I_{DDQ} Test Concept



- In a good circuit, IDDQ (Quiescent current) is negligible
- In a faulty circuit, IDDQ remain elevated after switching
- Measure I_{DDQ} current through V_{SS} bus to detect the fault
  - Can also measured through the VDD bus
- ATE or "current measurement device" can perform measurements

I_{DDQ} Test .... + and -

- I_{DDQ} **measure** current: slow
- I_{DDQ} was used functional test, delay test, memory test, ..
- Used to improve the IC reliability, reduce manufacturing cost by 50%, improve filed quality, cut burn-in failures

- Problems
  - Feature size in the nano-era
  - Increase in leakage

I_{DDQ} Test coverage (1)

- IDDQ can detect many faults and defects:
  - Stuck at faults
  - Delay faults
  - Weak faults
  - Bridging faults
  - CMOS Stuck-Open faults
  - Leakage current
  - Floating gate defects
  - Gate Oxide Shorts
  - etc

I_{DDQ} Test coverage (2)

- **Stuck at faults**
  - Defects causing n and pFET transistors in a gate to be **on**
  - *Bridging faults* with stuck-at fault behavior

- **Delay faults**
  - Most random CMOS defects cause a timing delay fault, not catastrophic failure
  - Many delay faults detected by I_{DDQ} test – late switching of logic gates keeps I_{DDQ} elevated
  - Delay faults not detected by I_{DDQ} test
    - Resistive via fault in interconnect
    - Increased transistor threshold voltage fault

I_{DDQ} Test coverage (3)

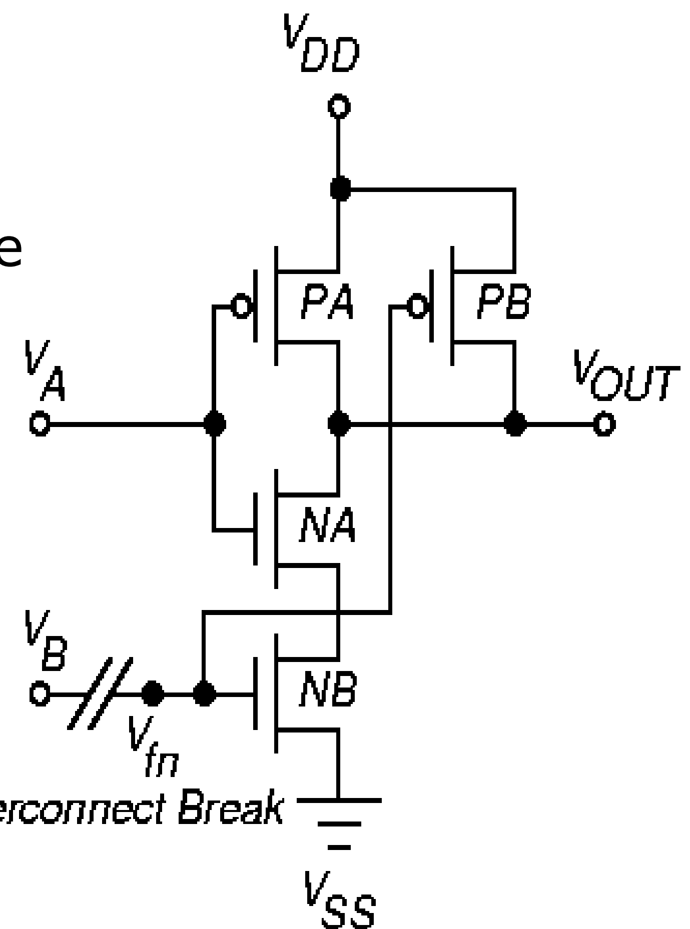
- **Weak faults**
  - *n*FET passes logic 1 as Vdd – V_{tn}
  - *p*FET passes logic 0 as 0 V + $|V_{tp}|$
  - Weak fault: transistor not fully turn on, so the signal passed is degraded
    - Increased propagation delay
    - Increases noises
- **CMOS Stuck-Open faults**
  - 100% detection not guaranteed
  - But work good in practice
    - Intermediate voltage of floating gate, hence high IDDQ

I_{DDQ} Test coverage (4)

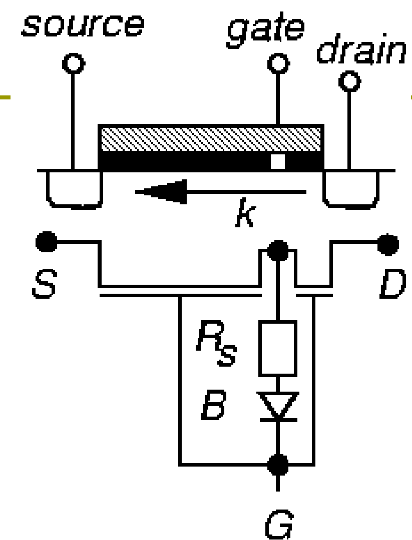
Floating gate defects

- V_{fn} voltage depends on the defect size
  - Small defect (100 – 200 Angstroms)
    - Coupling between the two wires
    - Delay fault
    - Weak voltage at the defective node
    - Detected with IDDQ
  - Large open
    - Floating gate
    - Stuck at fault?
    - Sometime can be detected
      - If $V_{tn} < V_{fn} < V_{DD} - |V_{tp}|$

NAND Gate

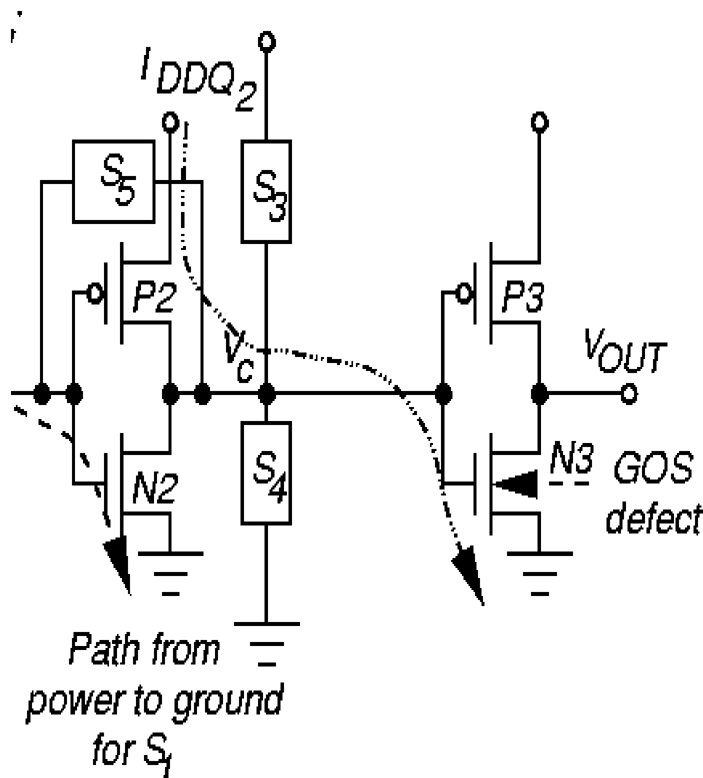


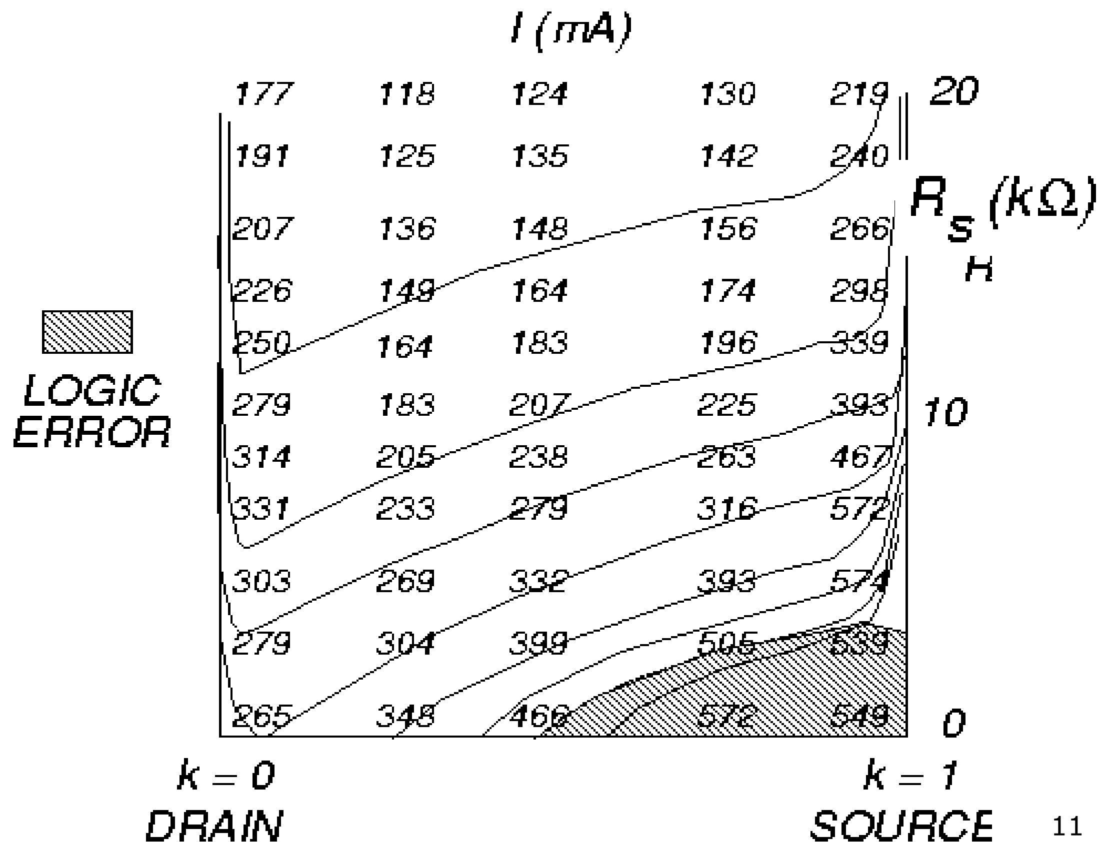
I_{DDQ} Test coverage (5)



Gate Oxide Short

- Gate no longer isolated from the channel
- Undesired current path the gate oxide
- I_{DDQ2} current results show 3 or 4 orders of magnitude elevation
  - In the good circuit, IDDQ2 current is 10 to 30 *nA.*





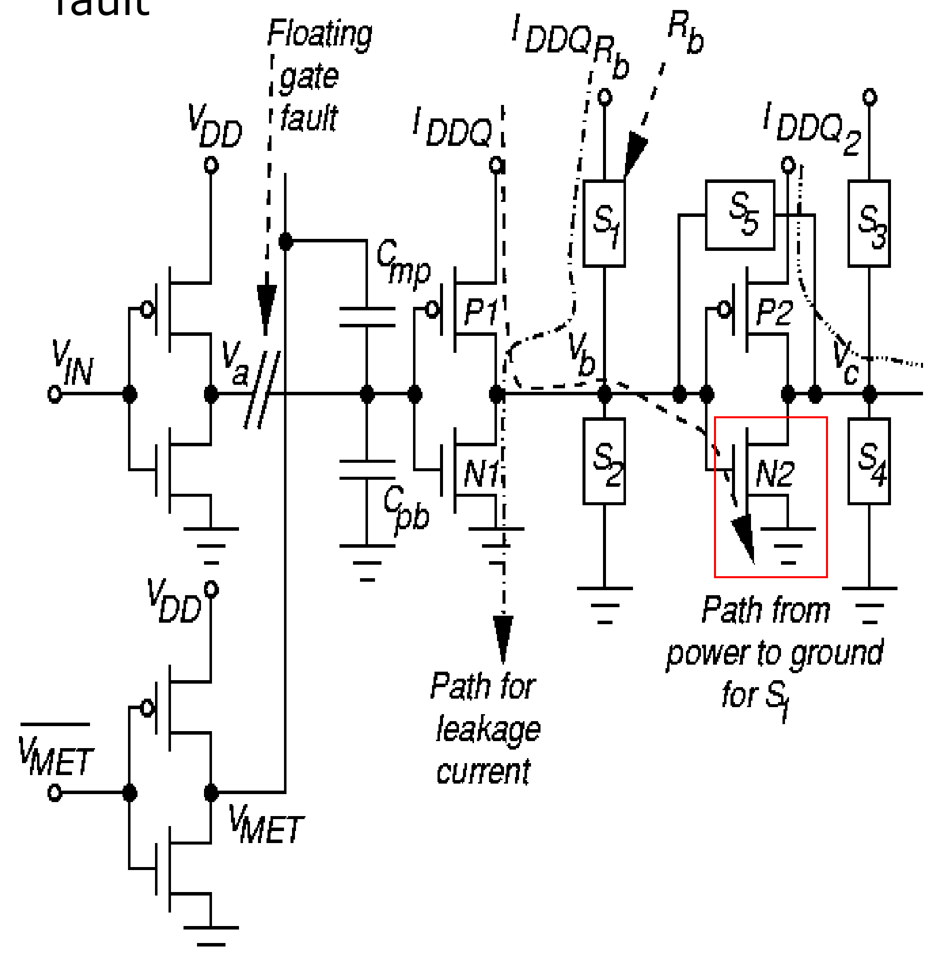
Vector generation for I_{DDQ} tests (1)

Leakage Fault Detection

[Mao and Gulati]

- Sensitize *leakage fault*
- Detection – 2 transistor terminals with leakage must have opposite logic values, & be at driving strengths
- Non-driving, high-impedance states won't work – current cannot go through them

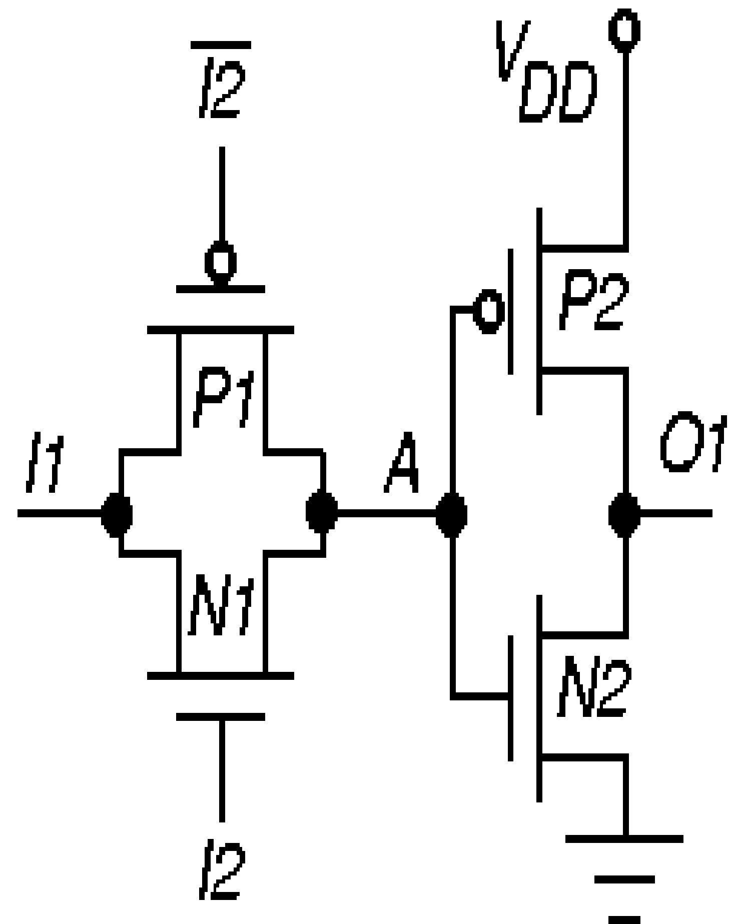
- N2 with **gate-source** leakage
- Detection requires Vb=1 and VIN=1
- This create the leakage through the fault



Vector generation for I_{DDQ} tests (2)

Weak Fault Detection – P1 (N1) Open

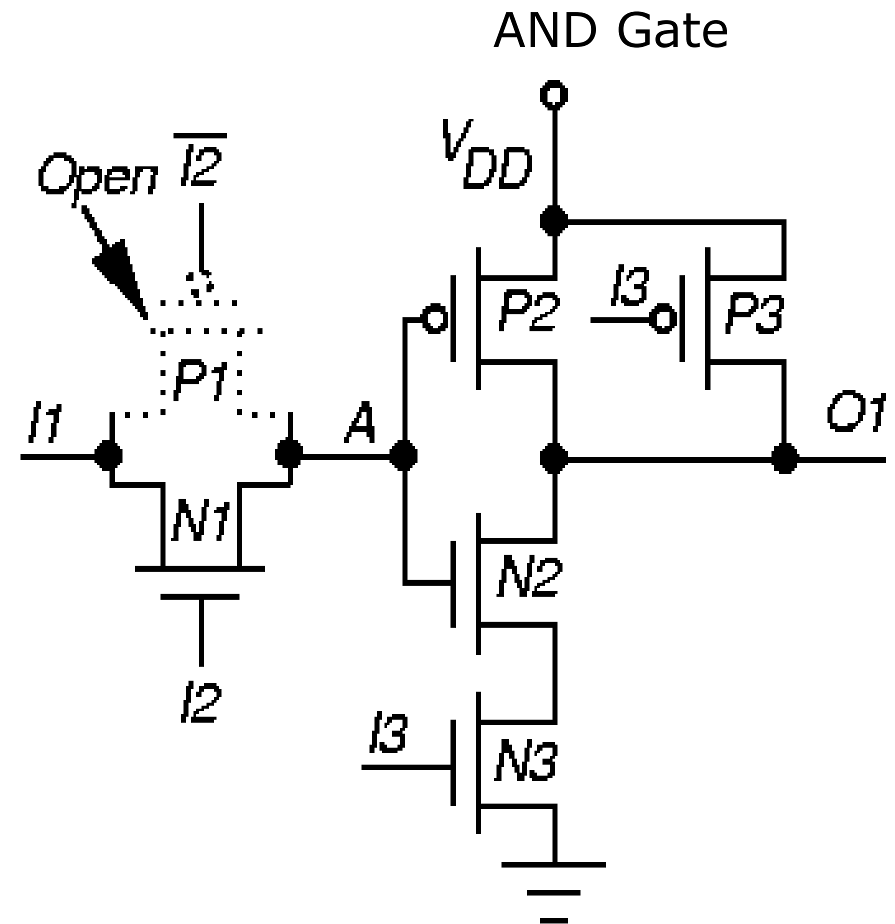
- P1(N1) degrades the input voltage
- Both transistors of inverter remain partially turned on
- Elevating I_{DDQ} from 0 μA to 56 μA



Vector generation for I_{DDQ} tests (3)

Weak Fault Detection – P1 Open

- P1 degrades the input voltage
- IDDQ will be not elevated unless I3 is set to 1
- No IDDQ path can exist if I3=0



Vector generation for I_{DDQ} tests (4)

Hierarchical Vector Selection

- Generate complete stuck-fault tests
- Characterize each logic component – relate input/output logic values & internal states:
  - To leakage fault detection
  - To weak fault sensitization/propagation
  - Uses switch-level simulation (once for each component)
- Store information in ***leakage & weak fault tables***
- Logic simulate stuck-fault tests – use tables to find faults detected by each vector
  - No more switch-level simulation

Vector generation for I_{DDQ} tests (5)

Leakage Fault Table

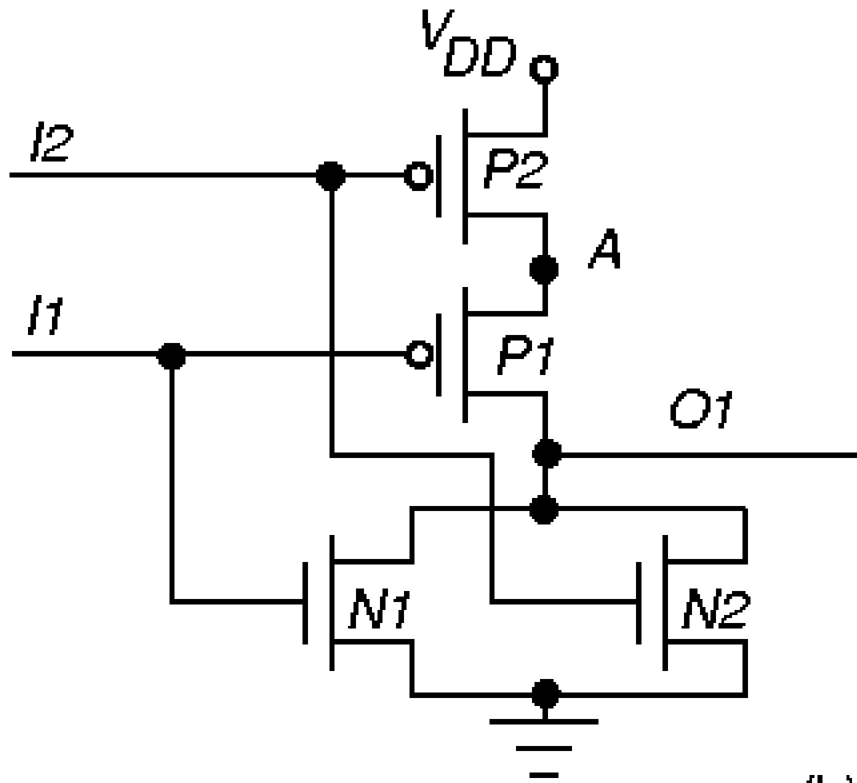
- k = # component I/O pins
- n = # component transistors
- $m = 2^k$ (# of input / output combinations)
- m x n matrix M represents the table
- Each logic state – 1 matrix row
- Entry $m_{i\,j}$ = **octal** leakage fault information
  - 6 Flags f_{BG} f_{BD} f_{BS} f_{SD} f_{GD} f_{GS}
  - Sub-entry $\boldsymbol{m_{i\,j}}$ **= 1 if leakage fault detected**

Vector generation for I_{DDQ} tests (6)

Leakage Fault Table: Example

k=3, n=4

m= 2^k =8; mxn=8x4



(a) Logic circuit.

NOR Gate

I_1	I_2	O_1	A
0	0	1	1
0	1	0	0
1	0	0	1
1	1	0	Z

(b) Logic simulation.

n

i	N_1	N_2	P_1	P_2
0	0	0	0	0
1	26	26	43	43
2	0	43	70	26
3	0	0	0	0
4	43	0	26	43
5	0	0	0	0
6	43	43	22	0
7	0	0	0	0

m

(c) Leakage fault table.

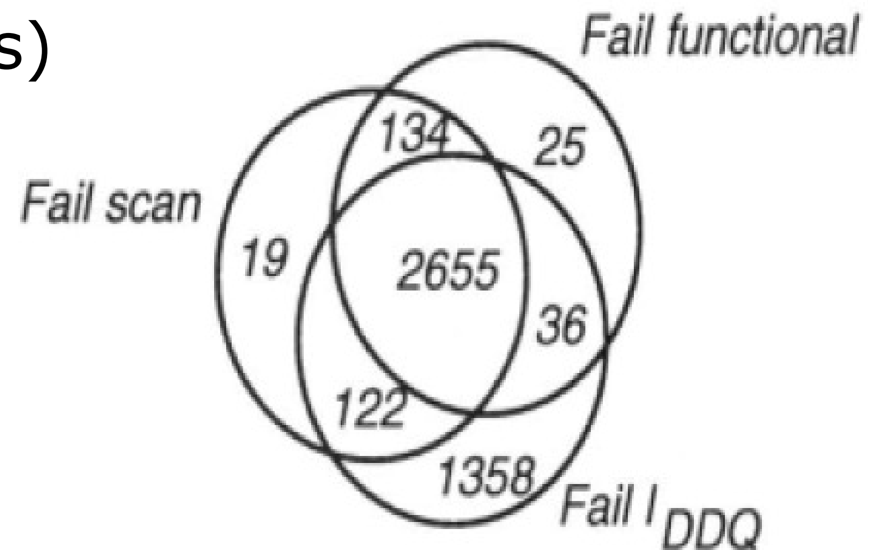
1	0	0 | 0	**1**	**1**
f_{BG}	f_{BD}	f_{BS} f_{SD}	f_{GD}	f_{GS}

Instrumentation difficulties

- Need to measure < 1 μA current at clock > 10 kHz
- Off-chip I_{DDQ} measurements degraded
  - Pulse width of CMOS IC transient current
  - Impedance loading of tester probe
  - Current leakages in tester
  - High noise of tester load board
- Much slower rate of current measurement than voltage measurement

IDDQ testing effectiveness

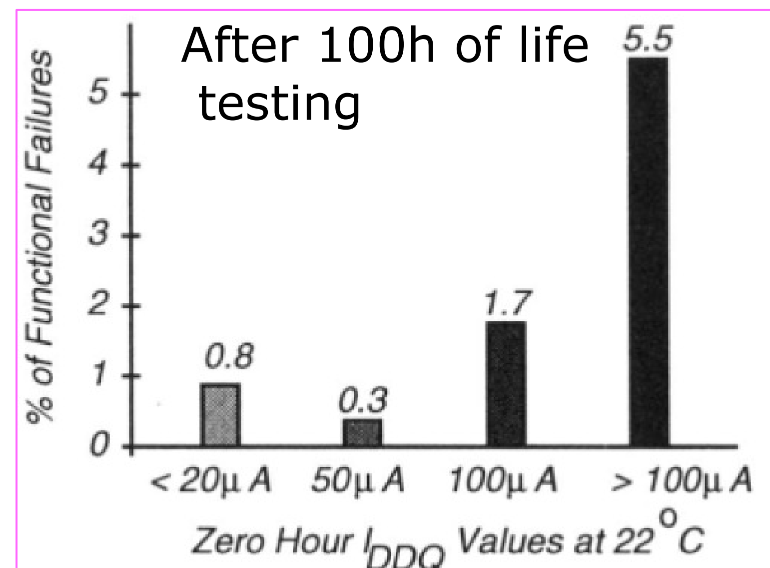
- HP static CMOS standard cell design
  (8577 gates and 436FFs)



- There is less correlation between IDDQ failures and voltage failures in general

- A mixture of testing methods is required to achieve a high product reliability

- IDDQ improve reliability



IDDQ testing effectiveness… Sematech Study(1)

- IBM Graphics controller chip – CMOS ASIC, 166,000 standard cells
- 0.8 μm static CMOS, 0.45 μm Transistors (L_{eff}), 40 to 50 MHz Clock, 3 metal layers, 2 clocks
- Full boundary scan on chip

- Tests:
  - Scan-based stuck-at faults (99.7% FC, slow 400ns rate)
  - Functional tests (design verification patterns;52% SAF FC; manually created)
  - Scan based delay fault test (90 % transition delay FC)
  - I_{DDQ} Tests (125) (96 % pseudo-stuck-at fault coverage).

IDDQ testing effectiveness… Sematech Study(2)

- Test process: Wafer Test →Package Test → Burn-In & Retest→ Characterize & Failure Analysis
- Data for devices failing some, but not all, tests.

***IDDQ* (5 μA limit)**

Scan-based Stuck-at	Pass	Pass	Fail	Fail	Scan-based delay
Pass		6	1463	7	Pass
Fail	14	0	34	1	Pass
Pass	6	1	13	8	Fail
Fail	52	36	1251		Fail
	Pass	Fail	Pass	Fail	

Functional

- **All test methods uniquely detected some defect class => none can be dropped from the test program**

IDDQ testing effectiveness… Sematech Study(3)

Sematech Conclusions:

- Hard to find point differentiating good and bad devices for I_{DDQ} & delay tests
- High # passed functional test, failed all others
- High # passed all tests, failed I_{DDQ} > 5 μA
- Large # passed stuck-at and functional tests
  - Failed delay & IDDQ tests
- Large # failed stuck-at & delay tests
  - Passed I_{DDQ} & functional tests
- Delay test caught delays in chips at higher temperature burn-in
  - chips passed at lower temperature

Limitations of I_{DDQ} Testing

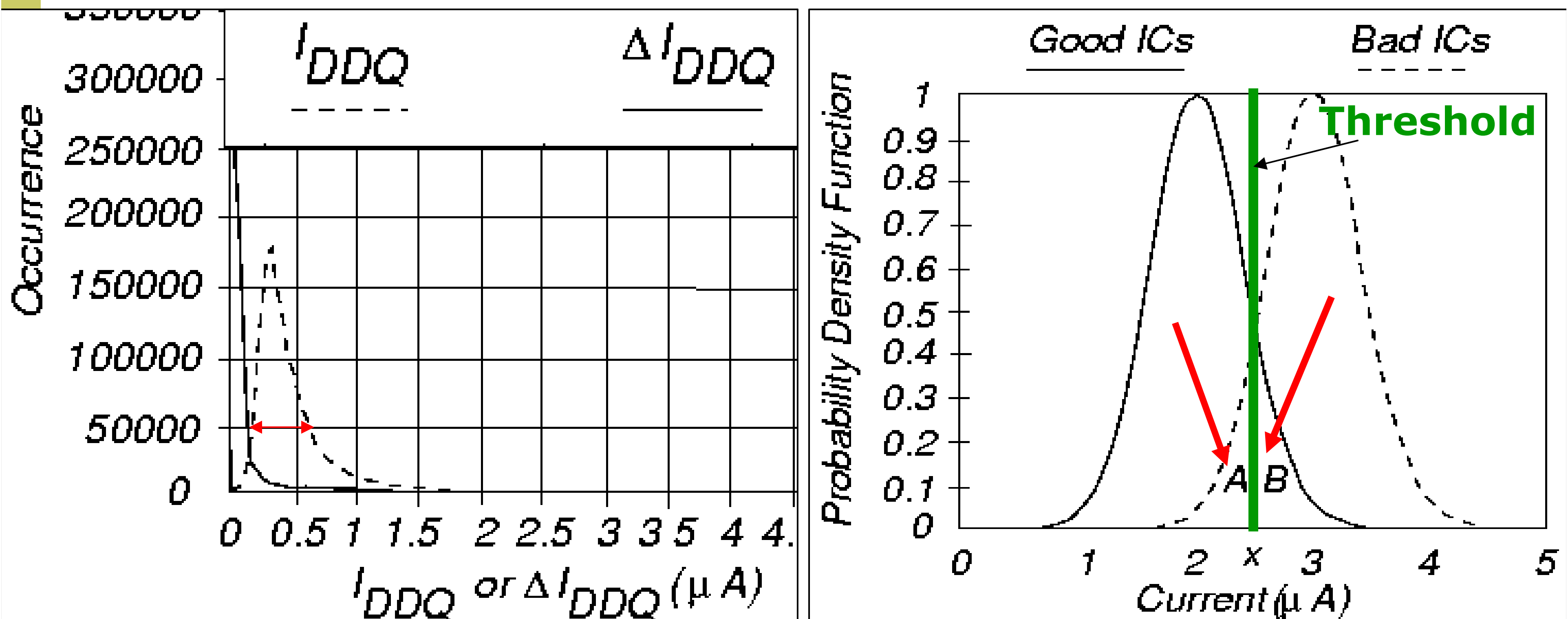
- Sub-micron technologies have increased leakage currents
  - Transistor sub-threshold conduction
  - Harder to find I_{DDQ} **threshold** separating good & bad chips
- I_{DDQ} tests work:
  1. When average defect-induced current greater than average good IC current
  2. Small variation in I_{DDQ} over test sequence & between chips
     - Detect passive defects and active defects simultaneously
- Now less likely to obtain two conditions (scaling)
  - Some predict the end of IDDQ testing

Delta I_{DDQ} Testing…… [Thibeault]

- Use derivative of I_{DDQ} at test vector as current signature

$$\Delta I_{DDQ}(i) = I_{DDQ}(i) - I_{DDQ}(i-1)$$

- Leads to a narrower histogram
- Eliminates any variation between chips (wafers)



Delta I_{DDQ} Testing…… Results

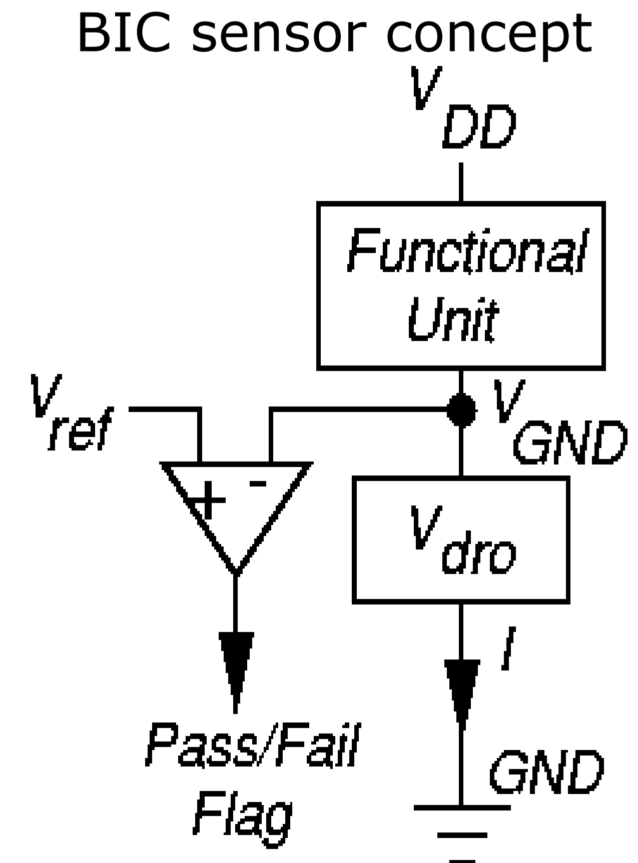
- **ΔI_{DDQ} Testing versus I_{DDQ} testing Results**
  - P: probability of a false decision
- ΔI_{DDQ} eliminates any constant (vector-insensitive) current increase due to process drift by differential operation
  - But process drift may still increases the measurement variations between vectors

Item	**I_{DDQ}**	**ΔI_{DDQ}**
RYL (yield loss ratio)	4.4e-4	3.5e-3
RTE (test escape ratio)	1.8e-1	2.1e-3
P (= *RYL* + *RTE*)	*Piddq* = 1.8e-1	*Pdelta* = 5.6e-3
Gain in test quality	*Piddq* / *Pdelta* = 31	

Built-in Current Testing…. [Maly and Nigh]

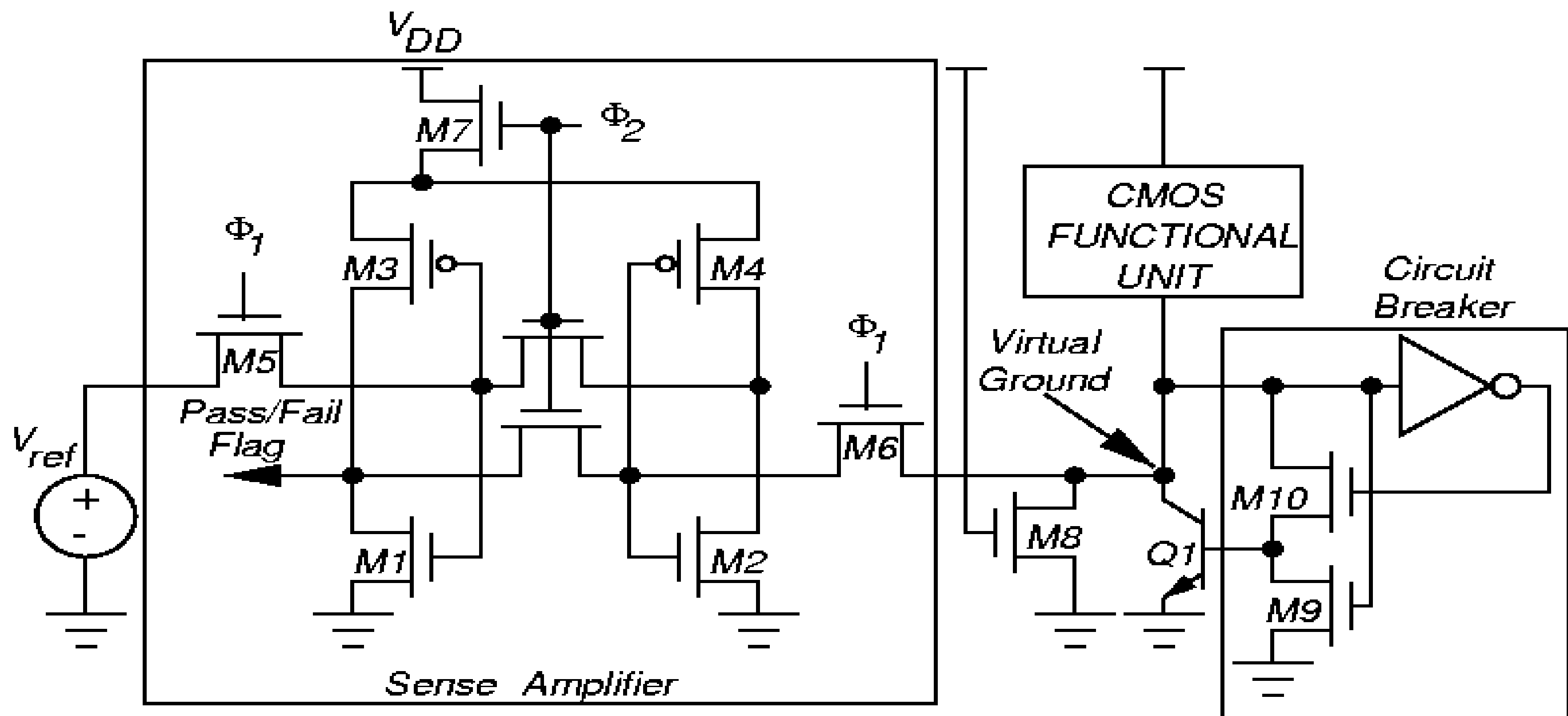
- Build current sensor into ground bus of device-under-test
- Voltage drop device (V_{dro})& comparator
  - Compares virtual ground V_{GND} with V_{ref} at end of each clock
    - $V_{GND} > V_{ref}$ only in bad circuits
  - Activates circuit breaker when bad device found

BIC sensor concept



Built-in Current Testing…. Example

- A **bipolar transistor** is used to get better resolution for current detection
- Circuit Breaker disconnect the defective functional unit from power when abnormal currents occur (e.g., due to VDD-GND shorts)



Summary

- I_{DDQ} tests improve reliability, find defects causing:
  - Delay, bridging, weak faults
  - Chips damaged by electro-static discharge
- No natural breakpoint for current threshold
  - Get continuous distribution – bimodal would be better
- Conclusion: now need stuck-fault, I_{DDQ}, and delay fault testing combined
- I_{DDQ} testing is becoming more problematic
  - Greater leakage currents in MOSFETs in deep sub-micron technologies
  - Harder to discriminate elevated I_{DDQ} from 100,000 transistor leakage currents
- ΔI_{DDQ} holds promise to alleviate problems
- Built-in current testing holds promise