VLSI Test Technology and Reliability (ET4076)

Lecture 9(1)

Digital DFT and Scan Design
(Chapter 14)

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Learning aims

- Explain the differences between Ad-hoc and structured DFT

- Describe Scan Design
  - concept/structure, advantages/disadvantages, etc

- Apply scan design to a sequential circuit and develop appropriate test patterns

- Describe Partial Scan
  - Concept/Motivation, test generation, Advantages versus disadvantages
Contents

- Introduction & Definition
- Ad-hoc methods
- Scan design
  - Concept, Structure, design and test procedure
  - Design rules, testing, observed
  - Hierarchical design, design automation, timing and power
- Partial-scan
  - Motivation, Definition, Architecture
  - Comparison, Test generation
- Variations of Scan
  - *Scan-hold flip-flop (SHFF)*
- Summary
Introduction & Definition (1)

- Three questions characterize complex system testing
  - Can tests that detect all faults assured?
  - Can test development time be kept within economical limits?
  - Can test execution time be kept within economical limits?

**Design for testability (DFT)** refers to design practices that help to answer these questions

- Electronic systems consists of different components
  - Digital logic
  - Memory blocks
  - Analog and mixed-signal blocks

  Each component requires specific DFT

- Component level-DFT are not sufficient for producing testable system
  - Access mechanism to the embedded component needed
Design for testability (DFT)

- refers to those design techniques that make test generation, test application and test evaluation cost-effective.

DFT methods for digital circuits:

- Ad-hoc methods
- Structured methods:
  - Scan
  - Partial Scan
  - Boundary scan
  - Built-in self-test (BIST)

DFT method for mixed-signal circuits:

- Analog test bus
Ad-Hoc DFT Methods

- Good design practices learnt through experience:
  - Partition large circuits into smaller subcircuits to reduce test generation cost
  - Avoid asynchronous (unclocked) feedback (e.g., oscillation).
  - Make flip-flops initializable.
  - Avoid large fanin gates (inputs/outputs difficult to observe/control).
  - Provide test control for difficult-to-control signals.
  - Avoid redundant gates.
  - Avoid gated clocks.
  - Consider ATE requirements (tristates, etc.)

- Design reviews conducted by experts or design auditing tools (testability measures)
  - Once problem found, either circuit modified or test point inserted

- Disadvantages of ad-hoc DFT methods:
  - Experts and tools not always available.
  - Test generation is often manual with no guarantee of high fault coverage.
  - Design iterations may be necessary.
Scan Design ....... Concept (1)

- **Main idea:**
  - obtain controllability & observability of FFs

- Add a test mode to the circuits
  - All FFs functionally form one or more shift registers
  - Inputs and output of these registers are made into PIs & POs
  - All FFs can be set to any desired state (by shifting in)
  - All states of FFs can be observed (by shifting out)
  - All FFs can be set/observed in “#FFs longest register” *CLK

- For the circuit to have scan capability
  - Single-clock scan FFs
    - Based on **D flip-flops**
  - Two-clock scan FF
    - Level Sensitive Scan Design
Scan Design .......... Concept(2)

- Scan capability:
  - Single-clock scan FF Based on D flip-flops

![D flip-flop diagram]

- Logic overhead

- Master latch
- Slave latch

- Normal mode, D selected
- Scan mode, SD selected

- CK
- TC
Scan Design .......... Concept(3)

- Scan capability:
  - Two-clock scan FF (Level Sensitive Scan Design LSSD)
Scan Design …… Structure

- The SD of the first SFF in the chain is connected to SCANIN
- Q of each SFF is connected to SD on the next SFF
- Q of the last SFF in the chain is connected to SCANOUT
- Three additional pins (SCANIN, SCANOUT, TC)

Not shown: CK or MCK/SCK feed all SFFs.
Scan Design ....... Example
Scan Design .... Design & test Procedure

- Circuit is designed using pre-specified design rules.

- Test structure (hardware) is added to the verified design:
  - Add a test control (TC) primary input.
  - Replace flip-flops by scan flip-flops (SFF) and connect to form one or more shift registers in the test mode.
  - Make input/output of each scan shift register controllable/observable from PI/PO.

- Use combinational ATPG to obtain tests for all testable faults in the combinational logic.

- Add shift register tests and convert ATPG tests into scan sequences for use in manufacturing test.
Scan Design .................. Rules

- After the functional correctness of design verified, it is modified to include scan function.
- To make design scan-testable, it has to satisfy some rules:
  1. **Use only clocked D FFs for state variables**
  2. **At least one PI pin (for TC) must be available for test; more pins, if available, can be used**
     - Any functional PI/PO can be used for SCANIN/SCANOUT
  3. **All FF clocks must be controlled from PIs**
     - Scan register function
  4. **Clocks must not feed data inputs of FFs**
     - FFs in scan are used to (a) capture combinational data in normal mode and (b) carry data our for observation during scan mode
Scan Design ............. Rules

- Correcting a Rule Violation
  - All clocks must be controlled from PIs.

If $D2=0$, then $Q=Q$ (previous)
If $D2=1$, then $Q=D1$
Testing of scan circuit is done in **two phases**:

1. **Test scan register by “Shift Test”**
   - A shift sequence 00110011 ... of length $n_{sff} + 4$ in scan mode (TC=0) produces 00, 01, 11 and 10 transitions in all flip-flops and observes the result at SCANOUT output.

2. **Test SAF in combinational logic**
   - Combinational ATPG is used
   - All FFs outputs are controllable (PPIs)
   - All FFs inputs are observables (PPOs)

**Scan test length:**
- Shift Test: $n_{SFF} + 4$ clock periods
- SAF Test: $(n_{SFF} + 1) n_{comb} + n_{SFF}$ \hspace{1cm} \([n_{comb}]: \# \text{ of comb. Vectors}\]
- Total: $(n_{comb} + 2) n_{sff} + n_{comb} + 4$ clock periods.
- May lead to long test time; e.g., 2,000 scan flip-flops, 500 comb. vectors, total scan test length $\sim 10^6$ clocks.

**Multiple scan registers** reduce test length!!
Assume 9 FFs
While S2 is scanned in, O1 is scanned out (overlapping)
Fault can be either detected by PO or SCANOUT
Scan design ........ Overhead(1)

- **IO pins**: at least one pin necessary.

- **Area overhead**:
  - *Gate overhead* = \[\frac{4 \ n_{\text{ff}}}{(n_g + 10n_{\text{ff}})}\] \times 100\%, where \(n_g = \text{comb. gates}\); \(n_{\text{ff}} = \text{flip-flops}\);
  - Example: \(n_g = 100k\) gates, \(n_{\text{ff}} = 2k\) flip-flops, overhead = 6.7%.

- **Wiring**:
  - Scan requires significant amount of routing
  - More accurate estimate must consider scan wiring and layout area.

- **Performance overhead**:
  - Multiplexer delay added in combinational path; approx. two gate-delays.
  - Flip-flop output loading due to one additional fanout; approx. 5-6%.

- **Design effort cost**
  - Rules checking & repair, synthesis, extraction, verification
Scan design .......... Overhead(2)

- ATPG Example: S5378

<table>
<thead>
<tr>
<th></th>
<th>Original</th>
<th>Full-scan</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of combinational gates</td>
<td>2,781</td>
<td>2,781</td>
</tr>
<tr>
<td>Number of non-scan flip-flops</td>
<td>179</td>
<td>0</td>
</tr>
<tr>
<td>Number of scan flip-flops</td>
<td>0</td>
<td>179</td>
</tr>
<tr>
<td>Gate overhead</td>
<td>0.0%</td>
<td>15.66%</td>
</tr>
<tr>
<td>Number of faults</td>
<td>4,603</td>
<td>4,603</td>
</tr>
<tr>
<td>PI/PO for ATPG</td>
<td>35/49</td>
<td>214/228</td>
</tr>
<tr>
<td>Fault coverage</td>
<td>70.0%</td>
<td>99.1%</td>
</tr>
<tr>
<td>Fault efficiency</td>
<td>70.9%</td>
<td>100.0%</td>
</tr>
<tr>
<td>CPU time on SUN Ultra II, 200MHz processor</td>
<td>5,533 s</td>
<td>5 s</td>
</tr>
<tr>
<td>Number of ATPG vectors</td>
<td>414</td>
<td>585</td>
</tr>
<tr>
<td>Scan sequence length</td>
<td>414</td>
<td>105,662</td>
</tr>
</tbody>
</table>
Scan design \ldots Hierarchical Scan*

- Scan flip-flops are chained within subnetworks before chaining subnetworks.

- Advantages:
  - Automatic scan insertion in netlist
  - Circuit hierarchy preserved – helps in debugging and design changes

- Disadvantage: Non-optimum chip layout.
Scan design .... Automated Design

- (full) scan design is considered the best DFT discipline
  - Completely automated using commercial design tools
  - Design and test are decoupled
- Rules may be violated due to funct. requirements (e.g., in ASIC)
  - **Partial Scan** is then used

```
Rule violations

Scan design rule audits

Gate-level Verified netlist

Behavior, RTL, and logic Design and verification

Scan netlist

Design

Scan hardware insertion

Test

Scan chain FFs order

Chip layout: Scan-chain optimization, timing verification

Combinational ATPG

Combinational vectors

Scan sequence and test program generation

Test program

Design and test data for manufacturing

Design Test

Mask data
```
Scan design......Timing and Power

- Small delays in scan path and clock skew can cause race condition.
- Large delays in scan path require slower scan clock.
- Dynamic multiplexers (transmission gates): Skew between TC and TC* signals can cause momentary shorting of D and SD inputs.
  - Static design is preferred, but require more transistors
- Power dissipation during scan
  - Random signal activity in combinational circuit during scan can cause excessive power dissipation.
Partial-Scan ............ Motivation(1)

- Directed Acyclic Graph (DAG) levelized
  - Nodes present FFs and edges the logic path between them
  - FFs of level 1 directly controlled by PIs
  - Circuit has **no feedback**! No cycle in the graph!
  - **Sequential Depth** = max level (e.g., =3)
  - Sequence of vectors that control all FFs is as long as Seq Depth
  - As Seq Depth increases, the test length increases
Partial-Scan ............ Motivation(2)

- Directed Graph can NOT be levelized
  - Circuit has feedback! Cycles in the graph!
  - We can NOT talk about Sequential Depth
  - Bound of sequence of vectors controlling all FFs unknown
  - Test length and ATPG run time can be quite large
- Test complexity can be reduced by:
  - Scan selected set of FFs: Minimum feedback vertex set (MFVS)
  - Corresponding nodes are removed from s-graph \(\rightarrow\) Acyclic graph
    - E.g., remove FF5 and FF7 (and scan them)
Partial-Scan ............. Definition

- A subset of flip-flops is scanned.

Objectives:
- Minimize area overhead and scan sequence length, yet achieve required fault coverage
- Exclude selected flip-flops from scan:
  - E.g., Break all large cycles
  - Improve performance
  - Allow limited scan design rule violations
- Allow automation:
  - In scan flip-flop selection
  - In test generation
- Shorter scan sequences

However,
- It requires **sequential** ATPG
Partial-Scan ……….. Architecture

- Select a minimal set of flip-flops for scan to eliminate all cycles.
- Alternatively, to keep the overhead low only long cycles may be eliminated.
- In some circuits with a large number of self-loops, all cycles other than self-loops may be eliminated.
- Separate CK’s for SFF and non-scan FFs
  - Necessary since SFFs can be active while non-scan FFs have to hold their values
Partial-Scan………… Comparison

- Partial versus full scan for s5378 circuit [Bell Lab’s 1991]

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<thead>
<tr>
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<th>Partial-scan</th>
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<tbody>
<tr>
<td>Number of gates</td>
<td>2,781</td>
<td>3,497</td>
<td>2,901</td>
</tr>
<tr>
<td>Number of non-scan flip-flops</td>
<td>179</td>
<td>0</td>
<td>149</td>
</tr>
<tr>
<td>Number of scan flip-flops ($n_{sff}$)</td>
<td>0</td>
<td>179</td>
<td>30</td>
</tr>
<tr>
<td>Gate overhead (Equation 14.2)</td>
<td>0.0%</td>
<td>15.66%</td>
<td>2.63%</td>
</tr>
<tr>
<td>Number of faults</td>
<td>4,603</td>
<td>4,603</td>
<td>4,603</td>
</tr>
<tr>
<td>PI/PO for ATPG</td>
<td>35/49</td>
<td>214/228</td>
<td>65/79</td>
</tr>
<tr>
<td>Fault coverage (Equation 7.12)</td>
<td>70.0%</td>
<td>99.1%</td>
<td>93.7%</td>
</tr>
<tr>
<td>Fault efficiency (Equation 7.13)</td>
<td>70.9%</td>
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<td>1,117</td>
</tr>
<tr>
<td>Test sequence length (Equation 14.1)</td>
<td>414</td>
<td>105,662</td>
<td>34,691</td>
</tr>
</tbody>
</table>
Partial-Scan Test Generation

- Scan and non-scan flip-flops are controlled from separate clock PIs:
  - Normal mode – Both clocks active
  - Scan mode – Only scan clock active

- Seq. ATPG model:
  - Scan flip-flops replaced by PPI and PPO
  - Seq. ATPG program used for test generation
  - Scan register test sequence, 001100..., of length $n_{sff} + 4$ applied in the scan mode
  - Each ATPG vector is preceded by a scan-in sequence to set scan flip-flop states
  - A scan-out sequence is added at the end of each vector sequence

- Test length = ($n_{ATPG} + 2$) $n_{sff} + n_{ATPG} + 4$ clocks
Scan variations..... Scan-Hold-Flip-Flop (SHFF)

- Add a hold capacity to SFF
- Applications:
  - Reduce power dissipation during scan
  - Isolate asynchronous/combinational parts during scan test
  - Useful Delay testing: Converts delay testing into combinational logic problem
- Disadvantages
  - Additional input pin HOLD to be routed to all FFs
  - SFF area increased with ~ 30% (4 additional gates)
  - Performance overhead (transparent mode: 1 to 2 gate delay in the path)

If HOLD=1, HL transparent
If HOLD=0, HL retains its value
Normal mode: TC=HOLD=1
Scan mode: TC=HOLD=0

Hold latch (HL)

To SD of next SHFF
Summary (1)

- Scan is the most popular DFT technique:
  - Rule-based design
  - Automated DFT hardware insertion
  - Combinational ATPG

- Advantages:
  - Design automation
  - High fault coverage; helpful in diagnosis
  - Hierarchical – scan-testable modules are easily combined into large scan-testable systems
  - Moderate area (~10%) and speed (~5%) overheads

- Disadvantages:
  - Large test data volume and long test time
  - Basically a slow speed (DC) test
Summary (2)

- Partial-scan is a generalized scan method; scan can vary from 0 to 100%.
  - Elimination of long cycles can improve testability via sequential ATPG.
  - Elimination of all cycles and self-loops allows combinational ATPG.
  - Partial-scan has lower overheads (area and delay) and reduced test length.
  - Partial-scan allows limited violations of scan design rules, e.g., a flip-flop on a critical path may not be scanned.

- Multiple scan chain
  - Reduce the test time by forming more than once scan chain that can be operated in parallel
  - Effective for BIST design (No pin penalty)
  - Effective for circuits with multiple clocks controlling different parts of the circuits