Boundary Scan Standard
(Chapter 16)

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Learning aims

- Describe the purpose of IEEE std 1149.1 (JTAG)
- Explain the JTAG concept & architecture
- Compare and analyze the different operation modes
Contents

- Motivation
  - Need of a standard
- Standard purposes
- Boundary Scan
  - Concept
  - Boundary scan instructions
  - Architecture
  - Boundary scan cell
- Boundary scan components
  - Registers, TAP controller
- Boundary Scan Description Language*
- Summary
Motivation ....... Traditional PCB Testing

- In 1970s: “In Circuit Testing ICT”
  - PCBs tested by probing the backs of the boards with nails
  - Technology component was “Dual-Inline-Package” DIP
  - Testing mechanisms relies on nails in a bed-of-nails tester
  - Printed Circuit Boards (PCBs) included discrete components
Motivation ........ Traditional PCB Testing

- **Surface-mount technology (SMT) replaced DIP**
  - Reduced space between PCB wires => Nails would short wires
  - Reduced inductance in PCBs (package height reduced)
  - Board inductance is serious problem for high speed
  - Component soldered on both sides of the PCB without drilling holes in PCB => Cost reduction (miniaturization)
  - There are no through holes pins with solder bumps for nails to hit => In Circuit Testing Impractical & expensive

- **Increase in device density**
- **Decrease in board size**
Motivation ........ Need to replace ICT

⇒ Need to replace In-Circuit Testing” with a STANDARD

- Std way to deliver vectors to electronics sub-assembly
- Can be used by designers (IC, board, system) without need to fully understand testing problems of other communities.
- Need standard System Test Port and Bus
- Integrate components from different vendors
  - Test bus identical for various components
  - One chip has to test hardware for other chips

Motivation ........ JTAG Team

- JTAG Meeting, September 17, 1988
Motivation

Purpose
Motivation

Basic motivation was miniaturization of device packaging, leading to ...
Surface mount packaging styles, leading to ...
Double sided boards, leading to ...
Multi-layer boards, leading to ...
A reduction of physical access test lands for traditional bed-of-nail in-circuit testers

Problem: how to test for manufacturing defects in the future?
Solution: add boundary-scan registers to the devices
Purpose of Standard

- Let test instructions and test data be serially fed into a \textit{component-under-test (CUT)}
  - Allows reading out of test results
  - Allows \textit{RUNBIST} command as an instruction
    - Eliminates excessive shifting when external tests used

- JTAG can operate at chip, PCB, & system levels
- Lets components be tested separately from wires
- Lets system interconnect be tested separately from components
-Lets other chips collect responses from CUT
- Allows control of tri-state signals during testing
Boundary Scan ........... Concept(1)

Each boundary-scan cell can:
- **Capture** data on its parallel input PI
- **Update** data onto its parallel output PO
- **Serially scan** data from SO to its neighbour’s SI
- Behave **transparently**: PI passes to PO
- Note: all digital logic is contained inside the boundary-scan register
**Boundary Scan**

- **Four** modes of operations:
  - **Normal/Transparent**: Data-in passed to Data-out
  - **Capture**: Test Data-In will be captured into “Capture Scan Cell” by the next ClockDR
  - **Update**: Data stored in “Capture Scan Cell” is propagated to Update Hold Cell”.
  - **Serial shift**: Test data shifted from SI and test response can be scanned out through SO

- Two D FFs with two front-end and back-end mux of data
Boundary Scan .......... Concept(2)

- Using the boundary scan path
- What does The Tester see?
Boundary Scan…… Architecture (1)

- A FSM TAP controller with inputs TCK, TMS, TRST*
  - TAP controller manages exchange of data and instructions among the board and chips
- A n-bit (n≥2) Instruction Register IR
  - IR receives instruction, decode it to perform operation on DR
- A boundary-scan cell on each I/O pins (configurable)
- 1 bit bypass Register
- Optional 32-bit identification register
- Set of four dedicated pins
  - TDI: Serial Test Data Input
  - TDO: Serial Test Data Output
  - TCK: Test Clock
  - TMS: Test Mode Select
  - TRST*: Asynchronous Reset
- TDI/TDO are similar to scan-in(scan-out of the scan path design
- Both TMS and TCK are distributed to all chips on the board
Boundary Scan Architecture (2)

- **Normal operation:** extra hardware on the chips is transparent
- **Test mode:** All inputs are scanned in from TDI and scanned out through TDO to the board

Boundary Scan allow two testing modes

- **External Testing**
  - Interconnect between the chips
- **Internal Testing**
  - Testing of the logic within the chip
Boundary Scan ....... Instructions(1)

- Since 1149.1-2001, four mandatory instructions: EXTEST, BYPASS, SAMPLE and PRELOAD

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Target (Active) Register</th>
<th>Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>Extest</td>
<td>Boundary Scan</td>
<td>Formerly All-0s</td>
</tr>
<tr>
<td>Bypass</td>
<td>Bypass</td>
<td>All-1s</td>
</tr>
<tr>
<td>Sample</td>
<td>Boundary Scan</td>
<td>Undefined</td>
</tr>
<tr>
<td>Preload</td>
<td>Boundary Scan</td>
<td>Undefined</td>
</tr>
</tbody>
</table>

IR \geq 2
Reset:
TMS = 1, 5 \times TCK
Boundary Scan........ Instructions(2)

- IEEE 1149.1 describes four mandatory and six optional instructions
- Instruction Register must be at least 2 bits long

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Selected Data Register</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Mandatory:</strong></td>
<td></td>
</tr>
<tr>
<td><code>Extest</code></td>
<td>Boundary scan (formerly all-0s code)</td>
</tr>
<tr>
<td><code>Bypass</code></td>
<td>Bypass (initialised state, all-1s code)</td>
</tr>
<tr>
<td><code>Sample</code></td>
<td>Boundary scan (device in functional mode)</td>
</tr>
<tr>
<td><code>Preload</code></td>
<td>Boundary scan (device in functional mode)</td>
</tr>
<tr>
<td><strong>Optional:</strong></td>
<td></td>
</tr>
<tr>
<td><code>Intest</code></td>
<td>Boundary scan</td>
</tr>
<tr>
<td><code>Idcode</code></td>
<td>Identification (initialised state if present)</td>
</tr>
<tr>
<td><code>Usercode</code></td>
<td>Identification (for PLDs)</td>
</tr>
<tr>
<td><code>Runbist</code></td>
<td>Result register</td>
</tr>
<tr>
<td><code>Clamp</code></td>
<td>Bypass (output pins in safe state)</td>
</tr>
<tr>
<td><code>HighZ</code></td>
<td>Bypass (output pins in high-Z state)</td>
</tr>
</tbody>
</table>

NB. All unused instruction codes must default to `Bypass`
**EXTEST**

- Actually reason behind boundary scan
- Allows **testing of connectivity** of pins of IC mounted on PCB
- Allow **testing of off-chip circuits**
- Fault models used are: SAF, bridging faults & opens

- Test vectors shifted in boundary scan register and applied to PCB inputs
- Shift responses out of boundary scan register of all chips to observe the response
Boundary Scan…….. Instructions(4)

- **EXTEST**

  - Allows testing of connectivity of pins of IC mounted on PCB and testing of off-chip circuits

![Diagram of EXTEST](image)

**INPUT CELL**

- **ShiftDR**
- **SO**
- **Mode**

**OUTPUT CELL**

- **ShiftDR**
- **SO**
- **Mode**

Component boundaries:

- Data transfer paths activated in EXTEST mode.
Boundary Scan……… Instructions(4)

- **BYPASS**
  - Bypass the boundary scan chain with one bit Bypass Register
  - Useful when only one component in the chain is being tested
 Boundary Scan…… Instructions(5)

- **SAMPLE**
  - Boundary scan register selected
  - Obtain a snapshot of the normal operation of the internal logic (without interruption)
  - Device in functional mode
Boundary Scan……… Instructions(6)

- **PRELOAD**
  - Preload known data into boundary scan cells prior to some follow-on operation (test, debug)
  - Device in functional mode
INTEST (optional)

- Boundary scan register selected/ Device in test mode
- Used to apply/shift external test patterns to the device itself
- Responses are scanned out
**Boundary Scan…….. Instructions(8)**

- **IDCODE (optional)**
  - Allow board-level test controller to read out component ID

- **Optional Identification register** selected, if available, else Bypass register selected
- **Used to capture internal 32-bit identification code** (manufacturer, part number, version number) and then shift out through TDO
**USERCODE (optional)**
- Intended for user-programmable components (FPGA)
- Allow external tester to determine user programming of the programmable component

- Optional Identification register selected, if available, else Bypass register selected
- Use to capture an alternative 32-bit identification code for dual personality devices e.g. PLDs
Boundary Scan…… Bypass Register

- 1 bit register, used to bypass a chip if wanted
  - Basic serial shift function
- It is set to 0 when TAP controller is in Capture-DR

- One-bit shift register, selected by the Bypass instruction
- Captures a hard-wired 0
- Note: in the Test-Logic/Reset state, the Bypass register is the default register if no Identification Register present
Boundary Scan ... Identification Register

- Optional register
  - Consists of version, part number, manufacturing identify

- 32-bit shift register
- Selected by \textit{Idcode} and \textit{Usercode} instruction
- No parallel output
- Captures a hard-wired 32-bit word
- Main function: identify device owner and part number

- Note: \textit{Idcode} is power-up instruction if Identification Register is present, else \textit{Bypass}
Boundary Scan

- Linked together to form boundary scan register
- The order of linking is determined by the physical adjacency of pins and/or by order of layout constraints

- Shift register with boundary-scan cells on:
  - device input pins
  - device output pins
  - control of three-state outputs
  - control of bidirectional cells

- Selected by the **Exttest, Intest, Preload** and **Sample** instructions
Boundary Scan……. Instruction register

- Serial-in parallel-out register
- IR consist of at least two shift registers
  - Hold register and Scan register (Update register)
- Allow coding of at least 4 mandatory instructions
TAP Controller

- 16 finite state machine which produce the various control signals
  - Dedicated signals to IR (ClockIR, ShiftIR, UpdateIR)
  - Dedicated signals to DR (ClockDR, ShiftRD, UpdateDR)
  - Reset*: distributed to IR and targeted DR
  - Select: distributed to output mux
  - Enable: distributed to output drive amplifier

16-state FSM
TAP Controller
(Moore machine)
A state transition occurs on the positive edge of TCK, and the controller output changes on the falling edge of the TCK.
Boundary Scan Description Language (BSDL)

**Purpose:**

- Facilitate communication of information describing test logic of parts:
  - Between companies and CAD tools
  - Can be used by automatic test-pattern generators
  - Used by synthesis tools to synthesize test logic

- Not usable as a simulation model
  - Cannot describe voltages, currents, or timing

- Implemented as subset of **VHDL**
  - Must modify for certain **VHDL** tools
BSDL................. Features

- Describable:
  - Length & structure of boundary scan reg.
  - Availability of optional TRST pin
  - Physical locations of TAP pins
  - Instruction codes
  - Device identification code

- Not describable:
  - TAP controller state diagram
    - Must be a standard one
  - Bypass register
    - Always present and always 1 bit
  - Length of Device Identification Register
    - Set by JEDEC standard
  - Presence of SAMPLE / PRELOAD, BYPASS, EXTEST instructions
    - Always present
  - Operation of user-defined instructions
BSDL.................... Entity description*

- **Entity description**
  - Describes component-specific test logic parameters
  - Describes standard VHDL package & package body
    - Defines BSDL subset of VHDL
    - Defines commonly used boundary scan cell types

- **Example**
  
  ```vhdl
  entity diff is
  generic (Physical_Pin_Map: string:= "Pack");
  port (TDI, TMS, TCK: in bit;
    TDO: out bit; IN1, IN2: in bit;
    OUT1: out bit; OUT2: buffer bit;
    OUT3: out bit_vector (1 to 8);
    OUT4: out bit_vector (4 downto 1);
    BIDIR1, BIDIR2, BIDIR3: inout bit;
    GND, VCC: linkage bit);
  use STD_1194_1_1994.all;
  attribute BOUNDARY_REGISTER of diff:entity is ...
  ```
BSDL............. TAP Descriptions*

- Says which logical signals comprise the TAP
- Specify which input port logic values enable JTAG compliance (part can either conform to JTAG or refuse to conform)
- Instruction register description:
  - Length
  - Op Codes -- can add optional instructions
  - Mapping from bit patterns to instruction Op Codes
  - Define private instructions
  - Specify bit pattern captured in Capture-IR controller state (2 LSB’s are always “01”)
- IDCODE and USERCODE register contents
Summary

- Boundary Scan Standard has become absolutely essential
  - No longer possible to test printed circuit boards with *bed-of-nails* tester
  - Not possible to test multi-chip modules at all without it
  - Supports BIST, external testing with Automatic Test Equipment, and boundary scan chain reconfiguration as BIST pattern generator and response compacter
  - Now getting widespread usage