VLSI Test Technology and Reliability

Said Hamdioui

Delft University of Technology
Computer Engineering Lab
Mekelweg 4, 2628 CD Delft
The Netherlands

S.Hamdioui@tudelft.nl
http://ce.et.tudelft.nl/~said
Skype: Said.Hamdioui
Tel: +31- 15 278 3643
+31- 62 880 2494
Office: EWI/15.020

2009-2010

Delft University of Technology

Instructor

- Education
  - 1997: MSEE from TU Delft (Cum Laude)
  - 2001: PhD from TU Delft (Cum Laude)
- Employment
  - Intel, CA, USA (3 years)
  - Philips Semiconductors R&D, Crolles, France (1 year)
  - NXP Semiconductors , Nijmegen, the Netherlands (2.5 years)
  - TU Delft (~2.5 years)
- Research area
  - VLSI Test technology, Reliability and fault tolerance
  - Silicon and non-silicon technology
- Publications
  - One book
  - Over 70 journals and conference papers

Goals of today…

- Understand the course organization, outline, examination, etc
- Be able to describe the importance of VLSI test technology and reliability for ICs
- Become familiar with key words in the field
- Be able to describe the major challenges in the field

Topics of today

- What is VLSI Test Technology and Reliability?
- Motivation
- About the course (organization, materials, goals, plan, …)

- Introduction to IC test
  - Definitions and concepts
- VLSI realization process
- Design for testability
- Manufacturing test flow
- Trends in SoC design and test

What is VLSI Test and reliability?

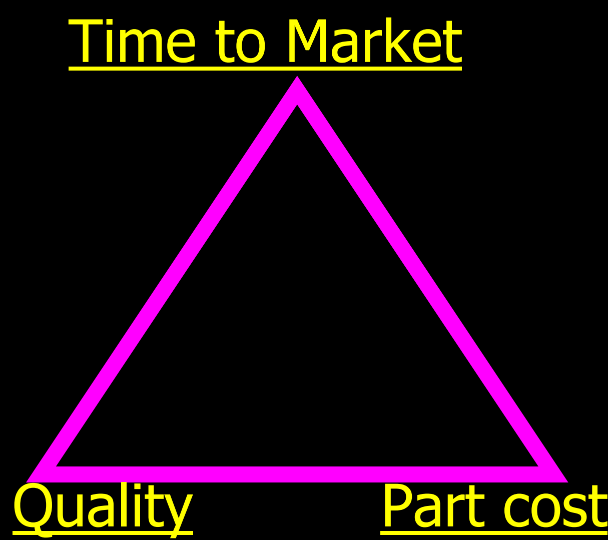
- Test/Quality
  - Guarantee that the IC performs its function at t=0
  - Conformance to specifications: time-independent
  - Measured in **DPM** (defects part per million)
  - Driven by defect/fault coverage & performance guard-bands
  - Impacts B2B relationship

- Reliability
  - Guarantee that the IC performs its function for $t \geq T_{lifetime} > 0$
  - Meeting specification over time: time-dependent
  - Measured in **FIT** (Failure in 10^9 device-operating hours)
  - Driven by changing material properties, application profile, environment,..
  - Impacts C2B relationship

Strong correlation between Quality & Reliability

Motivation……………. time, cost, quality

Quick to market advantages:
- **Predictability** $0.95T<T<1.05T$
- First in the market
- Fast response to competitive threat



Customer satisfaction
- Test escapes
- First good chip
- **Reliability**

Board System Product
- Diagnosis
- Rework/ repair

Chip Overhead IC
- Si area overhead
- Pad overhead

Test application
- Tester cost
- Testing time
- DFT cost

Predictability & Reliability are the driving factors

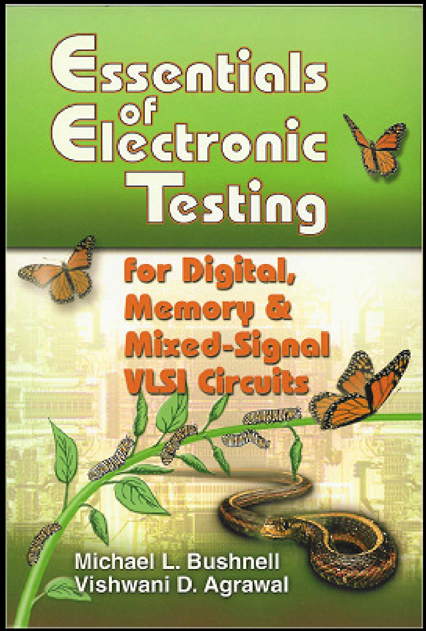
Motivation………………………… Share of test cost

Ref: SIA roadmap

The share of test cost continuously increases

About the course……… organization and materials

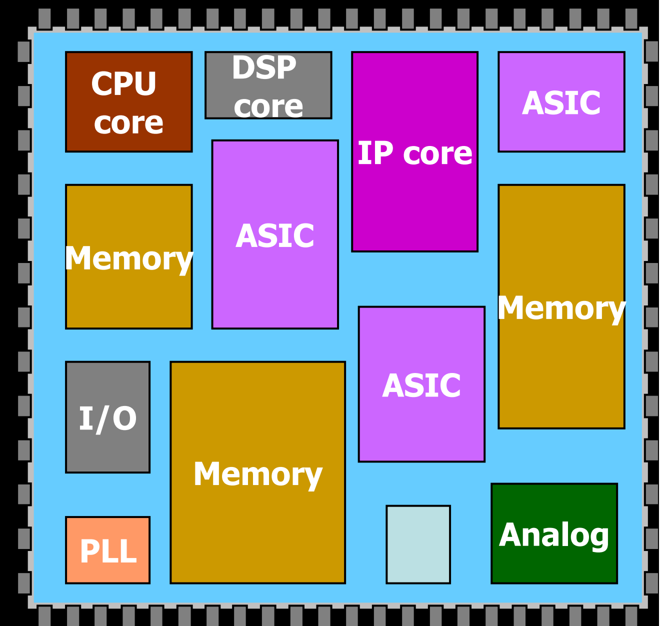
- **VLSI Test Technology and Reliability**
  - Code: ET4076
- **Course material:**
  - Book: *Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits*, M. L. Bushnell and V. D. Agrawal
  - Additional reading: scientific papers
- **Assessment:**
  - Oral exam (or writing a chapter): 90%
  - Assignments: 10%
- **ECTS**: 4
- **Expected prior knowledge**
  - Digital design
  - Some knowledge about IC manufacturing



About the course……… Contents

Things you'll be learning:

- VLSI Test philosophy
- Defects and fault modeling
- Test schemes/Design for testability for digital circuits
  - Algorithms, Scan design, Delay Test , etc
- Memory testing
- Boundary Scan
- Built-In-Self Test
- Testing for reliability
- Future trends in digital design and test



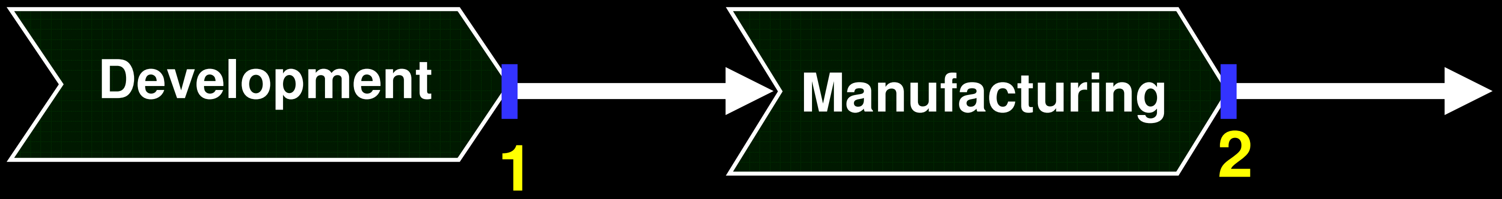
- Better understand the weaknesses of IC's and do research on VLSI Test
- Become a better VLSI designer

The basics of testing digital circuits: theory and practice

Introduction to IC Testing…. Verification vs. Testing

- Design synthesis: Given an I/O function, develop a procedure to manufacture a device using known materials and processes.
- Verification: Predictive analysis to ensure that the synthesized design, when manufactured, will perform the given I/O function [after development]
- Test: A manufacturing step that ensures that the physical device, manufactured from the synthesized design, has no manufacturing defect [after manufacturing].

Introduction to IC Testing…. Verification vs. Testing



1. (Design) Verification

- Verifies correctness of design (target **design errors**)
- Performed by simulation, hardware emulation, or formal methods.
- Performed **once** prior to manufacturing
- Responsible for **quality of design**

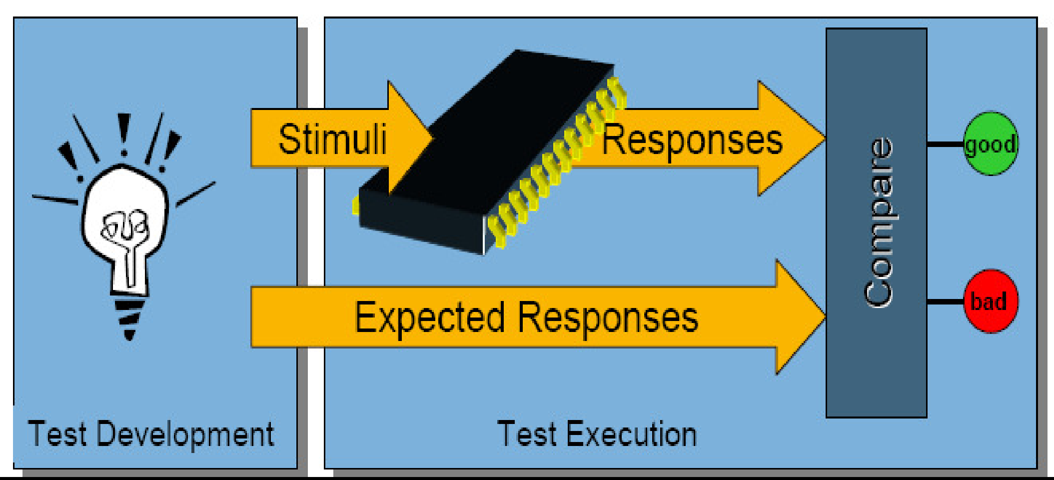
2. (Manufacturing) Testing

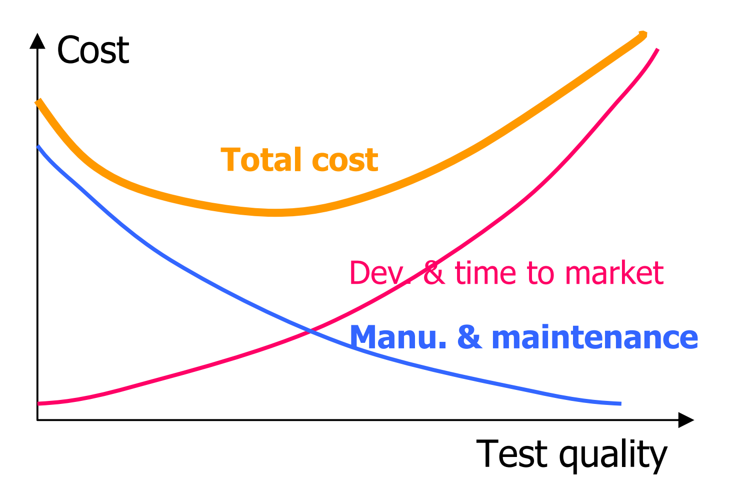
- Verifies correctness of manufactured IC (target manufacturing defects)
- Two-part process:
  - Test generation: software process executed once <u>during design</u>
  - Test application: electrical tests applied to hardware
- Test application performed on **every** manufactured device
- Responsible for **quality of devices**

Introduction to IC Test…. Definition

TESTABILITY:

- The ability to SYNTHESIZE, GENERATE, EVALUATE, APPLY and OBSERVE tests to satisfy
  - A range of predetermined objectives e.g.,
    - Fault coverage, Defect level, Time-to volume, etc
  - Subject to two fundamental constraints : **TIME** and **MONEY**





Testing has a profound effect on the cost

Introduction to IC Test…. Why testing?

- The motivation is the **QUALITY** where:

QUALITY= Meeting the expectation of the customer

- Manufacturing process is complicated & time consuming
- Defects are inevitable
  - Original silicon: E.g., impurities, dislocations
  - Manufacturing process: process variation, temperature fluctuations, opens, shorts, extra/missing transistors, spot defects, etc
  - Soft faults (in field)
    - Increase speed and noise margin reduction reduce robustness
    - Nanometer technologies sensitive to radiation (at sea level)

Testing is indispensable

Introduction to IC Test .... *Ideal versus real tests*

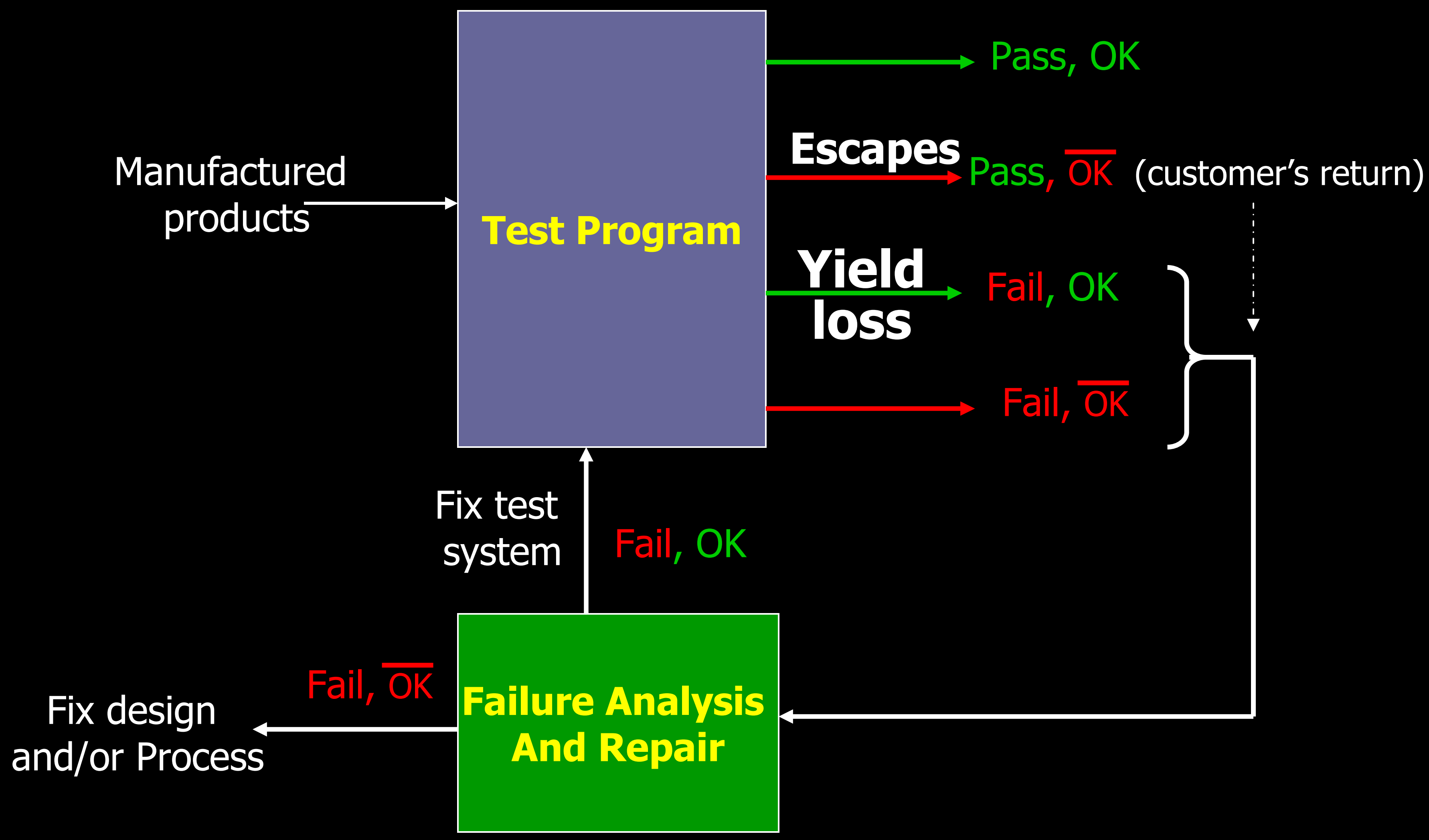
Ideal tests

- Detect all defects produced in the design and/or manufacturing
- Pass all functionally good devices
- Fail all functionally bad devices
- Detect all reliability related defects

Real tests

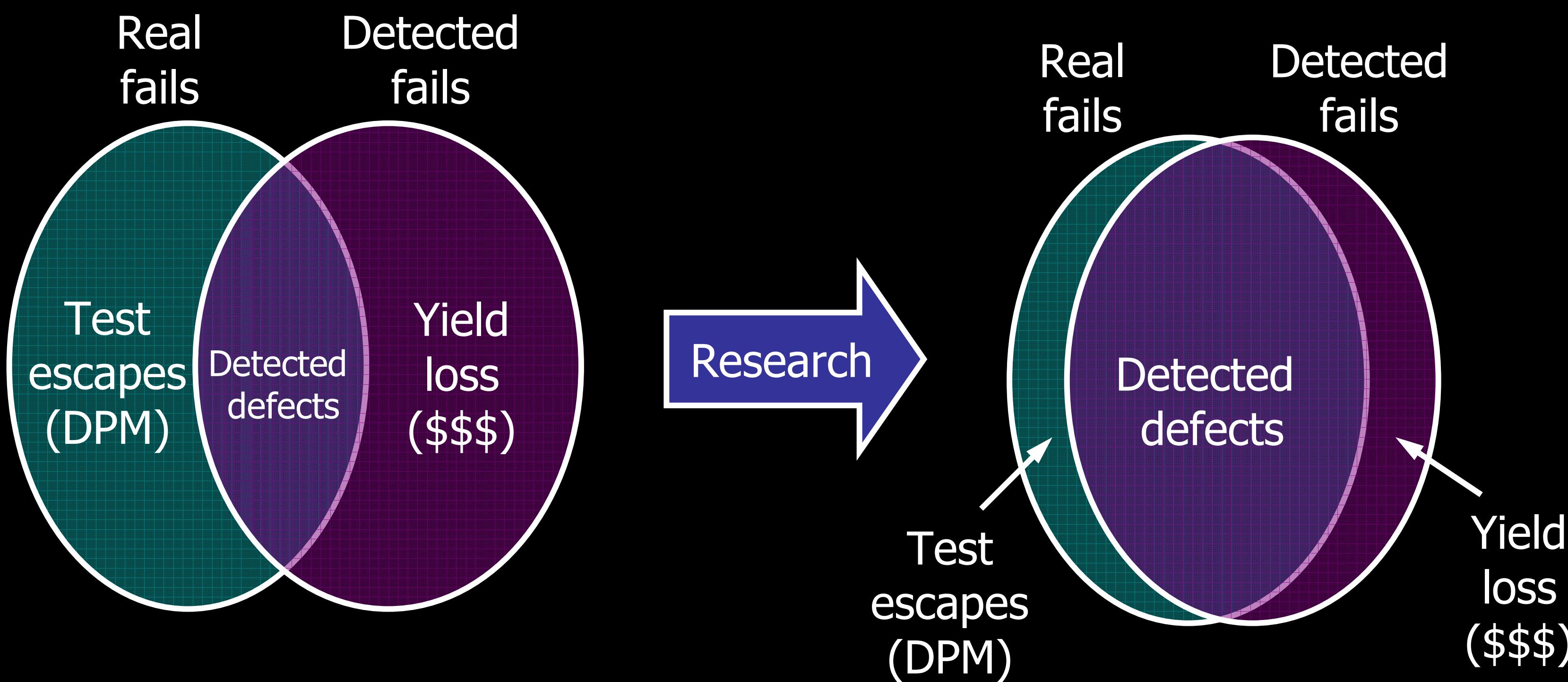
- Very large number of possible defects need to be tested
- Difficult to generate tests for some real defects (defect oriented testing)
- Based on analyzable **fault models**
- Incomplete coverage of modeled faults due to high complexity/ high cost
- Some good chips are rejected (**yield loss**)
- Some bad chips pass (**escapes**/ defect level in Defect-Per-Million **DPM**)

Introduction to IC Test ……… *Escapes and yield loss*



Introduction to IC Test .... Goal of R&D

- Research targets product **COST & QUALITY**
- Current tests PARTLY target real fails
- Research identifies real fails to reduce cost and increase quality



Introduction to IC Test .... Testing depends on

	Quality	Budget
Application	**Quality**	**Budget**
• Toys	Lowest	Lowest
• Consumer electronics	Low	Moderate
• Automotive/security	High	High
• Healthcare/aerospace	Highest	Highest

- **Circuit type**
  - Digital logic
  - Memory
  - Analog
  - RF

- **Testing stage**
  - Characterization (first silicon sample)
  - Production test (wafer test, e-sort)
  - Reliability test

Introduction to IC Test ……….. Cause of escapes

- Timing related defects
  - Complete timing testing impractical
  - Increased speed makes circuits more sensitive to smaller delays
    - Number of small delay defects increases rapidly
- Un-modeled faults/Untested faults
  - Not all faulty behavior identified and modeled/test time limitations
- Environmental failures
  - Failures at specific temperatures and/or voltages
  - Noise related failures/ signal integrity
- Circuit/process sensitivities
  - Design not verified over complete range of specifications
- Soft errors
  - Memory sensitivity increases with each technology generation

Introduction to IC Test….. Roles of Testing

- Detection:

  Determination whether or not the *device under test* (DUT) has some fault.

- Diagnosis:

  Identification of a specific fault that is present on DUT.

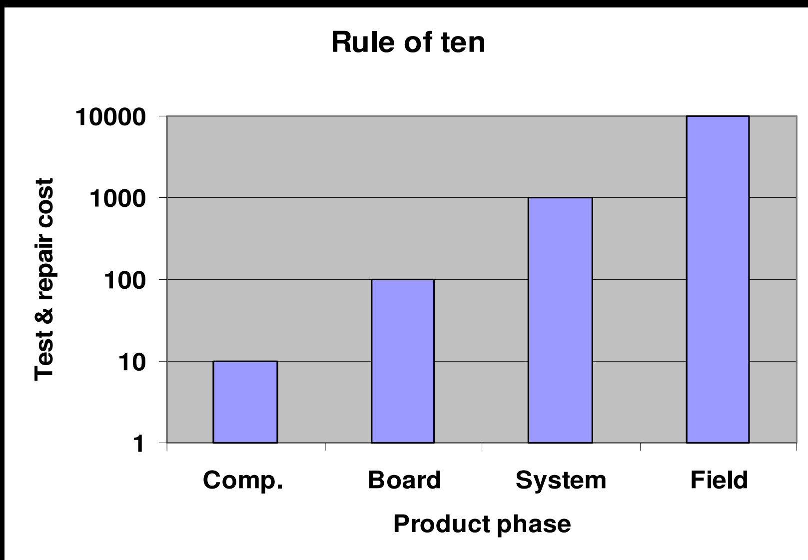
- Device characterization:

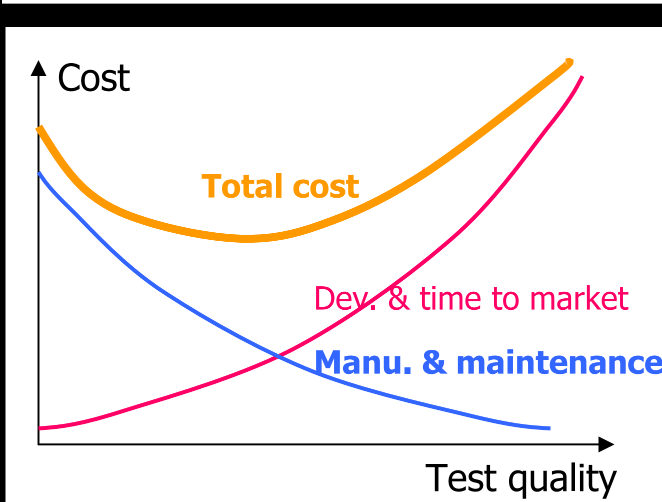
  Determination and correction of errors in design and/or test procedure.

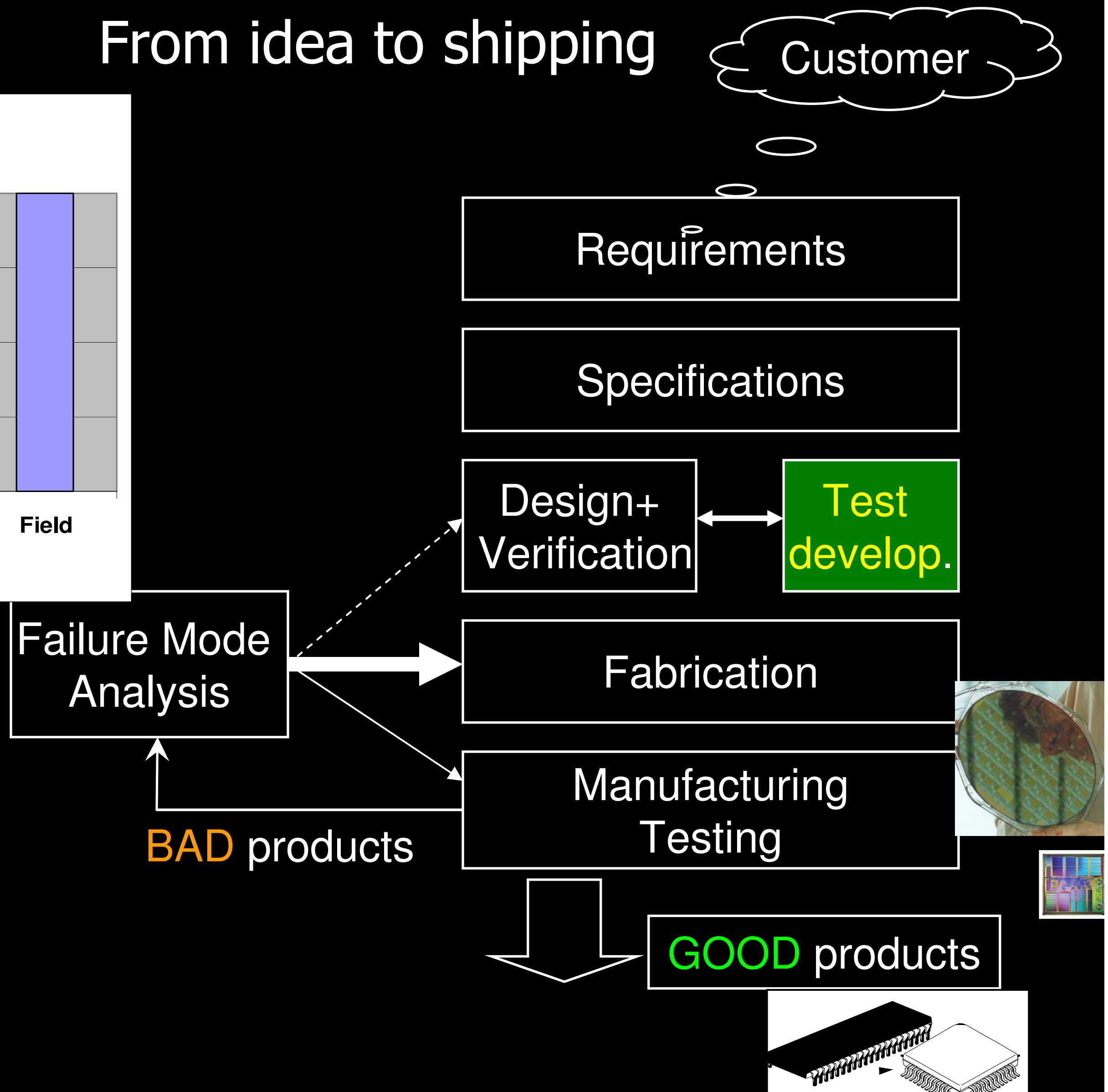
- *Failure mode analysis* (FMA):

  Determination of manufacturing process errors that may have caused defects on the DUT.

Today VLSI realization process





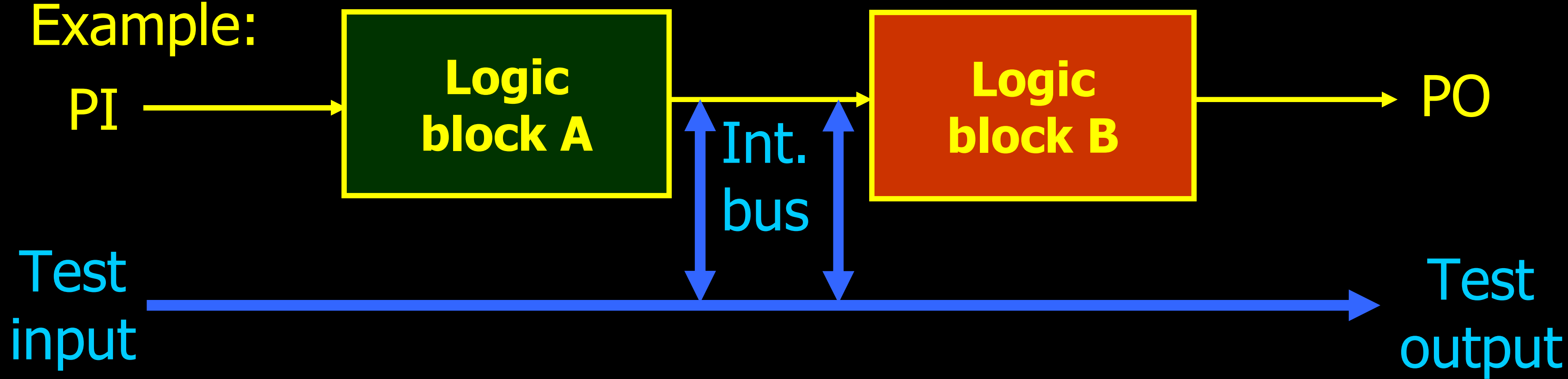


Design for Testability DFT

- *DFT refers to those design techniques that make test generation, test application and test evaluation cost-effective.*

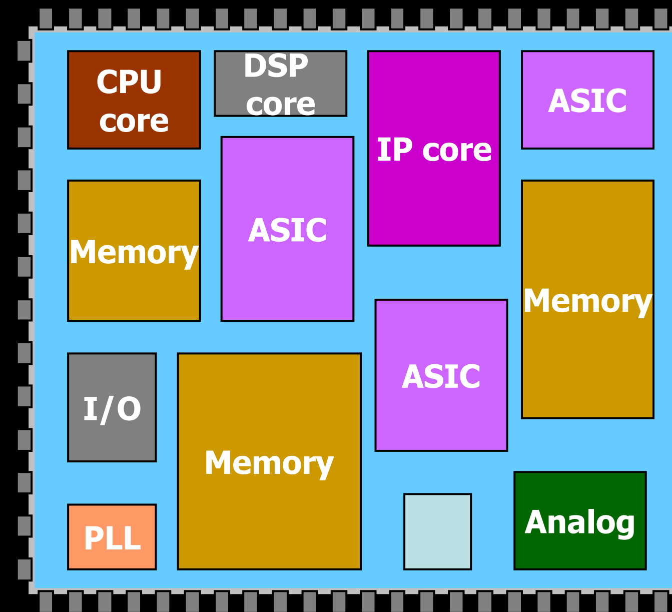
- DFT helps answering three main questions:
  - Can tests that detect all faults assured?
  - Can test development time be kept within economical limits?
  - Can test execution time be kept within economical limits?

- Example:



Design for Testability DFT

- Electronic systems consists of different components
  - Digital logic
  - Memory blocks
  - Analog and mixed-signal blocks



- Each component requires specific DFT
- Component level-DFT is not sufficient for producing testable system
  - Access mechanism to the embedded component needed

Design for Testability DFT

- DFT methods for digital circuits
  - Ad-hoc methods
  - Structured methods:
    - Scan/ Partial Scan
    - Built-in self-test (BIST)
    - Boundary scan
    - Test compression
    - ...

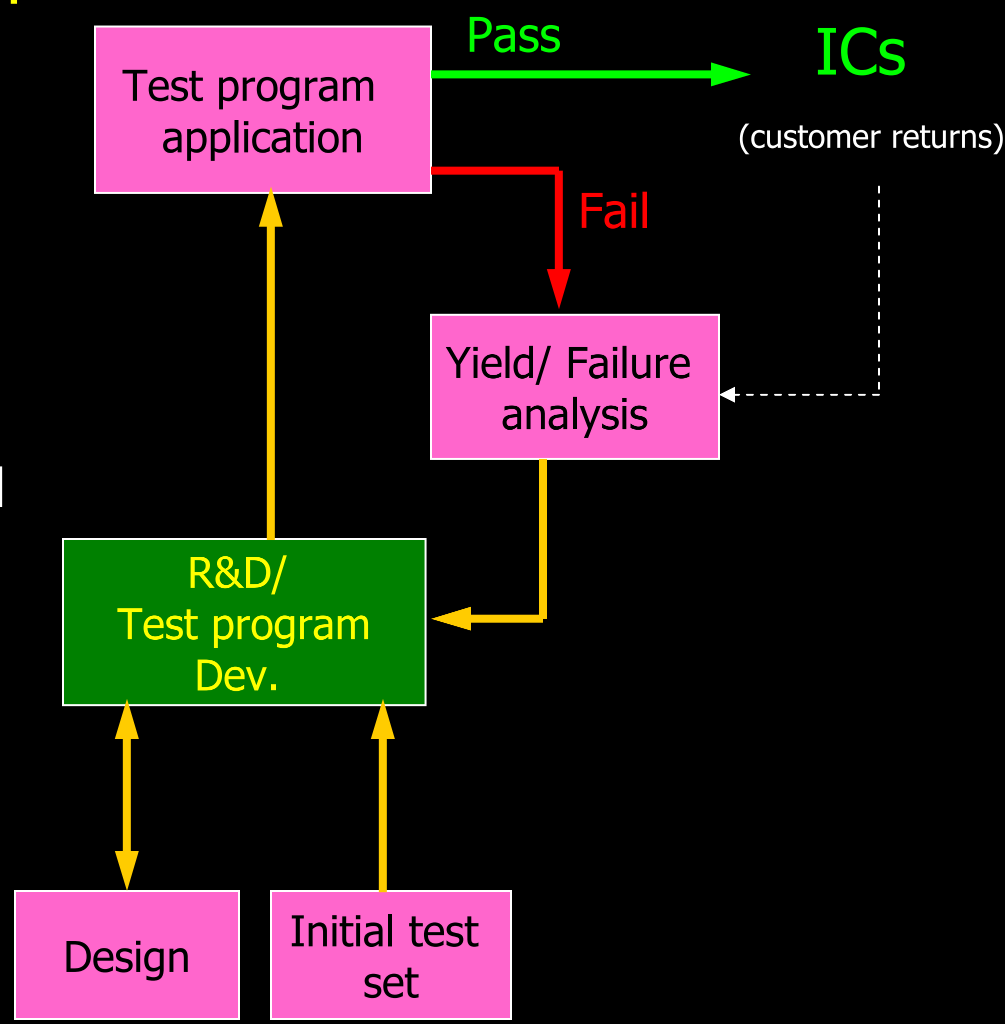
- DFT method for mixed-signal circuits
  - Analog test bus
  - BIST??

Manufacturing test flow

- Three main sources of test info:

- Initial test set from older technologies → adapt it
- New technologies introduces new faults → additional tests required (R&D)
- Depending on target yield (and customer returns), test set is adapted (using e.g., failure analysis)

- Test adaptation LOOP: Test application → Yield/failure analysis → R&D



Testing Costs

- Design for testability (DFT)
  - Chip area overhead and yield reduction
  - Performance overhead
- Software processes of test
  - Test generation and fault simulation
  - Test programming and debugging
- Manufacturing test
  - *Automatic Test Equipment* (ATE) capital cost
  - Test center operational cost

Testing Costs ……Manufacturing Testing in 2000AD

- 0.5-1.0GHz, analog instruments, 1024 digital pins: ATE purchase price

  = $1.2M + 1024 x $3000 = $4.272M

- Running cost (**five-year** linear depreciation)

  = Depreciation + Maintenance + Operation

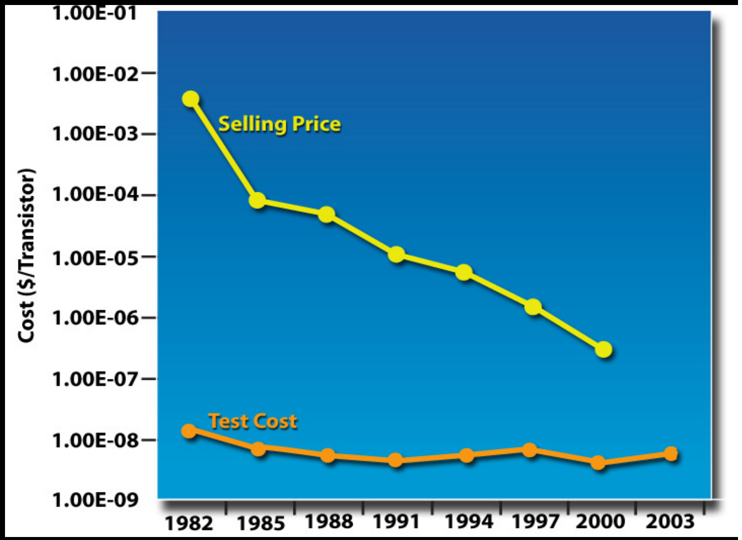
  = $0.854M + $0.085M + $0.5M

  = $1.439M/year

- Test cost (24 hour ATE operation)

  = $1.439M/(365 x 24 x 3600)

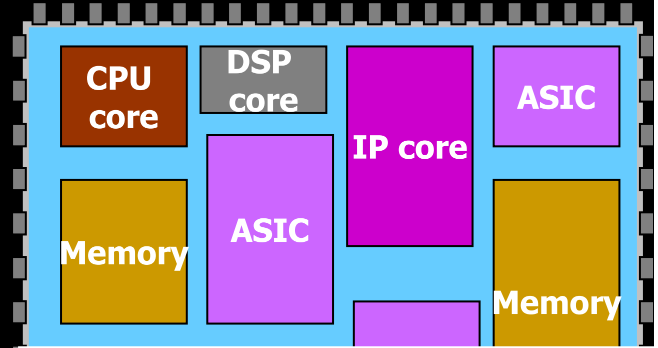
  = 4.5 cents/second

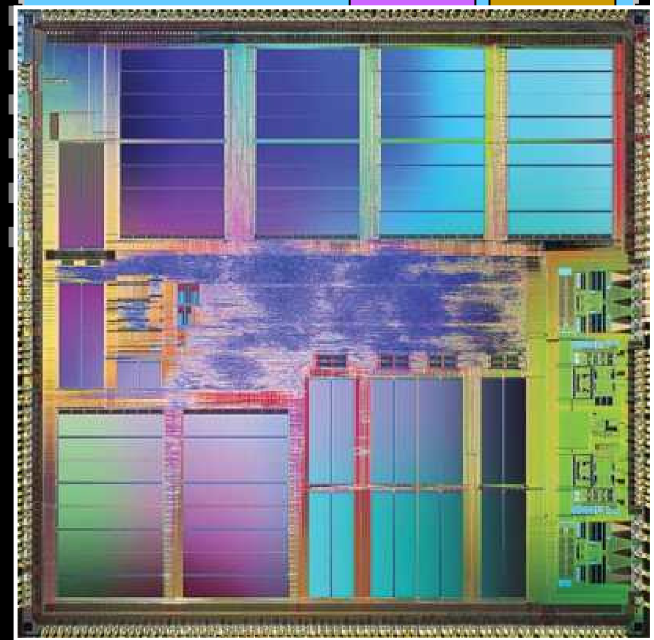


Assume: Circuit test time is 6 sec.
This results in test cost as 27 cents.
If only 65% pass the test (yield), the test contribution to the price of a good chip is 27/0.65 = 41.5 cents.

Trends in SoC design & test

- Enhancement in semiconductor IC & technology
  - Integration density is steadily increasing
  - Feature sizes decreasing (10nm in 2011?)
- More & different devices included and new types of structures integrated
  → Increase in complexity
- This impacts:
  - Design styles
  - Power ($P_{dyn} = \alpha.C.f.Vdd^2$)
  - Leakage (static and dynamic)
  - Testing (digital, analog,…)
  - Reliability (electromigration, ESD,…)
  - Signal integrity (cross talk, signal propagation, supply noise, …)

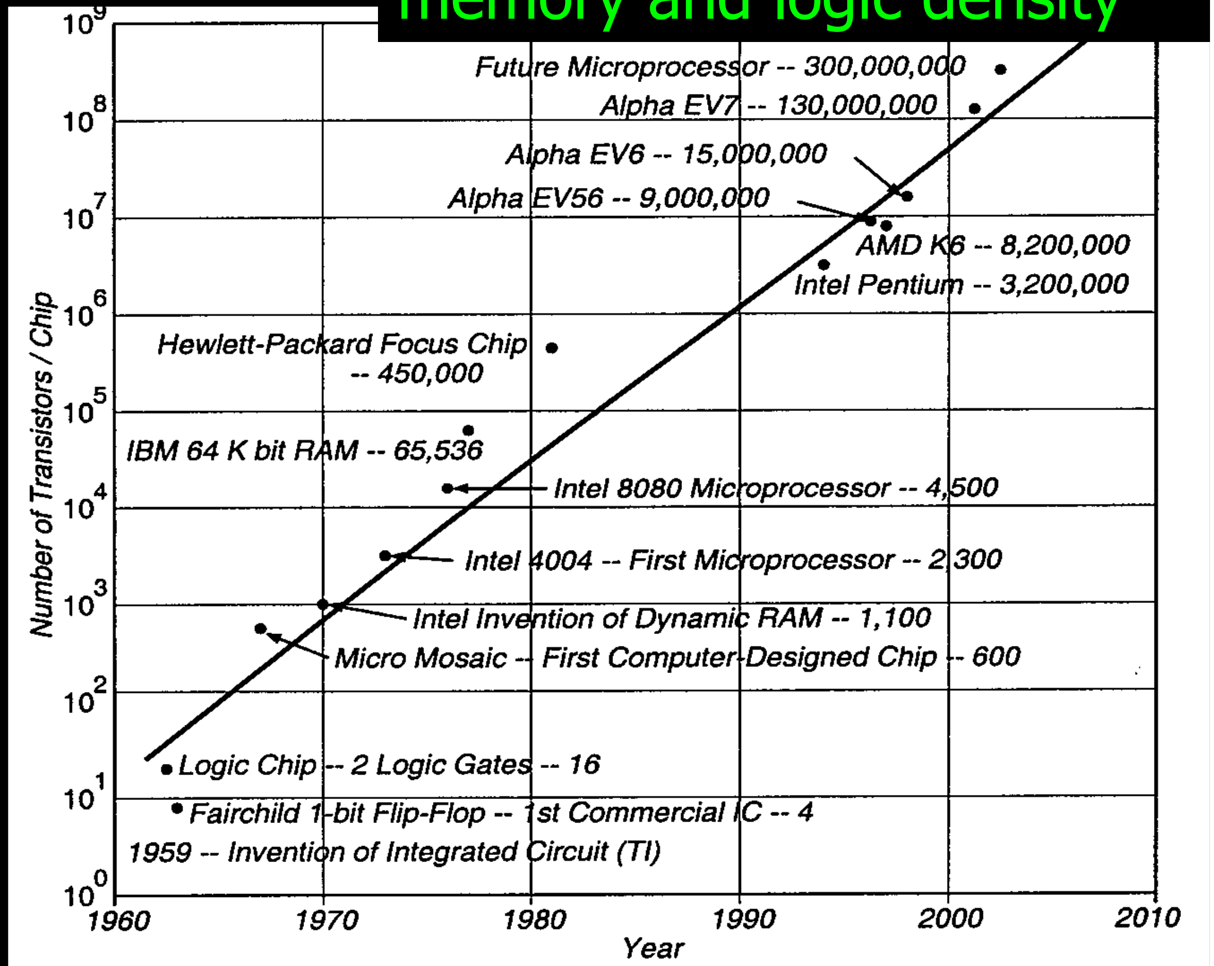




Design is no longer a matter of switches, zeros and ones….
It is about resistors, capacitors, inductors, noise, interference, radiation, etc.

Trends in SoC design & test…… Density

memory and logic density



Consequences

- Test complexity
- High leakage
- Cross talk
- Voltage drop
- Supply bounce
- EMC (electromagnetic compatibility)
- Propagation delay
- Reliability
- Radiation
- ….

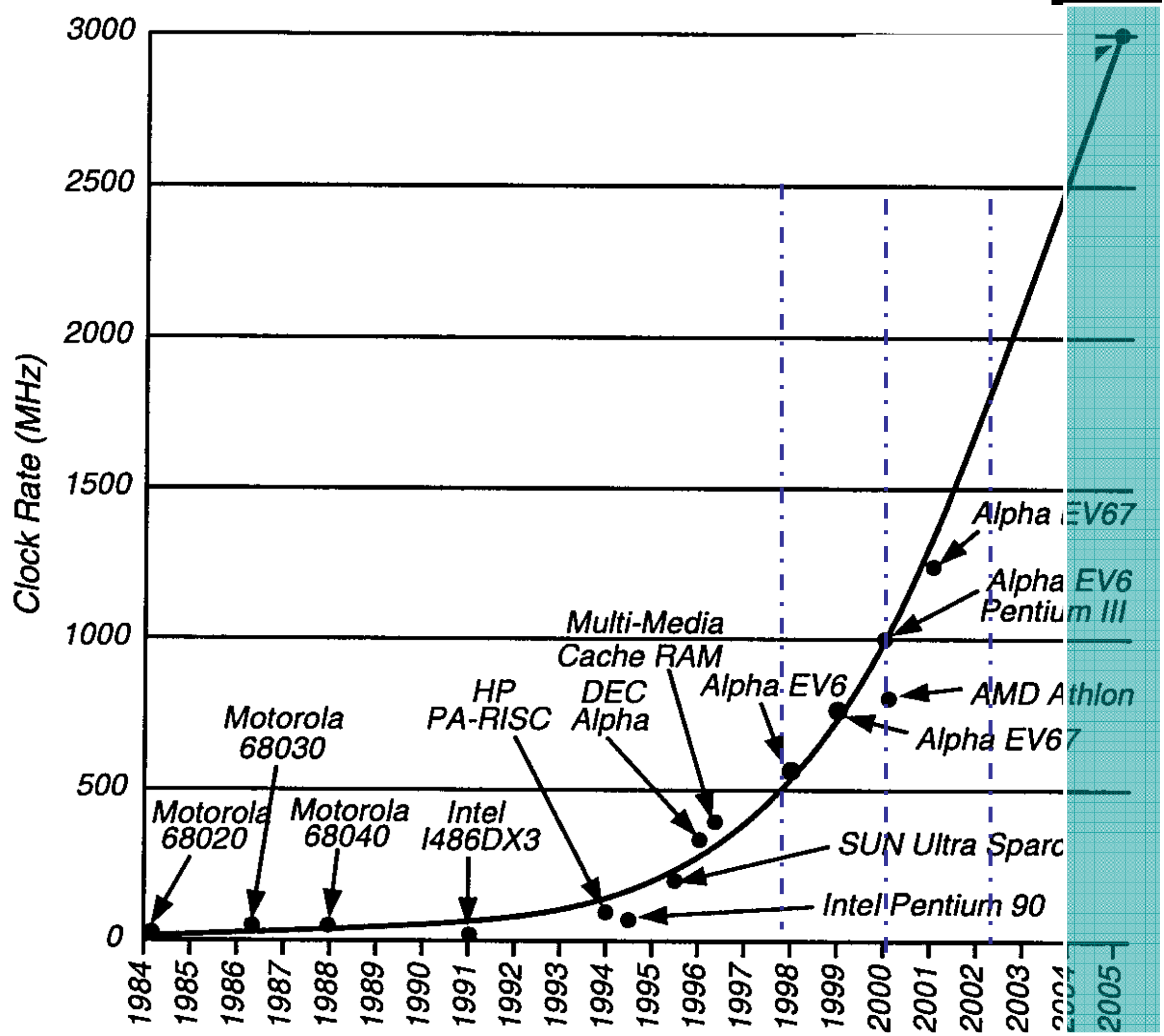
Number of transistors/chip increases ~ 60% per year
(Moore's law, April 1965)

Trends in SoC design & test….. Performance

Consequences

- At speed testing
- Delay testing
- Switching (di/dt) noise
- EMC
- ATE cost (Agilent)
  - ~2M$ +3K$/pin??
  - - Speed ~ 650Mhz??

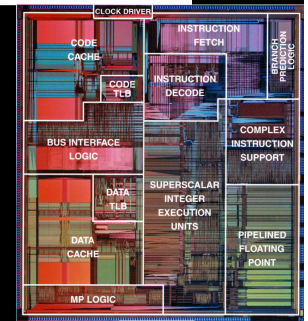
…..

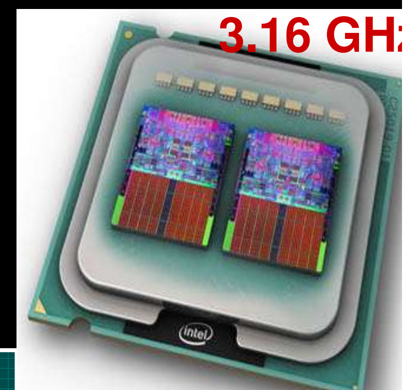


Exponential increase in the clock rate ~60% /year [till ~ 2004]

Trends in SoC design & test ………… multi-core

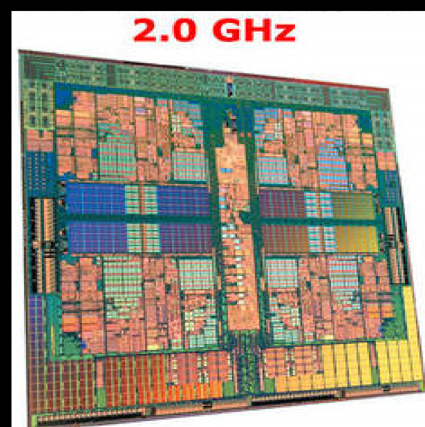
- 2001: Intel warned about the dangers of heat dissipation in processors. Solution: lay in producing chips with multi-cores
- 2004: announcement of dual-core processors
  - Increase productivity, Powerful energy-efficient performance, Leading-edge advanced computing experiences, etc
- Many-core, multi-core will be dominating





Intel dual core

- Consequences on Testing
  - Cross talk, interferences, noise from power lines
  - Test complexity
  - Temperature related faults
  - Process variations (…, 0.13um, 90nm, 65nm, 45nm, 32nm, …)
  - …



AMD Quad Core vs.

Trends in SoC design & test…….

Design is no longer a matter of switchers, zeros and ones….
It is about resistors, capacitors, inductors, noise, interface, radiation, etc.

SoC & scaling impacts e.g.,:

Design

- Increase in the design-productivity gap
- Styles has to be changes to make design manageable
- Design reuse (time-to-market)

Power dissipation

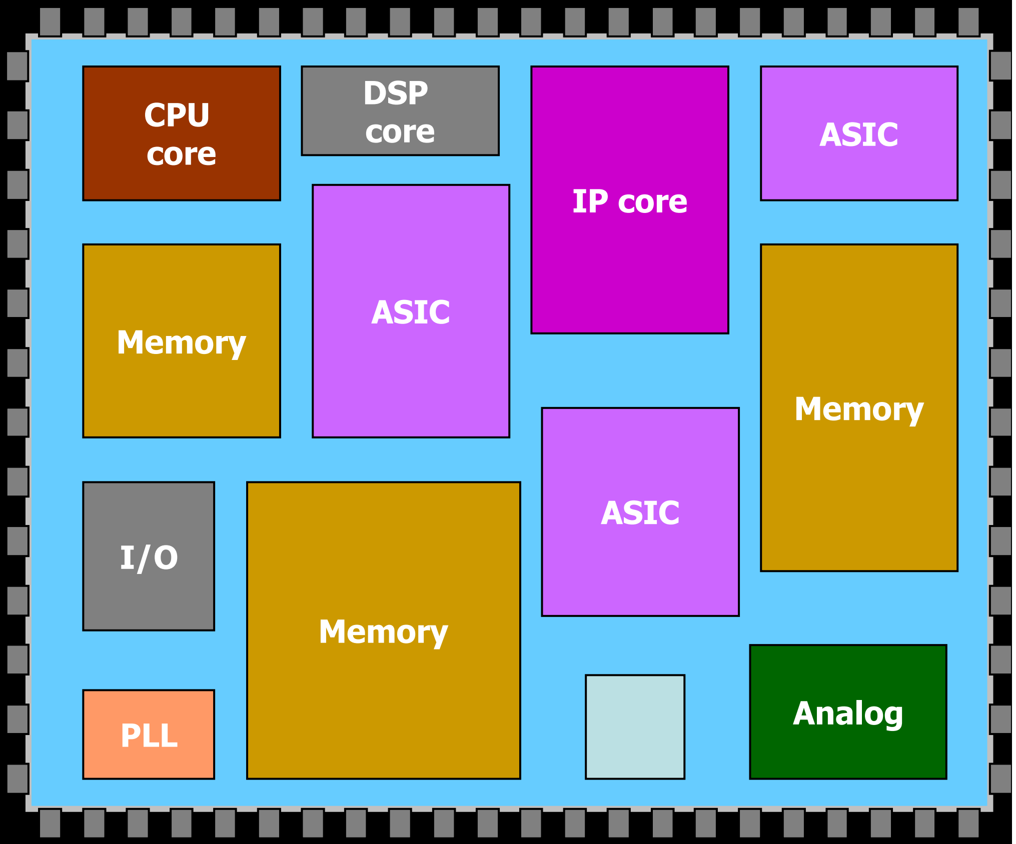
- Lower power design techniques

Testing, Reliability & Sig. Integrity

- Complexity (embedded blocks)
- Time consuming
- Electromigarion
- Signal interference/ Cross talk
- Noise
- …
- …..

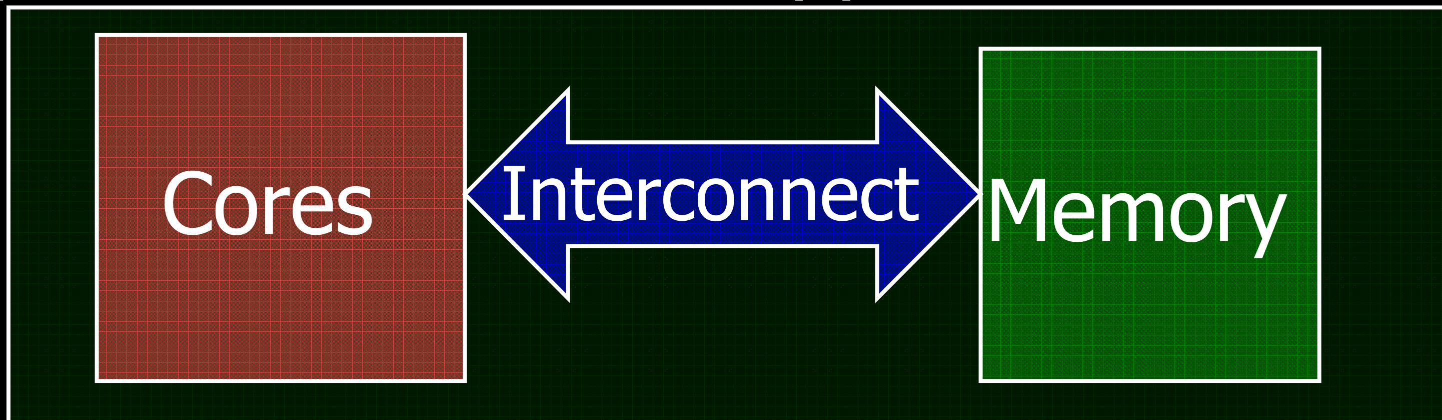
(High cost associated with scaling)

……



Research topics & roadmap @ CE-TUDelft

System/architecture approach



Design for Testability and Reliability

- **Cores**: Multi-core, nano-computing
- **Interconnect**: NOC
- **Memory**:
  - Conventional: SRAM, DRAM
  - Future: PCM, CMOL
- **Computer Aided Test (CAT) Tools**
- New Technology: 3D integration

Some successful stories and ongoing activities...

Altera, San Jose, CA

Taiwan

Belgium

Canada

Intel, CA

Design of Systems on Silicon, Valencia, Spain

MTD, Germany

Infineon Technologies, Munich, Germany

ST Microelectronics, France

Atmel, France

Philips/ NXP, Netherlands

Summary

- Test technology is an integral part of IC design manufacturing
- Test is becoming more important with technology scaling
- Design for testability
- Reliability, FIT, test, fault models, verification
- Yield, Yield loss, DPM, escapes,
- Detection, diagnosis, failure analysis, characterization
- Many challenges due to technology scaling
  - design, manufacturing & test