VLSI Test Technology and Reliability (ET4076)

Lecture 2 (1)

VLSI Test Process and Test Equipment
(Chapter 2)

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Previous lecture

- What is VLSI Test? Why is it needed?
- What is the difference between quality and reliability?
- Is VLSI Test related to design? How?
- What does the rule of ten mean?
- What is the difference between verification and testing?
- What is 'Fault Model', Yield (loss)', 'Escapes'?
- What does DFT mean?
- …

Learning aims of today

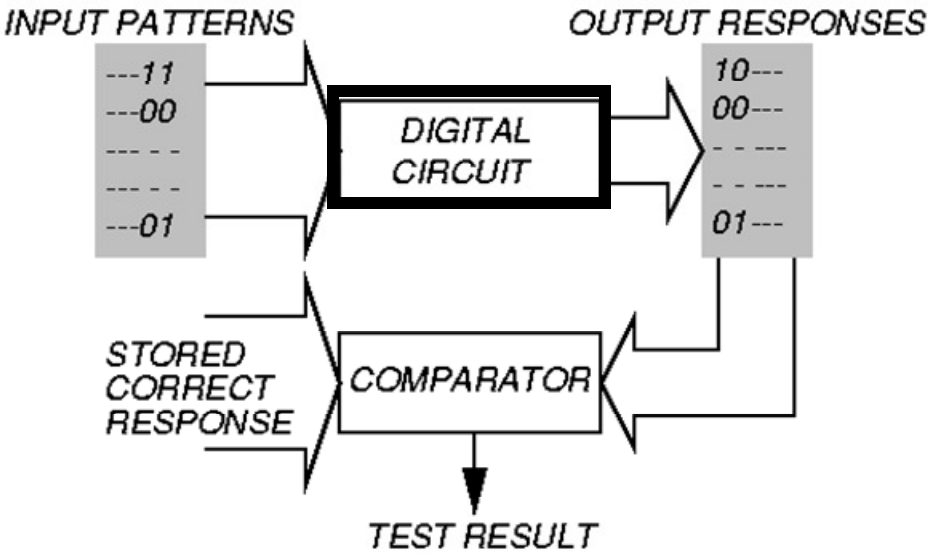
- The explanation of different stages of testing
- The difference between parametric and functional/structural testing
- Basic concept about test program generation
- ATE test cost and ways of reduction

Contents

- Test process
- Test stages
- Test types
- Test program generation
- Automatic Test Equipment

Testing Principle

- Test vectors, expected responses, matching
- VLSI Devices are tested by **Automatic Test Equipment**
  - Powerful computer operating under the control of a **test program**



Test stages

- **Characterization, debug design,** (Verification testing)
- **Manufacturing/production testing**
- **Burn-in (Testing for reliability)**
- **Acceptance testing (incoming inspection)**

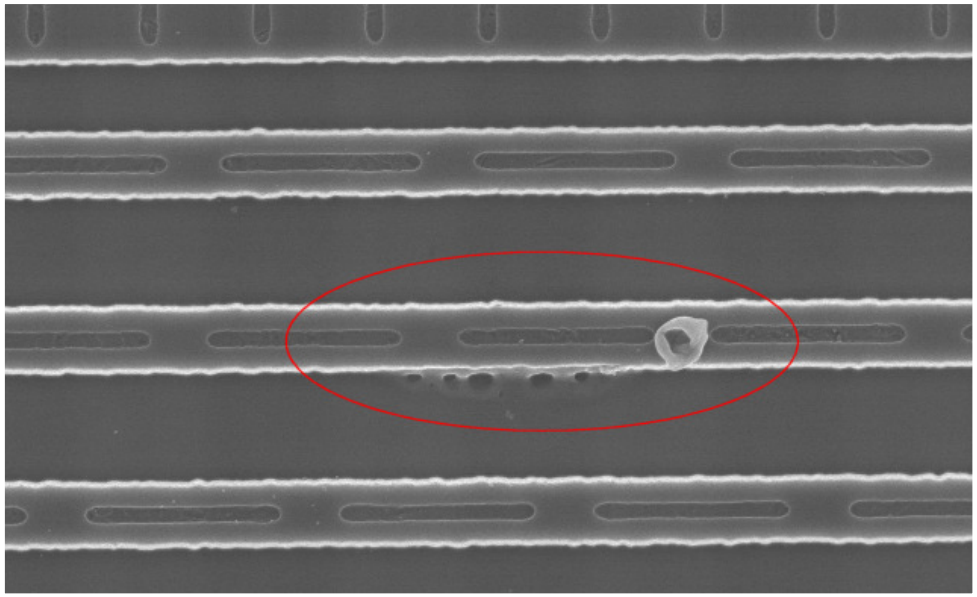
Test stages .....Characterization

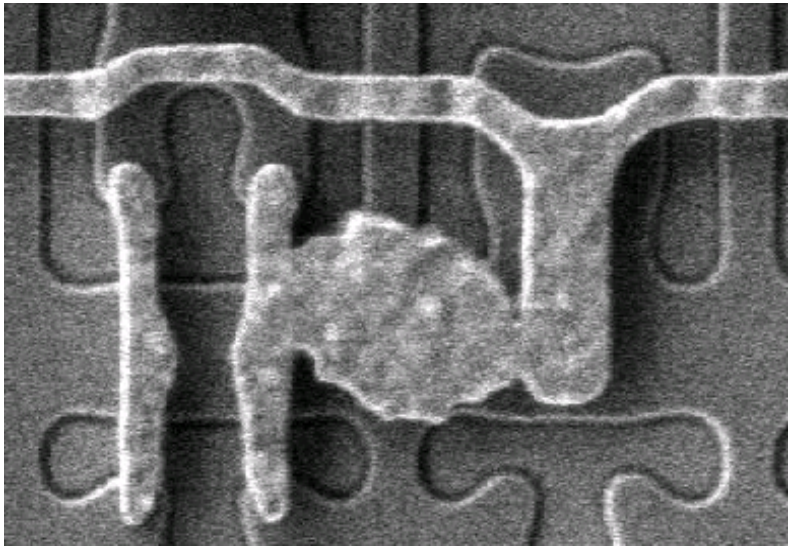
- Verifies correctness of design and of test procedure – usually requires correction to design
- Ferociously expensive
- Performed on a new design before production
- Purpose: verify the correctness+specifications
- Comprehensive AC and DC measurements

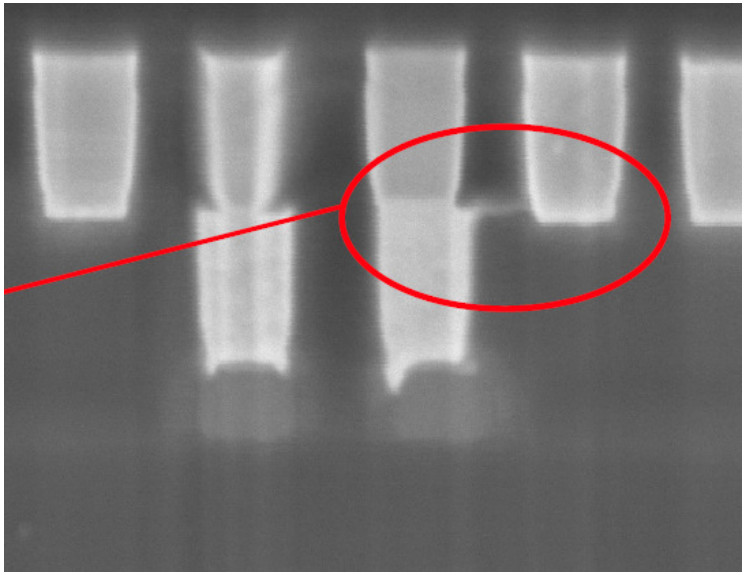
- May comprise:
  - Scanning Electron Microscope (SEM) Testers
  - Bright-Lite detection of defects
  - Electron beam tests
  - Artificial intelligence (expert system) methods
  - Repeated functional tests

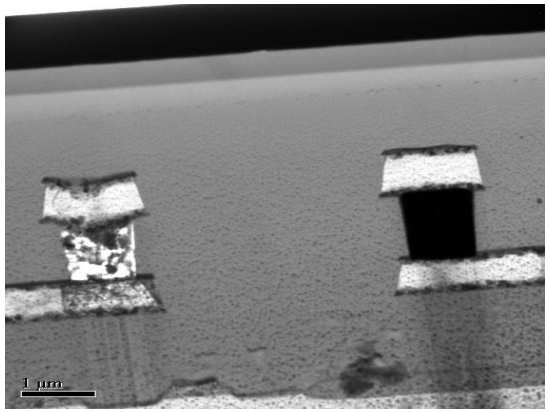
Test stages .....Characterization

Scanning Electron Microscope







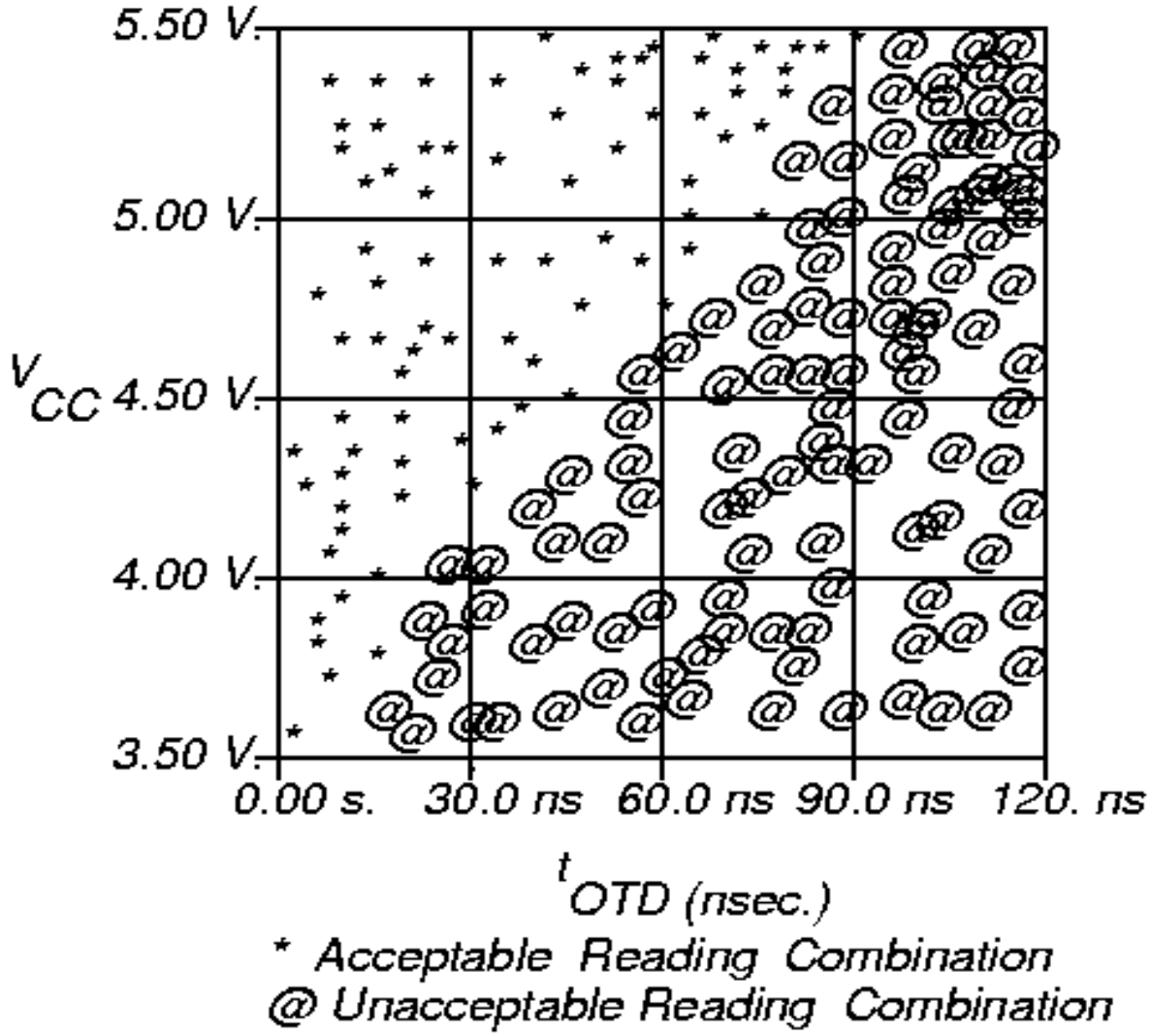


Test stages .....Characterization

- **Determine the exact limits of device operating values**
- **Worst-case test**
  - Choose test that passes/fails chips
  - Select statistically significant sample of chips
  - Repeat test for every combination of 2+ environmental variables (measure various DC & AC parameters***)***
  - Plot results in ***Shmoo plot***
  - Diagnose and correct design errors
  - Develop **production test program**
- **Continue throughout production life of chips to improve design and process to increase yield**

Test stages ……Characterization

Shmoo plot



Test stages …..Production Test

- Determines whether manufactured chip meets specs
- Less comprehensive than characterization tests
- Must cover high % of modeled faults
- Must minimize test time (to control cost)
- No fault diagnosis; not repetitive; go/no-go decision
- Test every device on chip
- Test at speed of application or speed guaranteed by supplier

Test stages …….Burn-in/Stress Test

- **Process:**
  - Subject chips to high temperature & over-voltage supply, while running production tests
- **Coverage:**
  - ***Infant mortality***
    - These are damaged chips that will fail in the first 2 days of operation
    - Causes bad devices to actually fail before chips are shipped to customers
    - Short term burning (10-30 hours)
    - Failures due to sensitive design and process variations
  - ***Freak failures***
    - Devices having same failure mechanisms as reliable devices
    - Long term burning (100-1000 hours)
- **Very expensive! (balance the cost against reliability requirements)**

Test stages ……Incoming Inspection

- **Purpose**:
  - Avoids putting defective device in a system where cost of diagnosis exceeds incoming inspection cost
- Often done for a random sample of devices
  - *Sample size* depends on device quality and system reliability requirements
- **Can be:**
  - Similar to production testing
  - More comprehensive than production testing
  - Tuned to specific systems application

Manufacturing level tests

- Wafer sort or probe
  - Test site characterization
- Packaged device tests

Manufacturing level tests

- ***Wafer sort* or *probe*** test – done before wafer is scribed and cut into chips
  - Includes test site characterization – specific test devices are checked with specific patterns to measure:
    - Gate threshold
    - Polysilicon field threshold
    - Poly/contact sheet resistance, etc.

Test types: content based

- ***Parametric (DC and AC) tests***
- ***Functional tests/ Structural tests***

Test types: content based

- ***Parametric (DC and AC) tests***

  Measures electrical properties of pin electronics: (fast and cheap)
  - DC: contact, max I, leakage, threshold, ..
  - AC: delay test, set up and hold time, at speed,..

- ***Functional/structural tests***
  - Used to cover very high % of modeled faults
  - Test every transistor and wire in digital circuits
  - Long and expensive
  - May use different stresses (e.g., guardband)
  - **Main topic of course**

Test types…….Electrical/ Parametric

- Observed at the chip pins
- Test modifies observed voltage/current/delay @pin
- **Two types of electrical faults**:
  - Major deviation from the specs
  - Unacceptable limits of operation
- **They consist of:**
  - **Contact test**
    - Test pins for opens and shorts
  - **DC Tests**
    - Measure steady state electrical characteristics using Ohm's law
  - **AC tests**
    - Perform measurements using alternative voltages at some frequencies

Test types …….DC Parametric Tests

- **Power Consumption:**

  Find worst-case power consumption for static and dynamic situations (measure the max current drawn at specified voltage)

- **Output Short Current**

  verify that the output current drive is sustained at high and low output voltage

- **Output Drive Current**

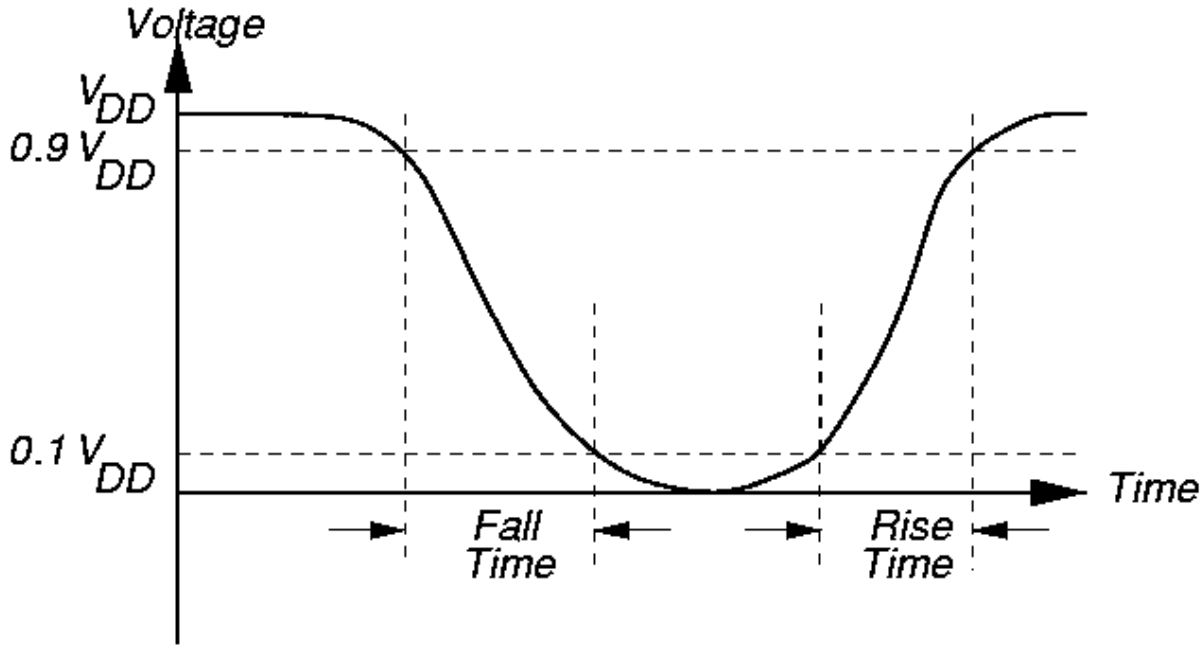
  For a specified output device current, verify that the output voltage is maintained

- **Threshold**

  Determine V_{IL}, V_{IH} , V_{OL} and V_{OH}

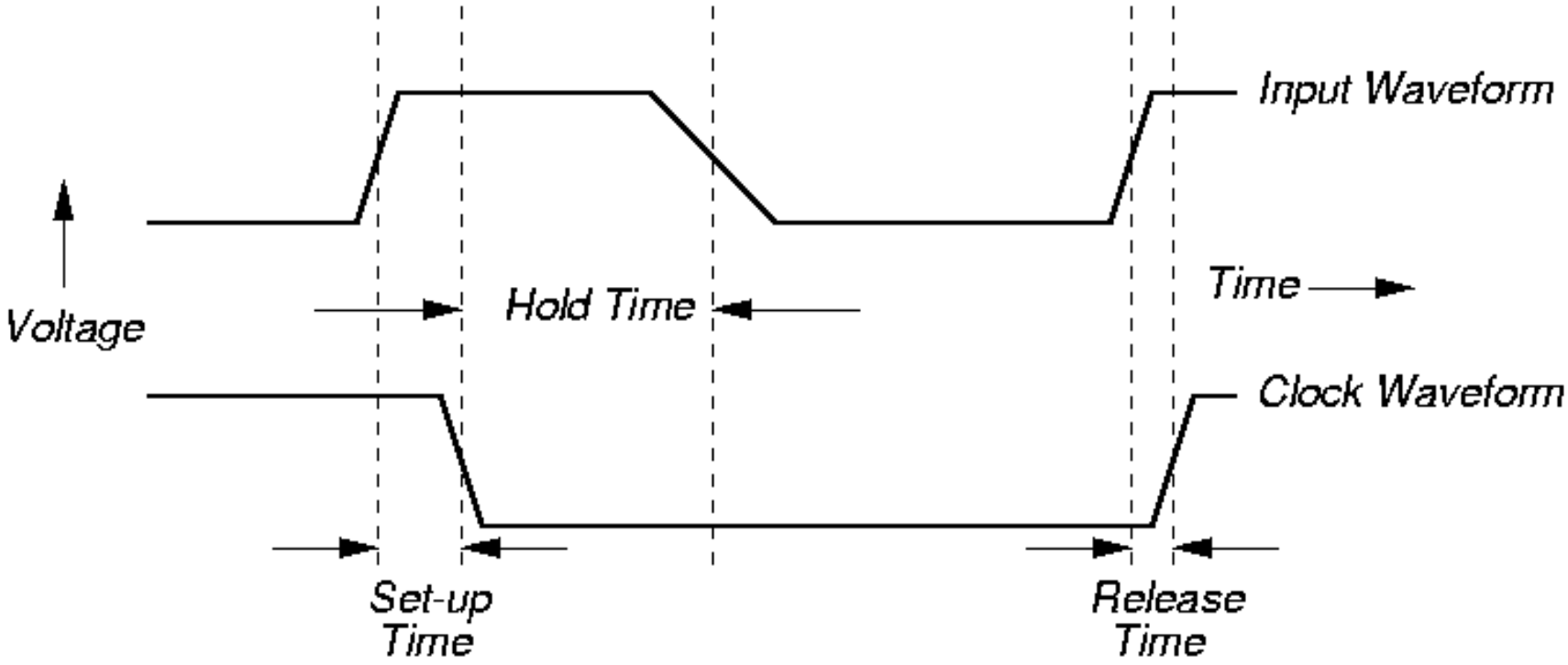
Test types …….AC Parametric Tests

- Set-up and Hold Time tests
- Propagation Delay tests
- Rise and Fall Time tests



Test types ……. AC Parametric Tests

- Set-up and Hold Time tests

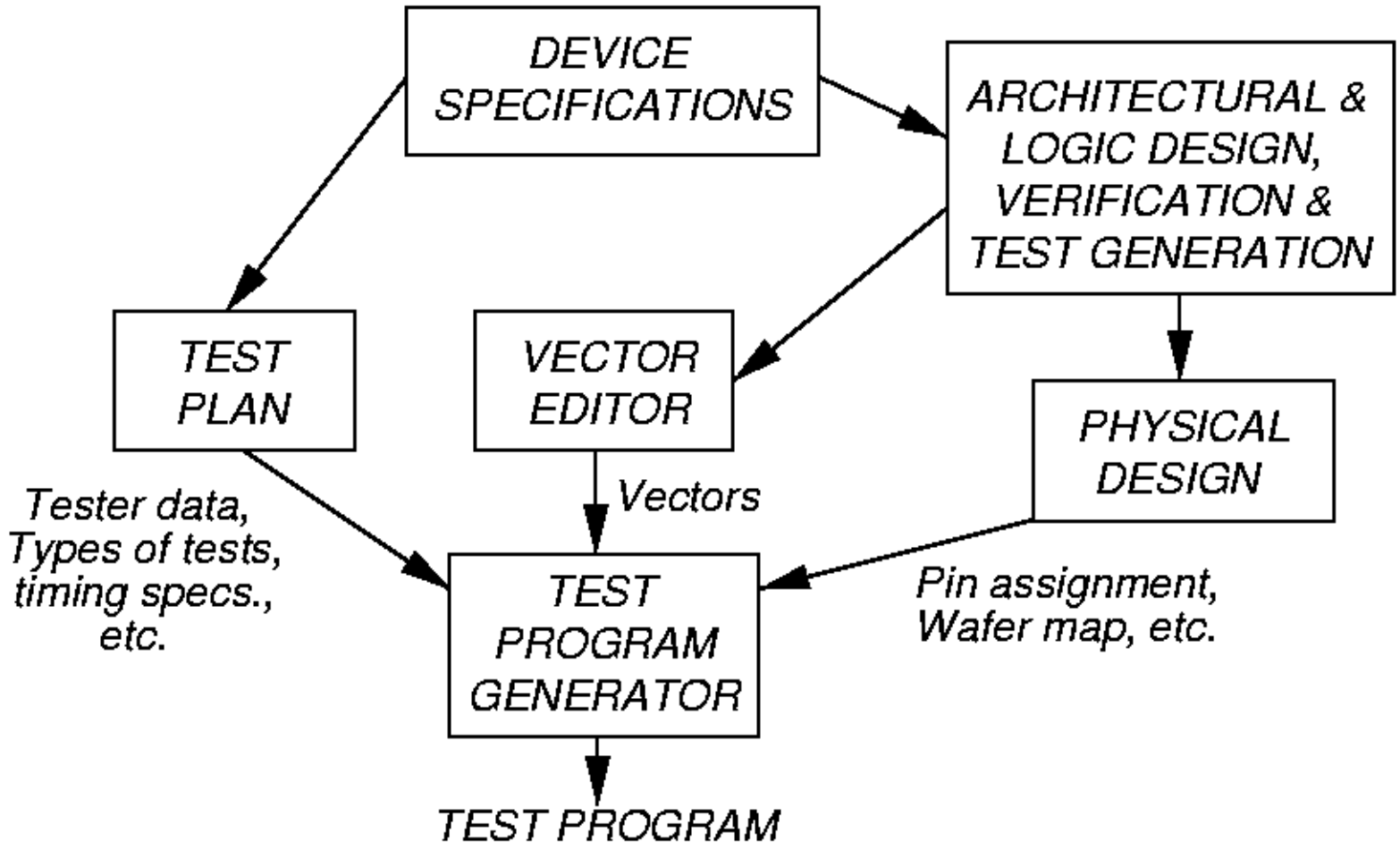


Test Specifications, plan and generation

- **Test Specifications:**
  - Functional Characteristics (IO timing, Algorithms, …)
  - Type of *Device Under Test* (DUT)
  - Physical Constraints – Package, pin numbers, etc.
  - Environmental Characteristics – supply, temperature, humidity, etc.
  - Reliability – acceptance quality level (defects/million), failure rate, etc.

- **Test plan generated from specifications**
  - Type of test equipment to use
  - Types of tests
  - Fault coverage requirement

Test Specifications, plan and generation



Test Specifications, plan and generation

Test Data Analysis

- **Uses of ATE test data:**
  - Reject bad DUTs
  - Fabrication process information
  - Design weakness information
- **Devices that did not fail are good only if tests covered 100% of faults**
- ***Failure mode analysis* (FMA)**
  - Diagnose reasons for device failure, and find design and process weaknesses
  - Allows improvement of logic & layout design rules

Automatic Test Equipment (ATE)

- Apply test pattern to ***device under test DUT***
- Analyze responses from DUT
- Mark DUT as good or bad

ADVANTEST
Model T6682 ATE

(one Test Head)

Automatic Test Equipment Components

- ***Powerful computer***
- **Test Program** (e.g., written in Test Description Language)
- ***Test head*** interface through custom printed circuit board to *wafer prober* (unpackaged chip test) or *package handler* (packaged chip test), touches chips through a socket (*contactor)*
- ***Probe card –*** custom *printed circuit board* (PCB) on which DUT is mounted in socket – may contain custom measurement hardware (current test). Interfaces ATE test head to set of probe needles
- ***Probe needles* (*Membrane probe*)–** come down and scratch the pads to stimulate/read pins
- ***Pin electronics* (PE) –** electrical buffering circuits, put as close as possible to DUT (*Channels;* e.g., 1024)
- …

T6682 ATE Specifications*

- Uses 0.35 μm VLSI chips in implementation
- 1024 pin channels
- Speed: 250, 500, or 1000 MHz
- Timing accuracy: +/- 200 ps
- Drive voltage: -2.5 to 6 V
- Clock/strobe accuracy: +/- 870 ps
- Clock settling resolution: 31.25 ps
- *Pattern multiplexing*: write 2 patterns in one ATE cycle
- *Pin multiplexing*: use 2 pins to control 1 DUT pin

ATE Major Cost Reduction

- **Multi-site Testing**
  - One ATE tests several devices at the same time
  - For both probe and package test
  - DUT interface board has > 1 socket
    - Test head designed to handle more multiple packages simultaneously
  - Add more instruments to ATE to handle multiple devices simultaneously
  - Usually test 2 or 4 DUTs at a time, usually test 32 or 64 memory chips at a time
  - Limits:
    - # instruments available in ATE to handle all of the required pins
    - Type of handling equipment available for a given package type
- **DFT methods and Built-In Self-Test**

Automatic Test Equipment

- LTX FUSION HF ATE

Summary

- Type of testing
- Parametric tests versus Functional tests
- Typical test program
- ATE
  - Cost Problems
    - Pin inductance (expensive probing)
    - Multi-GHz frequencies
    - High pin count (1024)
  - ATE Cost Reduction
    - Multi-Site Testing
    - DFT and Built-In Self-Test