VLSI Test Technology and Reliability (ET4076)

Lecture 2 (p2)

Fault Modeling

(Chapter 4)

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Previous lecture

- What are the different test stages?
- What is the difference between parametric and functional/structural testing? Give examples.
- What does DUT, ATE, and multi-site testing mean?
- How can be ATE cost reduced?
- ..

Learning aims of today

- Describe the difference between a defect and a fault model
- Describe some common defects
- Describe common used fault models
- Define the fault set of a combinational circuits
- Use the concept of fault equivalence and fault dominance to reduce the fault set

Contents

- Functional versus structuring testing
- Level of abstraction
- Why model faults?
- Failure mechanisms
- Defect classification
- Common fault models
- Stuck-at faults
  - Single stuck-at faults
  - Fault equivalence
  - Fault dominance and checkpoint theorem
  - Classes of stuck-at faults and multiple faults
- Transistor faults

Some definitions

- **Defect**
  - An **unintended** difference between the implemented hardware and its intended design
  - E.g., process defects, age defects, …
- **Error** of faulty behavior
  - A **wrong** output signal produced by a defective system.
  - An "effect" whose cause is some "defect"
- **Fault model**
  - A representation of a "defect" at an "abstract function level"

Functional versus structural testing

- Assume 10 input AND function
  - To guarantee that the circuit function correctly, 2^{10} =1024 input patterns needs to be evaluated
  - Too long test time
  - Not realistic for real circuits (with several hundred of inputs)
  - **This is Functional Test**
  - Useful for verification of design (before manufacturing)

- **Structural test**
  - Use fault models
  - Allow the development of test algorithms
  - Reduces the test complexity
  - (Technology independent fault models and tests)

Model and level of abstraction

Increasing level of abstraction

Behavioral

Functional

Logical

Electrical

Layout

If (cond) then read (x)

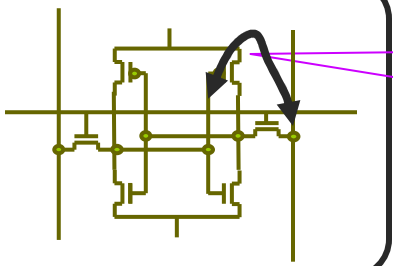
Behavioral fault

Column decoder

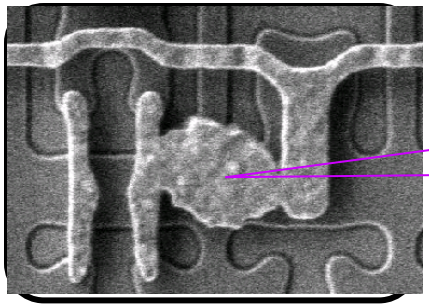
Row decoder

Memory array

Functional fault; Stuck-at-fault



Electrical fault

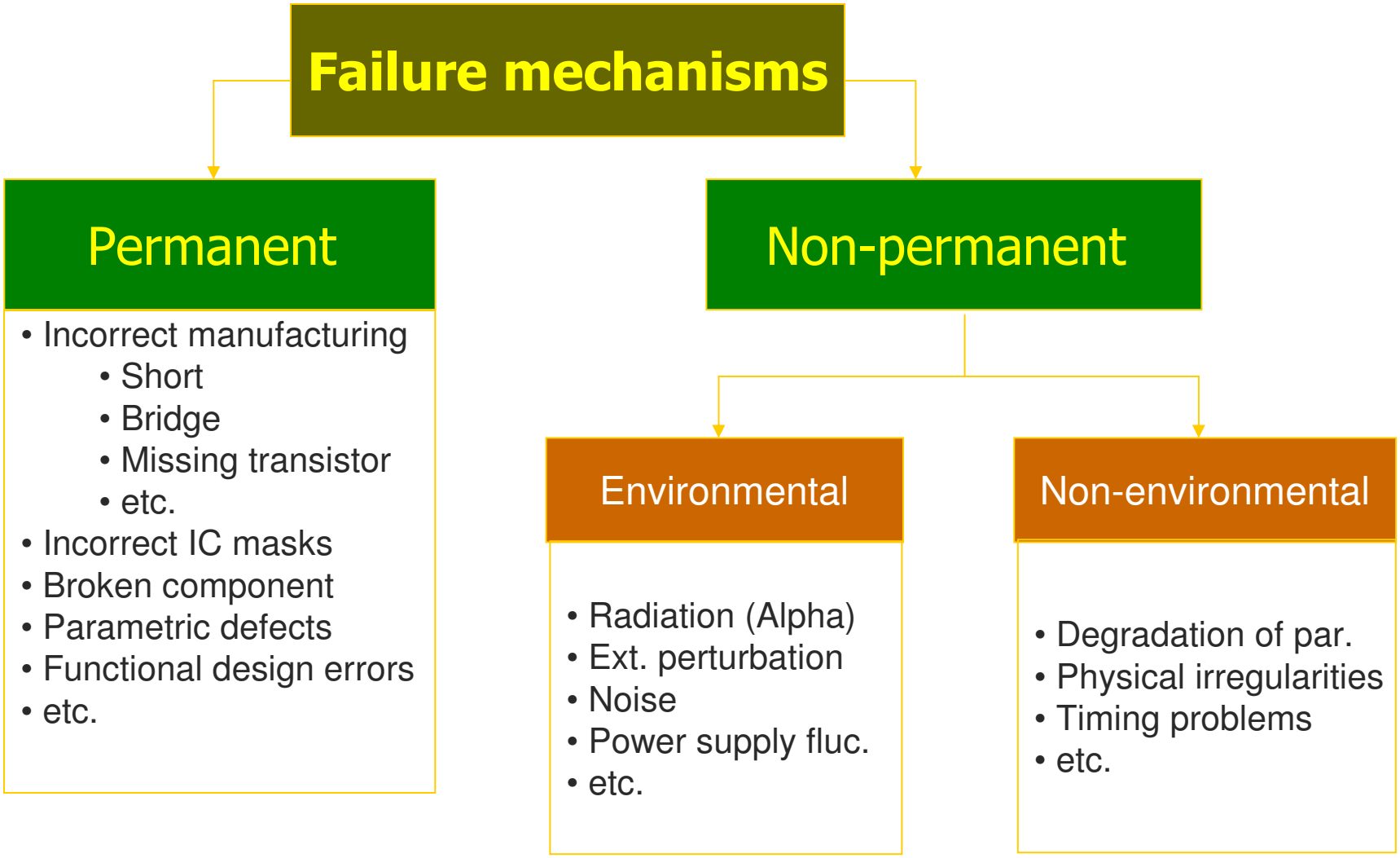


Defect

Why Model Faults?

- I/O function tests inadequate for manufacturing (functionality versus component and interconnect testing)
- Real defects (often mechanical) too numerous and often not analyzable
- A fault model identifies targets for testing
- A fault model makes analysis possible
- Effectiveness measurable by experiments

Failure mechanisms.....*Classification*



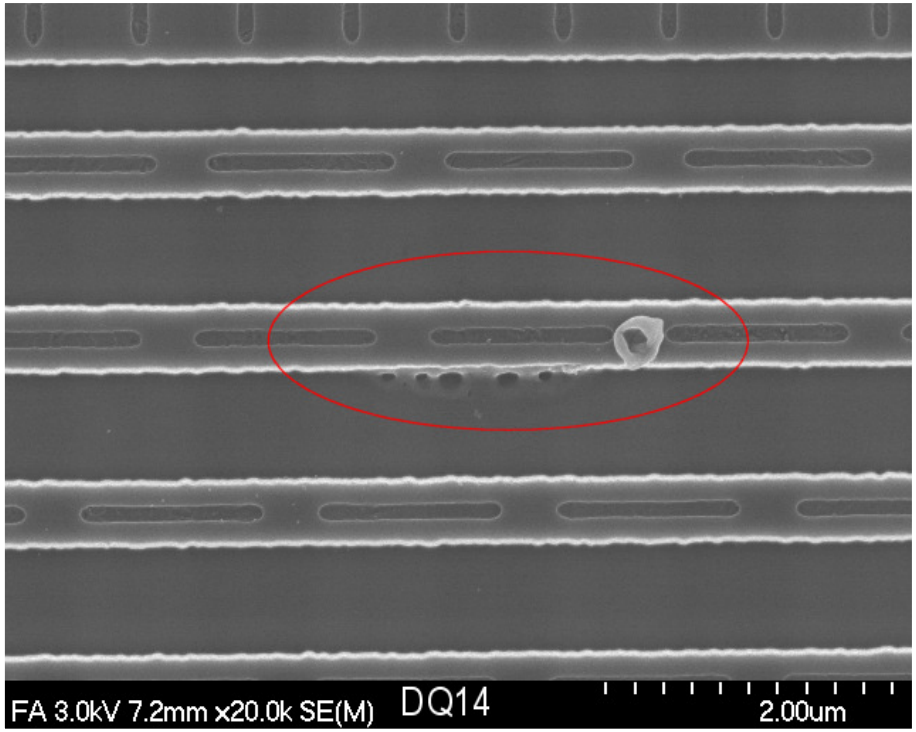
Failure mechanisms

Real Defects in Chips

- Processing defects
  - Missing contact windows
  - Parasitic transistors
  - Oxide breakdown
  - . . .
- Material defects
  - Bulk defects (cracks, crystal imperfections)
  - Surface impurities (ion migration)
  - . . .
- Time-dependent failures
  - Dielectric breakdown
  - Electromigration
    - . . .
- Packaging failures
  - Contact degradation
  - Seal leaks
  - . . .

Failure mechanisms.... *Use of copper*

- Example of open defects on the data lines of memory, found by failure analysis using scanning electron microscopy (SEM)
- Cause permanent and delay faults
- Copper wiring is difficult to deposit on silicon which causes opens

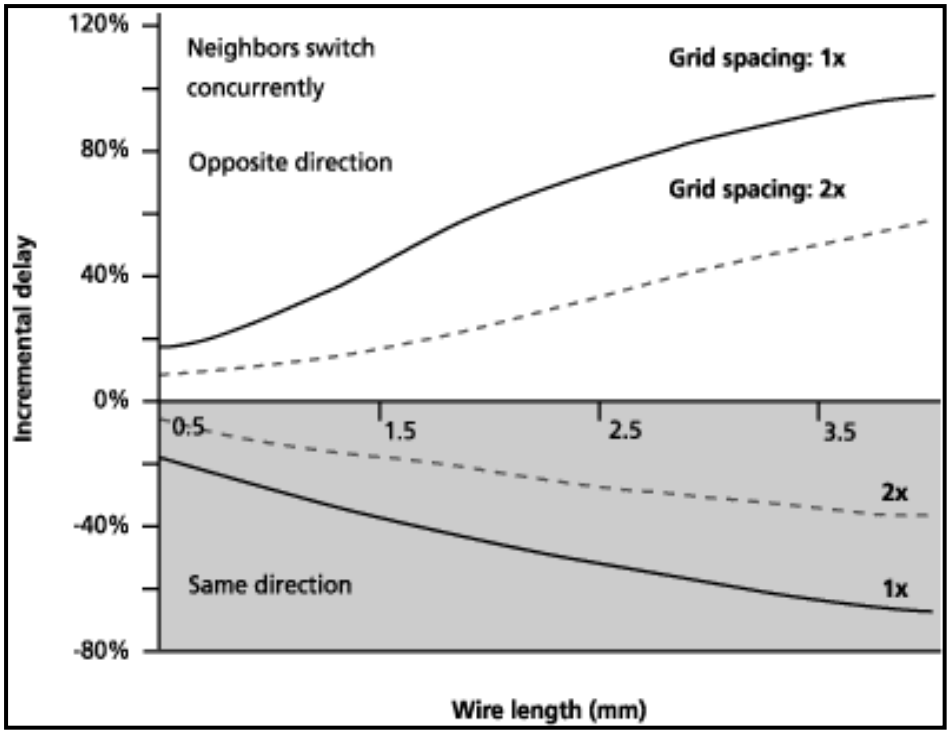


Ref. Infineon, DE

Manufacturing shift toward copper wiring
Increases susceptibility to opens

Failure mechanisms..... *Cross talk*

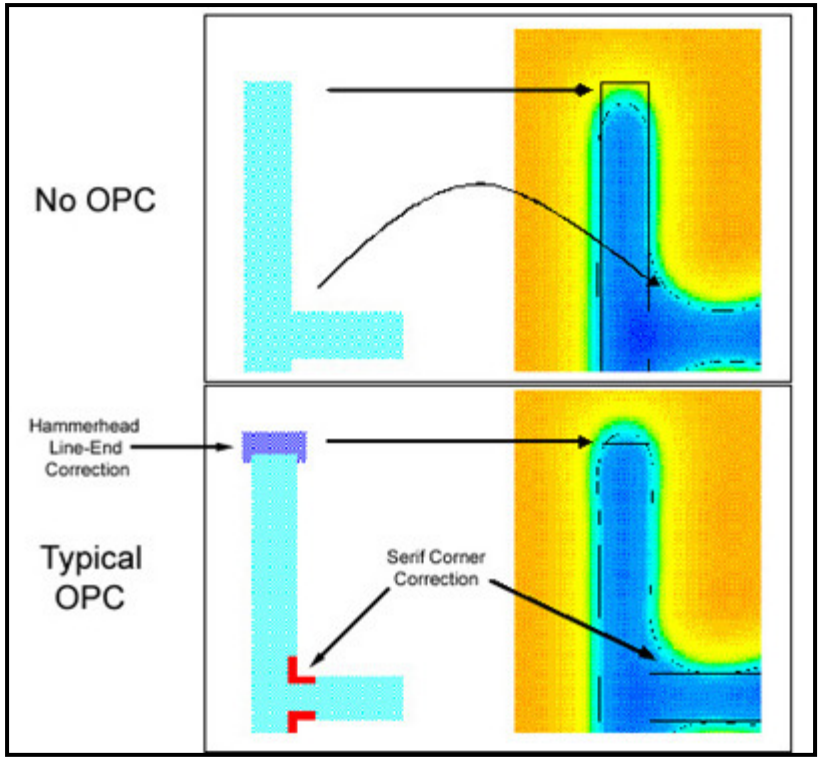
- Crosstalk and delay increase with:
  - increasing wire length
  - shrinking dimensions
- Delay causes non-permanent faults
- These faults are difficult to detect
- Becomes a hot topic with scaling technology



Continued increase in integration density increases susceptibility to crosstalk

Failure mechanisms .. *Proximity effects*

- Small feature sizes are difficult to manufacture due to proximity effects
- Optical proximity correction (OPC) improves the quality of shapes on silicon
- Correction algorithms are becoming too complex



Ref: Synopsys website

Continued decrease in feature sizes increases on-chip variations in behavior

Observed *PCB* Defects

Defects on Printed Circuit Board (PCB) are different from that of VLSI chips

Defect classes	**Occurrence frequency (%)**
Shorts	51
Opens	1
Missing components	6
Wrong components	13
Reversed components	6
Bent leads	8
Analog specifications	5
Digital logic	5
Performance (timing)	5

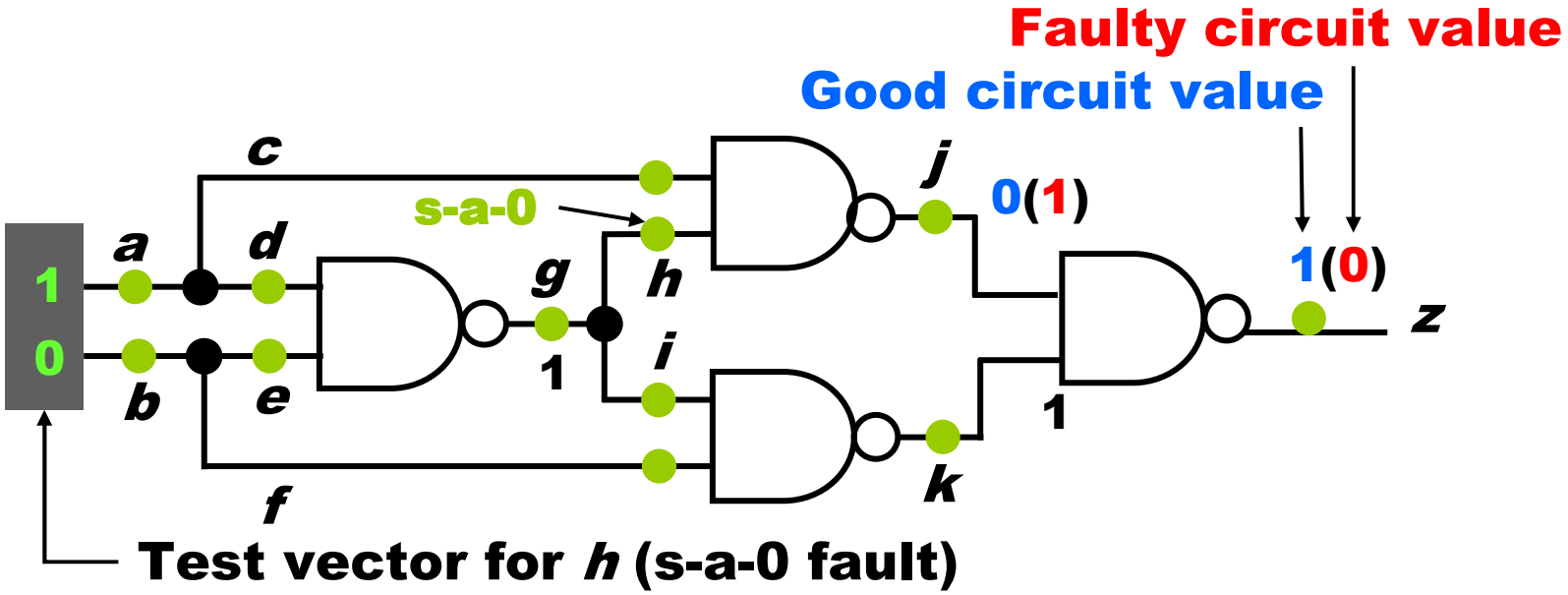
Ref.: J. Bateson, *In-Circuit Testing*, Van Nostrand Reinhold, 1985.

Common Fault Models

- **Single stuck-at faults**
- **Bridging faults**
- PLA faults (missing cross-point, extra cross-point, …)
- **Delay faults** (transition, path, …)
- **Intermittent faults** (appears and disappear within ΔT)
- **Memory faults**
- **Multiple faults**
- **Transistor faults** (stuck-open and stuck-short faults)
- Behavior faults (processors: instruction fault, branch fault,)
- Analog faults
- …
- For more examples, see the book (p. 60-70)

Single stuck at fault!!!

- Three properties define a single stuck-at fault
  - Only one line is faulty
  - The faulty line is permanently set to 0 or 1
  - The fault can be at an input or output of a gate
- Example: XOR circuit has 12 fault sites (●) and 24 single stuck-at faults
  - Fault sensitization, Fault propagation, Line justification



Fault equivalence

- Number of fault sites in a Boolean gate circuit:
  = #PI + #gates + # (fanout branches).

- **Fault equivalence:**

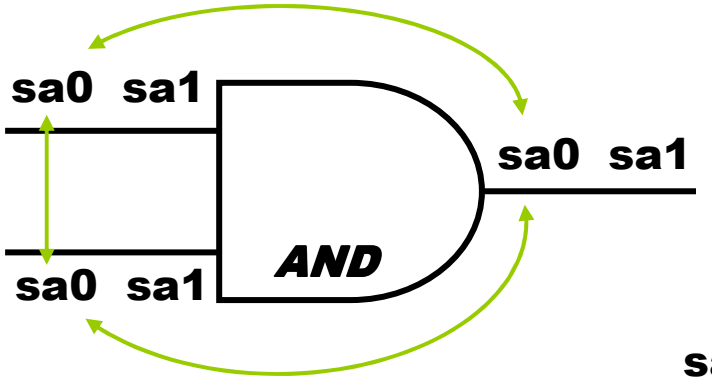
  Two faults f1 and f2 are equivalent if all tests that detect f1 (f2) also detect f2 (f1).

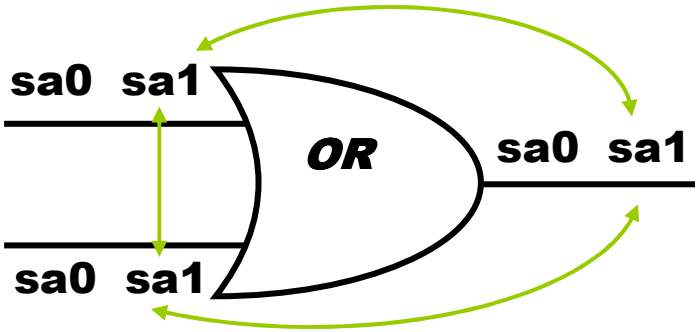
- If faults f1 and f2 are equivalent then the corresponding faulty functions are identical (*indistinguishable*).

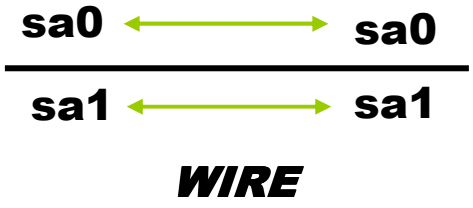
- **Fault collapsing:**

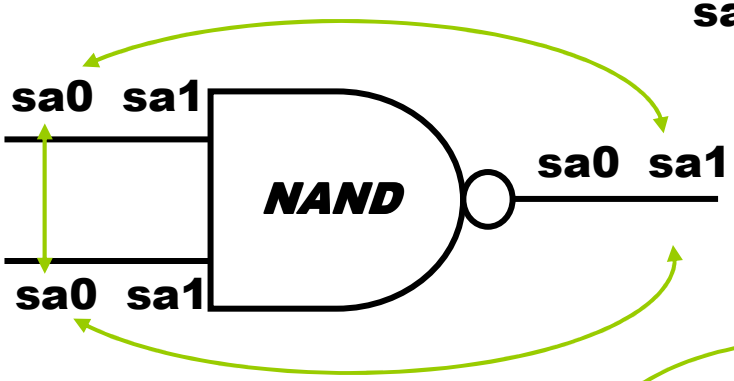
  All single faults of a logic circuit can be divided into disjoint equivalence subsets, where all faults in a subset are mutually equivalent. A collapsed fault set contains one fault from each equivalence subset.

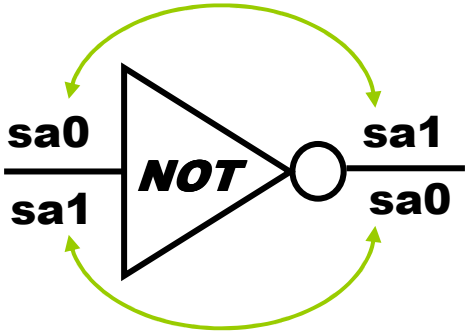
Fault equivalence…. Equivalence rules

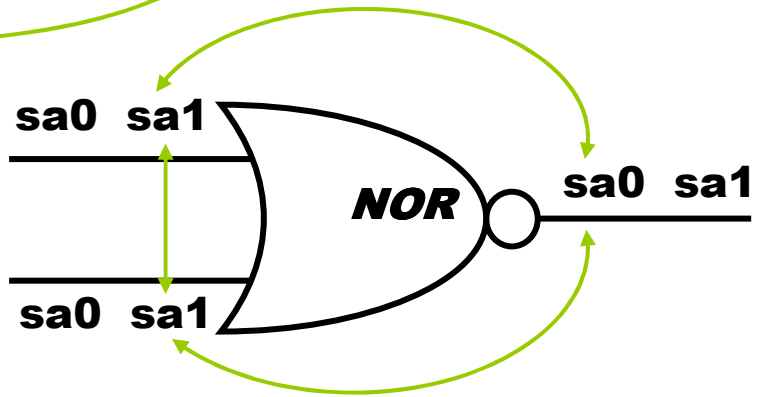


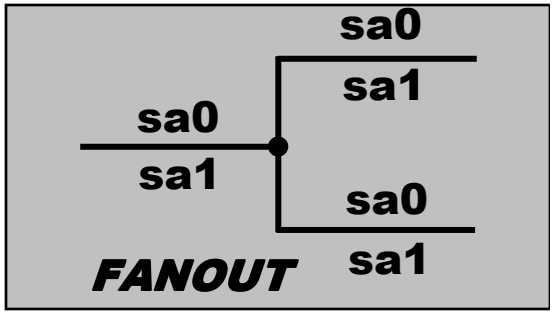




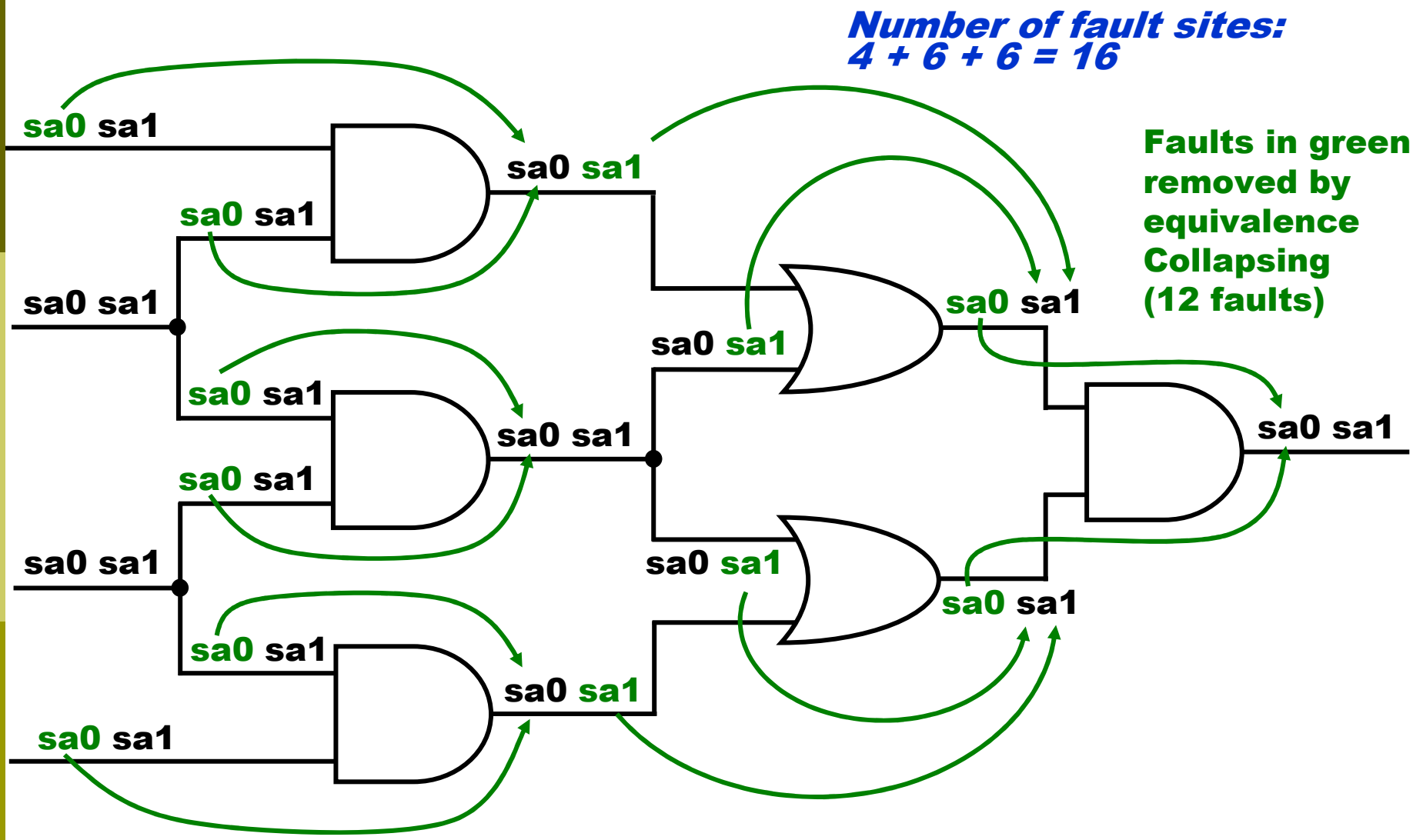








Fault equivalence…… Example

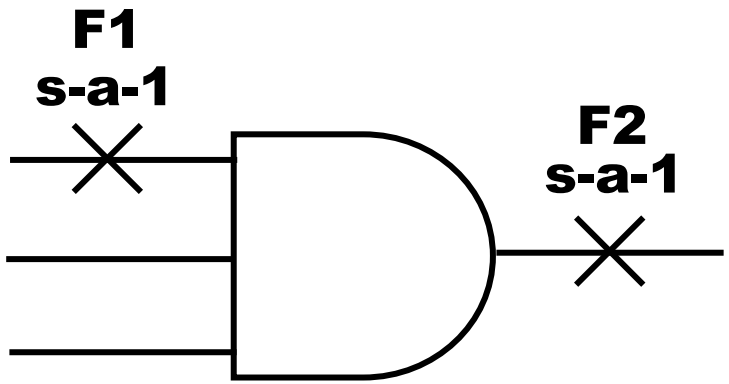


$$\text{Collapse ratio} = \frac{20}{32} = 0.625$$

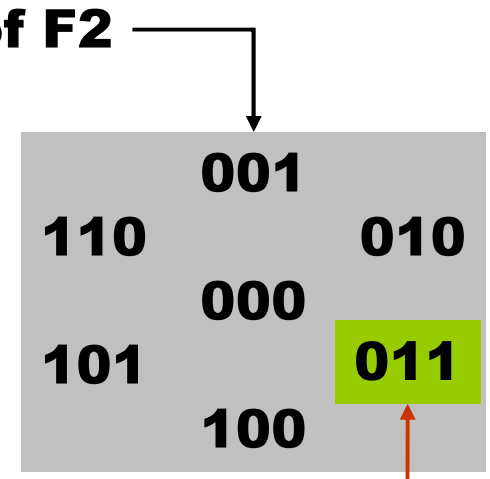
Fault dominance

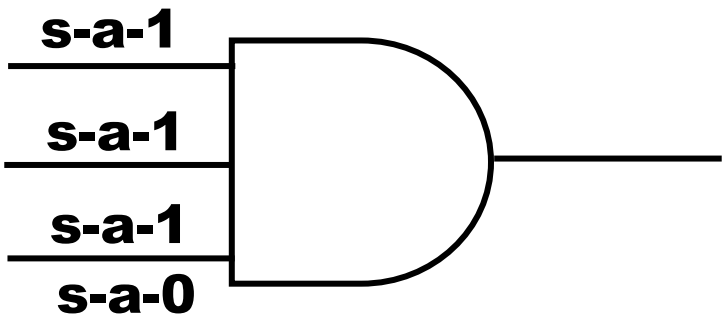
- If **all** tests of some fault F1 detect another fault F2, then F2 is said to **dominate** F1.
- Dominance fault collapsing: If fault F2 dominates F1, then F2 is removed from the fault list.
- When dominance fault collapsing is used, it is sufficient to consider only the input faults of Boolean gates. See the next example.
- In a tree circuit (without fanouts) PI faults form a dominance collapsed fault set.
- If two faults dominate each other then they are equivalent.

Fault dominance…… Example



F2 dominates F1



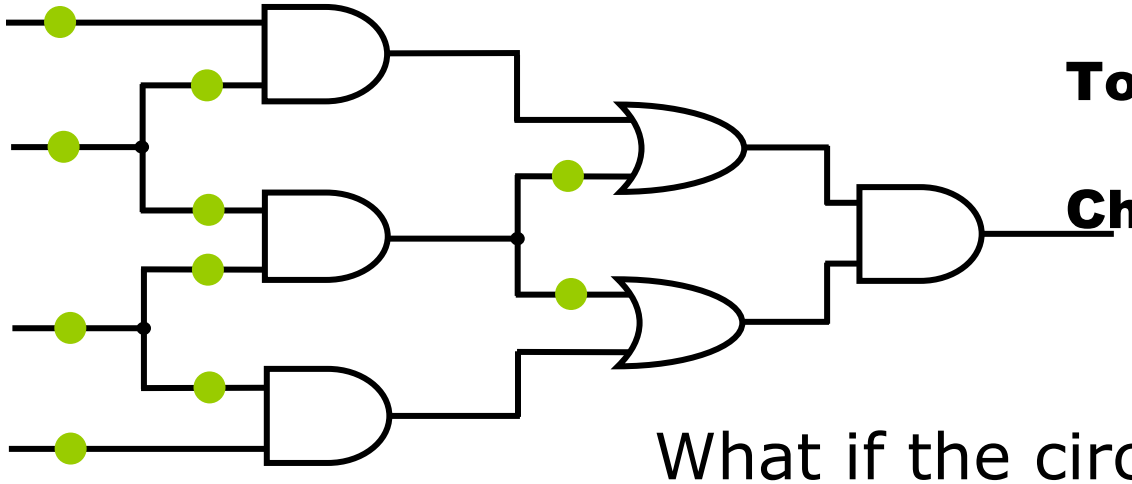


A dominance collapsed fault set

Checkpoints

- Primary inputs and fanout branches of a combinational circuit are called ***checkpoints***.

- **Checkpoint theorem**: A test set that detects all single (multiple) stuck-at faults on all checkpoints of a combinational circuit, also detects all single (multiple) stuck-at faults in that circuit.



Total fault sites = 16

Checkpoints (●) = 10

What if the circuit has no fanout?

Classes of stuck-at faults

- Following classes of single stuck-at faults are identified by fault simulators:
  - ***Potentially-detectable fault*** -- Test produces an unknown (X) state at *primary output* (PO); detection is probabilistic, usually with 50% probability.
  - ***Redundant fault*** -- No test exists for the fault.
  - ***Untestable fault*** -- Test generator is unable to find a test.
  - *Initialization fault* -- Fault prevents initialization of the faulty circuit; can be detected as a potentially-detectable fault.
  - *Hyperactive fault* -- Fault induces much internal signal activity without reaching PO.

Multiple Stuck-at Faults

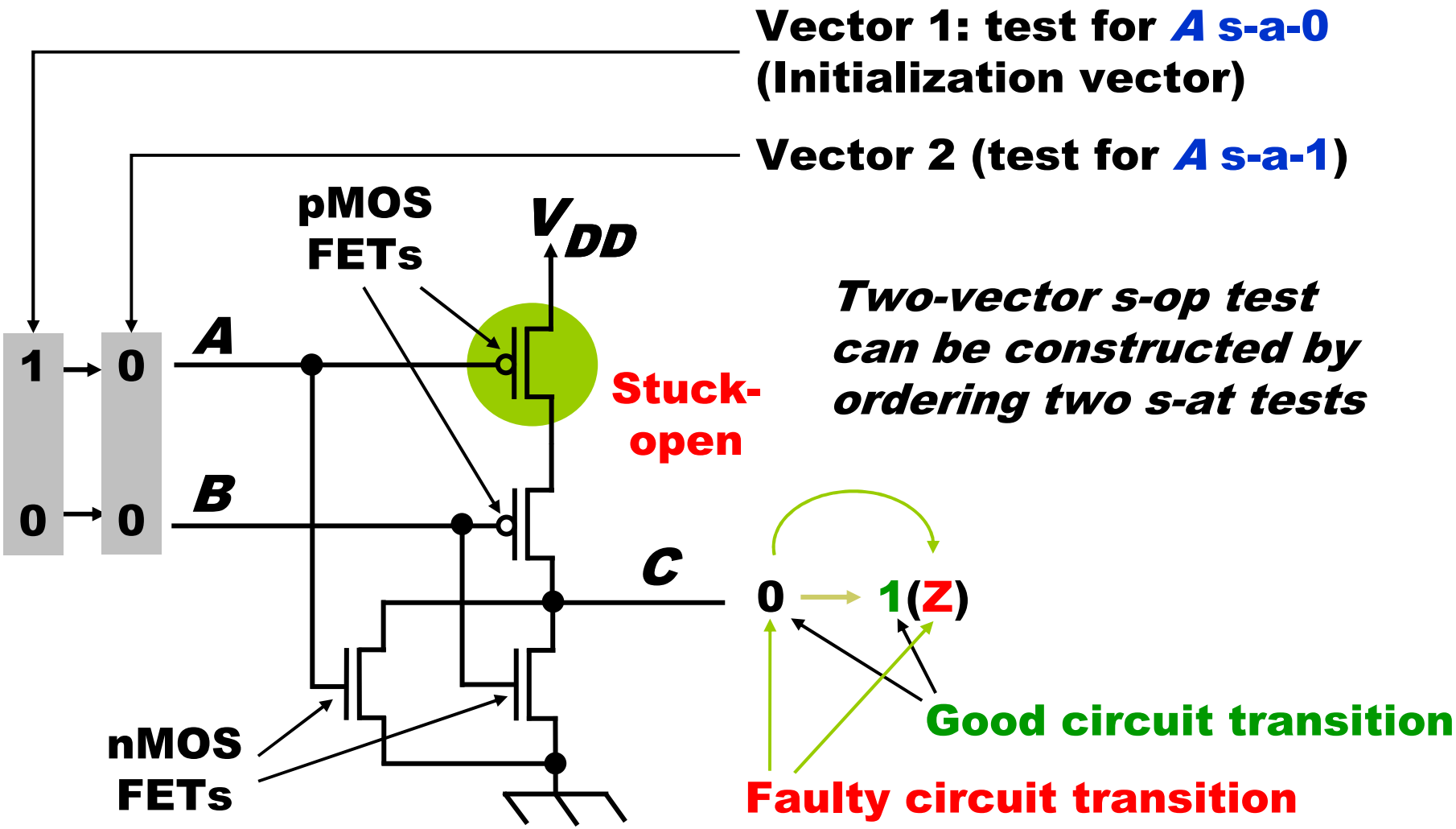
- A multiple stuck-at fault means that any set of lines is stuck-at some combination of (0,1) values.
- Not consider in practice
- The total number of single and multiple stuck-at faults in a circuit with k single fault sites is 3^k-1.
- A single fault test can fail to detect the target fault if another fault is also present, however, such **masking** of one fault by another is rare.
- Statistically, single fault tests cover a very large number of multiple faults (~**99.6**%).

Transistor (Switch) Faults

- MOS transistor is considered an ideal switch and two types of faults are modeled:
  - **Stuck-open** -- a single transistor is permanently stuck in the open state.
  - **Stuck-short** -- a single transistor is permanently shorted irrespective of its gate voltage.
- Detection of a stuck-open fault requires **two vectors.**
- Detection of a stuck-short fault requires the measurement of **quiescent current** ($\mathbf{I_{DDQ}}$).

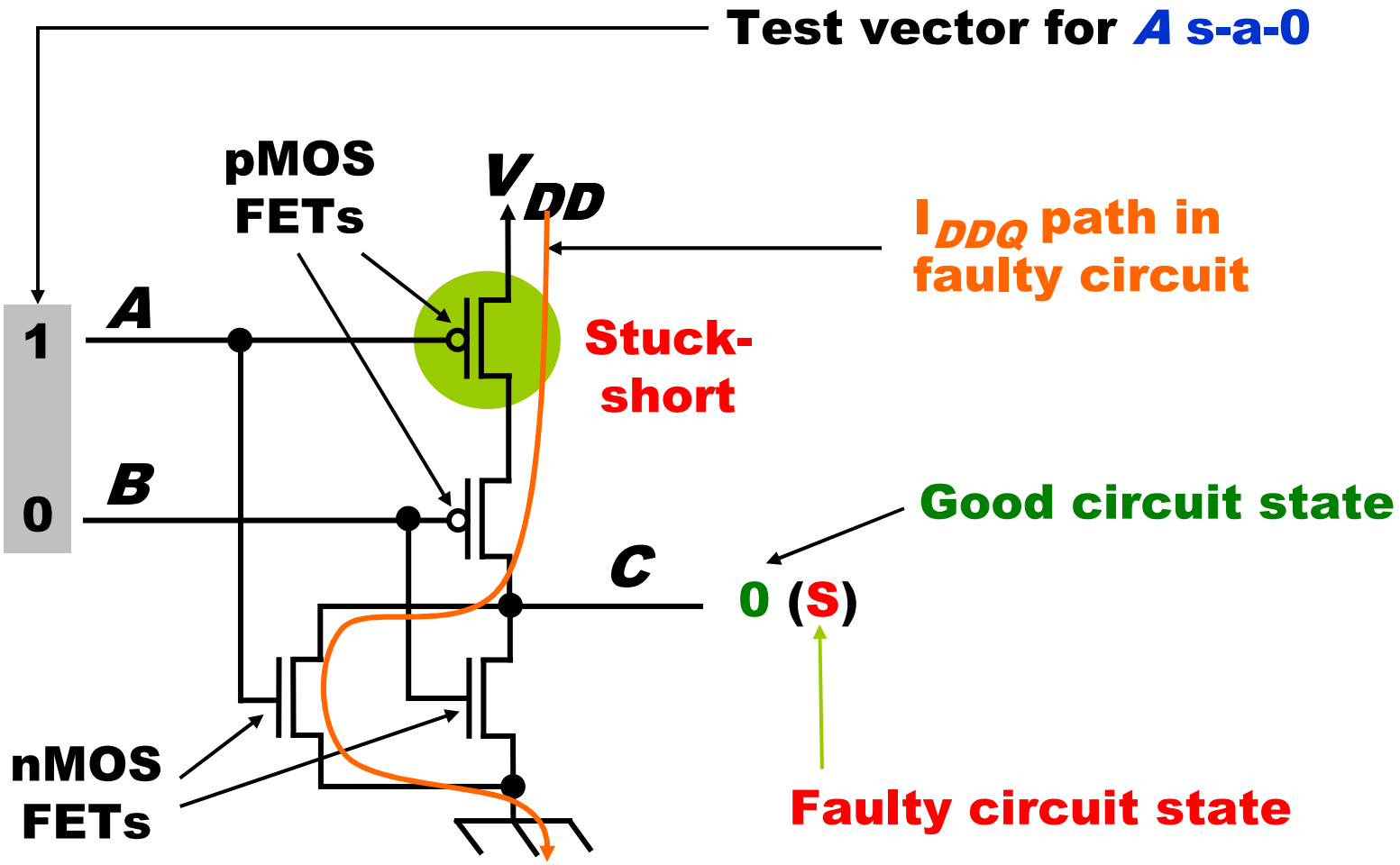
Transistor Faults …..Stuck-Open

- Example (NOR gate)



Transistor Faults …..Stuck-Short

- Example (NOR gate)



Summary

- Fault models are analyzable approximations of defects and are essential for a test methodology.
- For digital logic single stuck-at fault model offers best advantage of tools and experience.
- Many other faults (bridging, stuck-open and multiple stuck-at) are largely covered by stuck-at fault tests.
- Stuck-short and delay faults and technology-dependent faults require special tests.
- Memory and analog circuits need other specialized fault models and tests.

- Next lecture –
  we will talk about …

  Fault Simulation