VLSI Test Technology and Reliability (ET4076)

Lecture 8 (1)

Delay Test

(Chapter 12)

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2009-2010

Learning aims

- Define a path delay fault & delay test problem
- Distinguish between robust and non-robsut test
- Generate a test for a path delay fault
- Describe the different delay test methods

Contents

- Delay Test Problem
- Path delay test
  - Robust test versus non-robust test
  - Test generation
- Other fault models
- Delay test methodologies
  - Combinational, enhanced-scan and normal-scan
- Some practical aspects
  - At-speed test, Timing analysis & delay test
- Summary

Delay test problem ……..Terminology

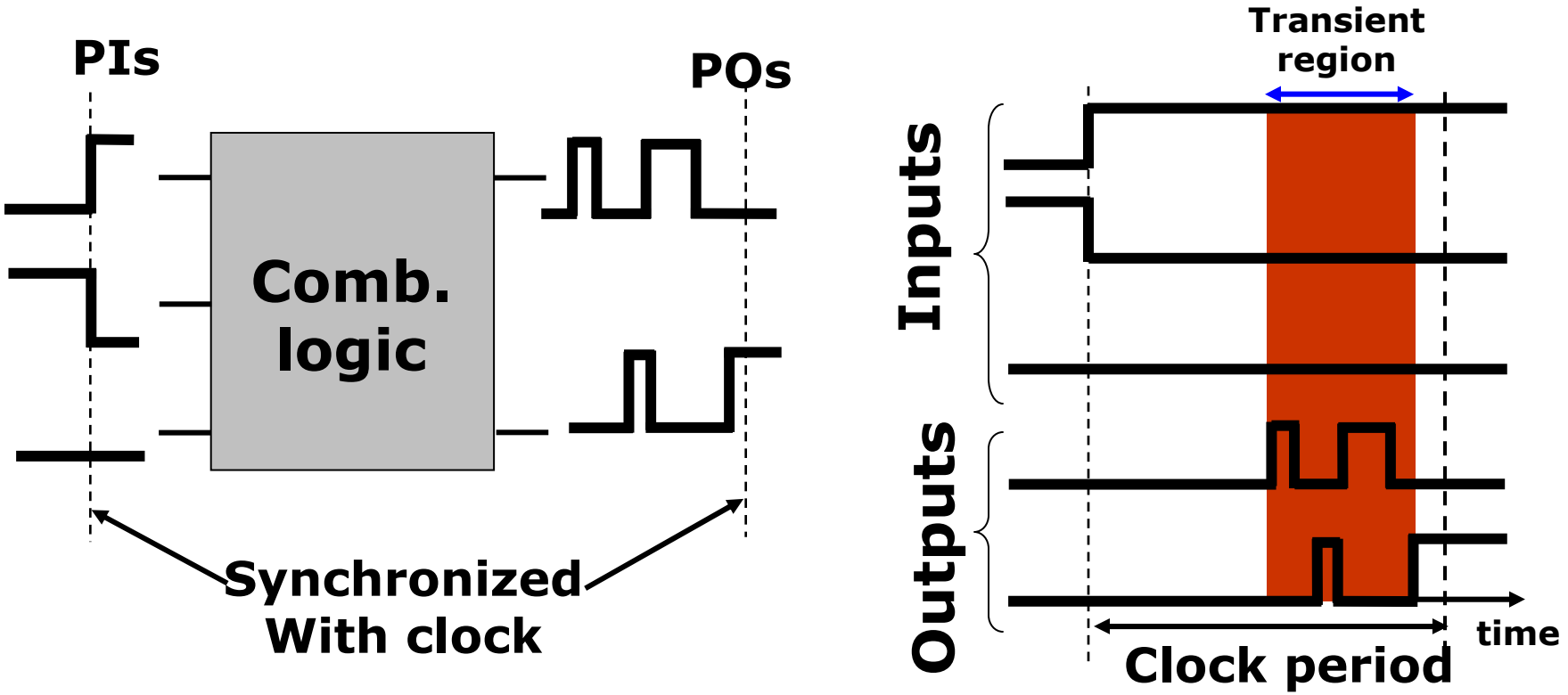
- **Delay Fault**:
  - A circuit has a delay fault if the delay of one of more paths (not necessary the critical path) exceeds the clock period
- **Critical path**:
  - it is the longest delay combinational path of a circuit
- **A Delay Test**:
  - a vector-pairs (two-pattern) test that launches transitions at one or more circuit inputs. A fault is detected by sampling one or more circuit outputs after the nominal circuit propagation
- **Delay faults have to be considered to achieve adequate DPM levels**
  - Application of 100% FC SAF test at high speed cannot realize a high product quality
  - Special delay tests are required

Delay test problem ……..Terminology

- **Switching** or **inertial delay**
  - It is the interval between input change & output change of a gate
  - Depends on input capacitance, device (transistor) characteristics, output capacitance of gate, input rise or fall times, states of other inputs (second-order effects), etc.
  - Approximation: fixed rise and fall delays (or min-max delay range, or single fixed delay) for gate output.

- **Propagation delay**
  - It is the time a signal even (transition) takes to traverse a path.
  - Consists of device **switching delay** and **interconnect** transport delays
  - Depends on transmission line effects (distributed R, L, C parameters, length and loading) of routing paths.
  - Approximation: modeled as lumped delays for gate inputs.
  - See Section 5.3.5 for timing models.

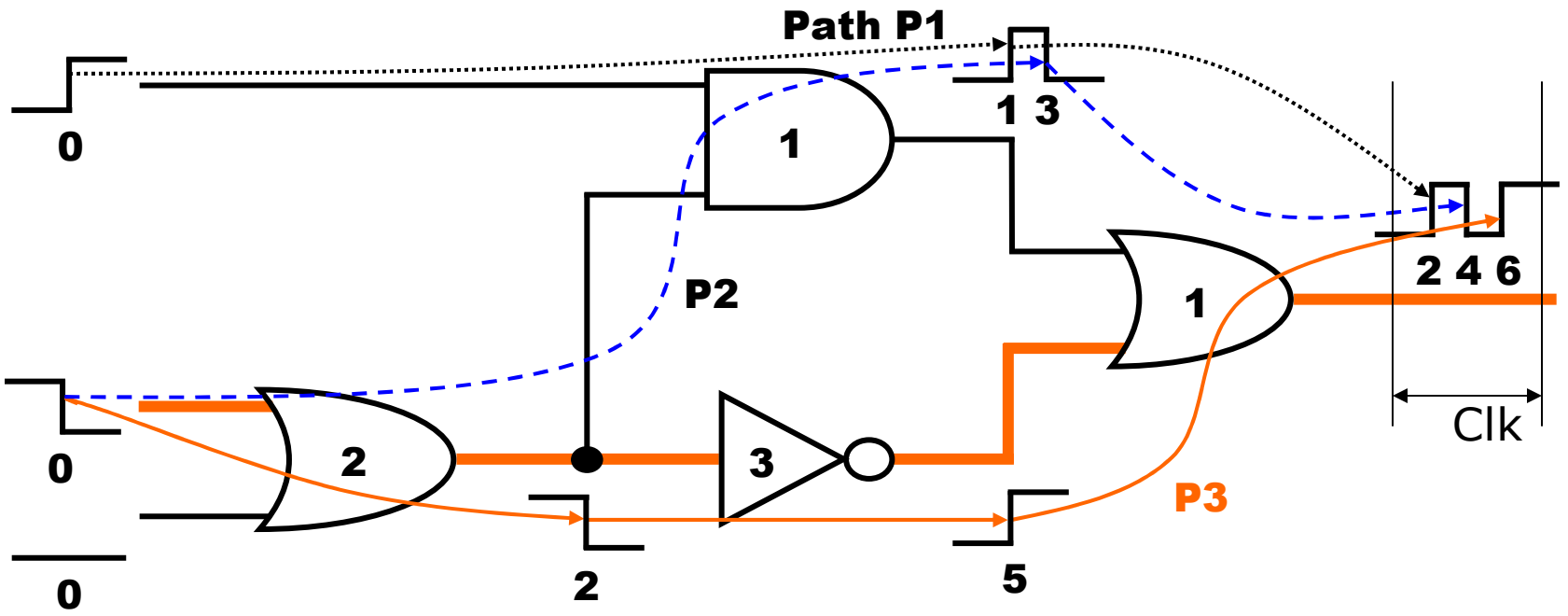
Delay test problem ….Digital Circuit Timing



- The right edge of PO transition region is determined by the delay of longest combinational path activated
- For a correct operation, delay should not exceed one clock period; otherwise **delay fault**
- Delay tests consists of **two** vectors

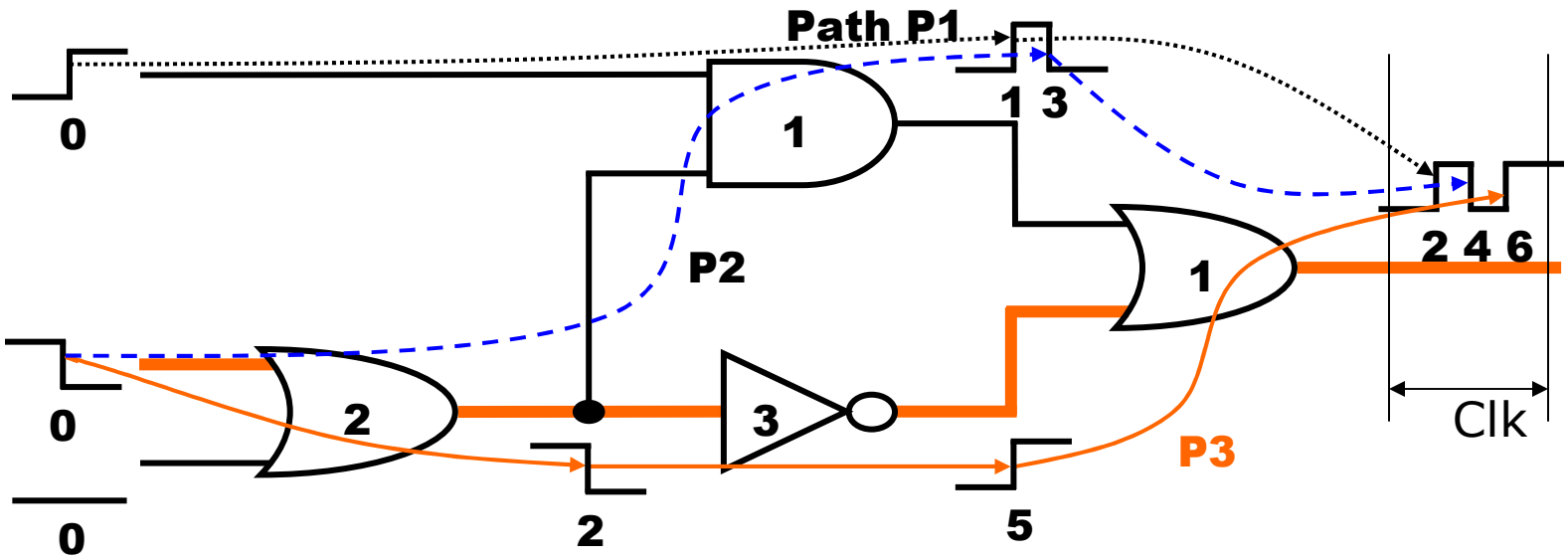
Delay test problem ……. Propagation Delay

- Gates modeled with lumped inertial delays that are integer multiples of a small time unit (1, 2, 3)
- Critical path is P3 with a delay of 6
- If T_{CLK}=7, every path will be faulty if delay exceeds 7



Delay test problem ……. Propagation Delay

- Test vector T_V= 010 -> 100
- **Single** faulty path
  - If delay of P3 <6, PO=1 irrespective of delays in P1 and P2.
  - Hence T_V will NOT detect delay <6 in P1 and P2.
- **Multiple** faulty path
  - More than one path is faulty at a time
  - Fault may (may not) be detected (depends on interferences)



Path delay test…… Definitions

- **A path delay fault (PDF):**
  - Its is a distributed series of defects along a specific circuit path. Individual delay is insufficient to cause a fail; however, the combined effect does cause a fail (**global fault model**)
  - An **important fault model** used in delay testing
- Each combinational path has two path-delay faults: rising and failing transitions
- Number of path delay faults in the circuit is twice the number of physical path in the circuits
- Only single-path delay is considered in practice (not multiple-path delay)

Path delay test ……. Non-robust test(1)

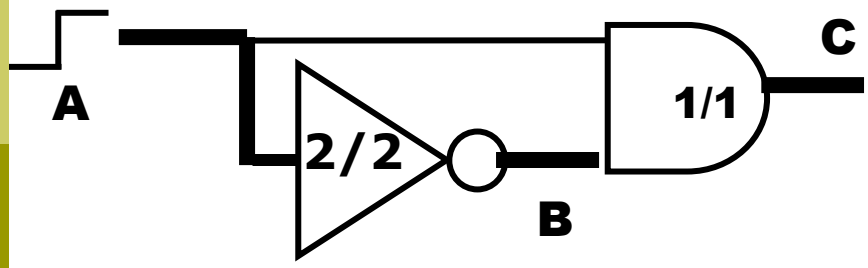
- **A non-robust test**:
  - A test that guarantees the detection of a path-delay fault when no other path-delay fault is present.

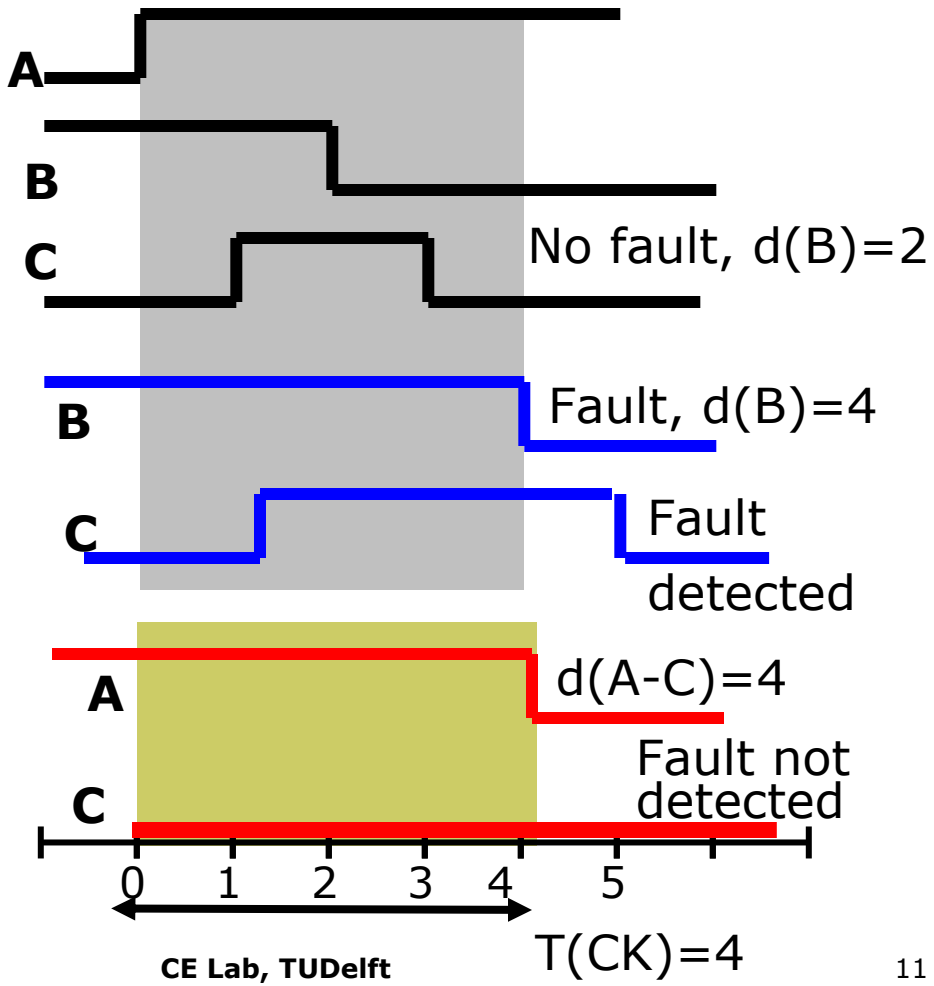
- **Singly-testable path-delay fault**:
  - A path-delay fault for which a non-robust test exists.

- Generation of non-robust test: vector pair V1, V2
  1. Initiates appropriate transition at the begin of the path
  2. **Static sensitization of path:** all paths input signals for a path under test assume **non-controlling** values in steady state (following the application of V1).
  3. Apply V2

Path delay test ……. Non-robust test(2)

- Generation of non-robust test: rising delay A-B-C
  - Initiation: A=0
  - **Static sensitization of path:** realized with A=1
  - Hence: vector: A= 0-> 1
- Fault detected only if A-C has no delay





Path delay test ……. Robust Test(1)

- **A robust test:**
  - A test that guarantees the detection of a path-delay fault of the targeted path, **irrespective** of delay faults on other paths.
  - It is a combinational vector-pair, V1, V2, that satisfies the following conditions:
    - Produce ***real events*** (different steady-state values for V1 and V2) on all **on-path** signals.
    - All on-path signals must have ***controlling events*** arriving via the targeted path.
- A robust test is also a non-robust test.
- Concept of robust test is general – robust tests for other fault models can be defined

Path delay test ……..5 value algebra

- **Generate tests for two consecutive time-frames simultaneously**
  - More efficient => Need higher order Boolean algebra
- **A Five-Valued Algebra**
  - Signal States: S0, U0 (**F0**), S1, U1 (**R1**), XX.
    - E.g., S0= steady 0, F0=falling 0, R1=raising 1, etc
  - On-path signals: F0 and R1.
  - Off-path signals: F0=U0 and R1=U1.

	S0	U0	S1	U1	XX
NOT	S1	U1	S0	U0	XX

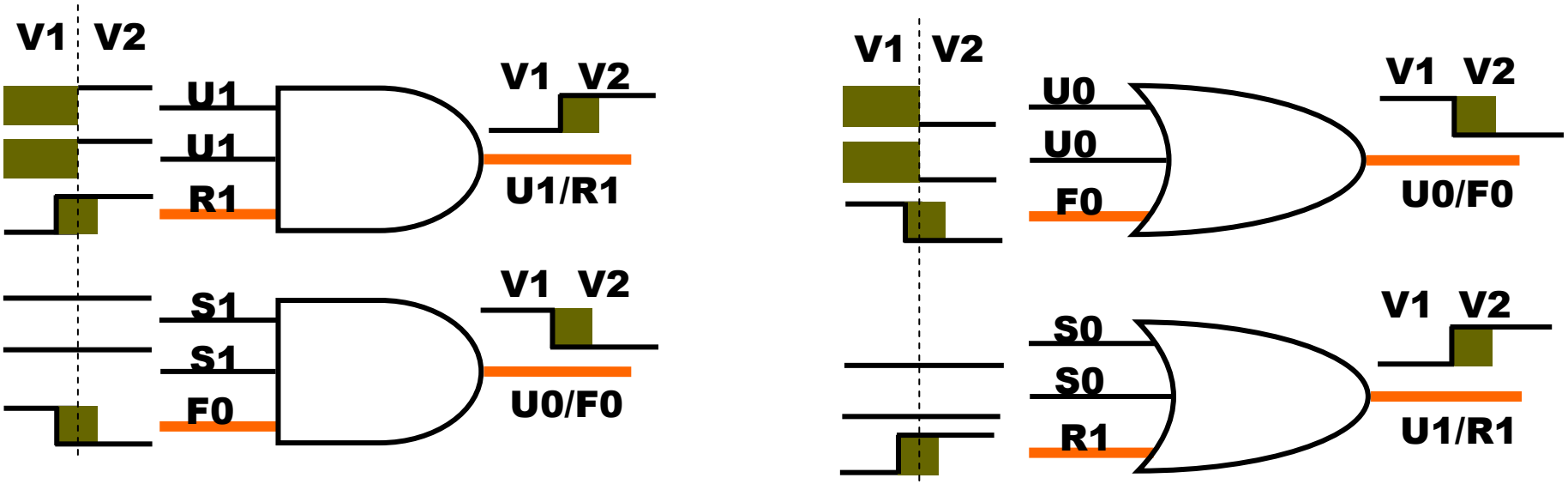
AND	S0	U0	S1	U1	XX
S0	S0	S0	S0	S0	S0
U0	S0	U0	U0	U0	U0
S1	S0	U0	S1	U1	XX
U1	S0	U0	U1	U1	XX
XX	S0	U0	XX	XX	XX

OR	S0	U0	S1	U1	XX
S0	S0	U0	S1	U1	XX
U0	U0	U0	S1	U1	XX
S1	S1	S1	S1	S1	S1
U1	U1	U1	S1	U1	U1
XX	XX	XX	S1	U1	XX

Ref.:
Lin-Reddy
IEEETCAD-87

Path delay test ……. Robust Test(2)

- Robust Test Conditions
  1. If a transition is **from controlling value to a non-controlling value**, then all **off-path inputs** must be only at the **non-controlling** value for the **second clock period** of path-delay fault (V2)
  2. If a transition is **from non-controlling value to a controlling value**, then all **off-path inputs** must be set at the steady **non-controlling** value for **both** clock periods of path-delay fault (V1 and V2)



Path delay test……PDFs

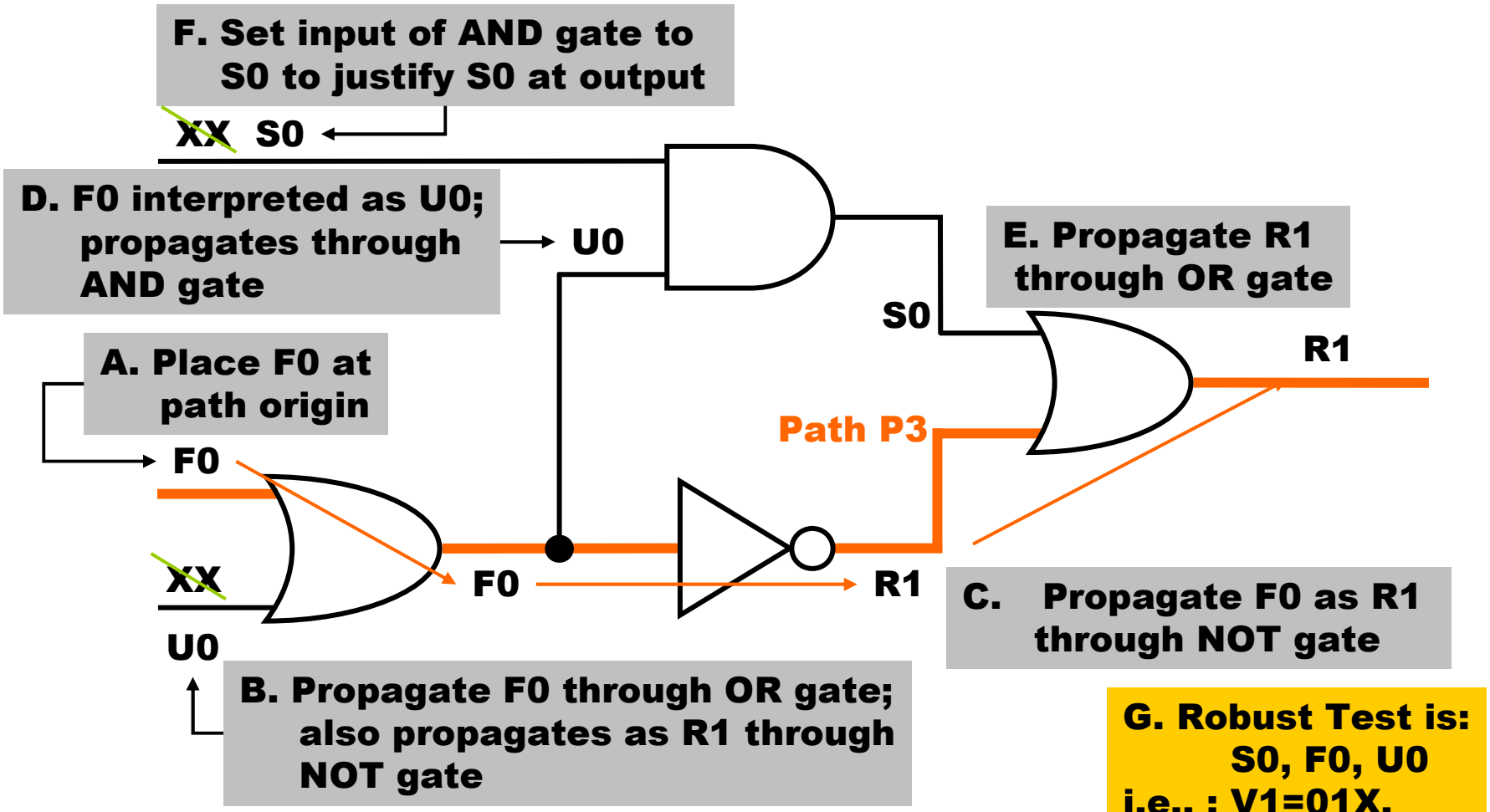
- Two Path Delay Faults PDFs (for each physical path)
  - Rising transition
  - Falling transition.
- Total number of paths is an **exponential** function of gates.
  - **Critical paths**, identified by static timing analysis (e.g., *Primetime* from Synopsys), must be tested.
- PDF tests are delay-independent.
  - Robust tests are preferred, but some paths have only non-robust tests.

Path delay test……PDFs

- Three types of PDFs (*JETTA* (11), 1997):
  - *Singly-testable* PDF – has a non-robust or robust test.
  - *Multiply-testable* PDFs – a **set** of singly untestable faults that has a non-robust or robust test. Also known as functionally testable PDFs.
  - *Untestable* PDF – a PDF that is neither singly nor multiply testable.

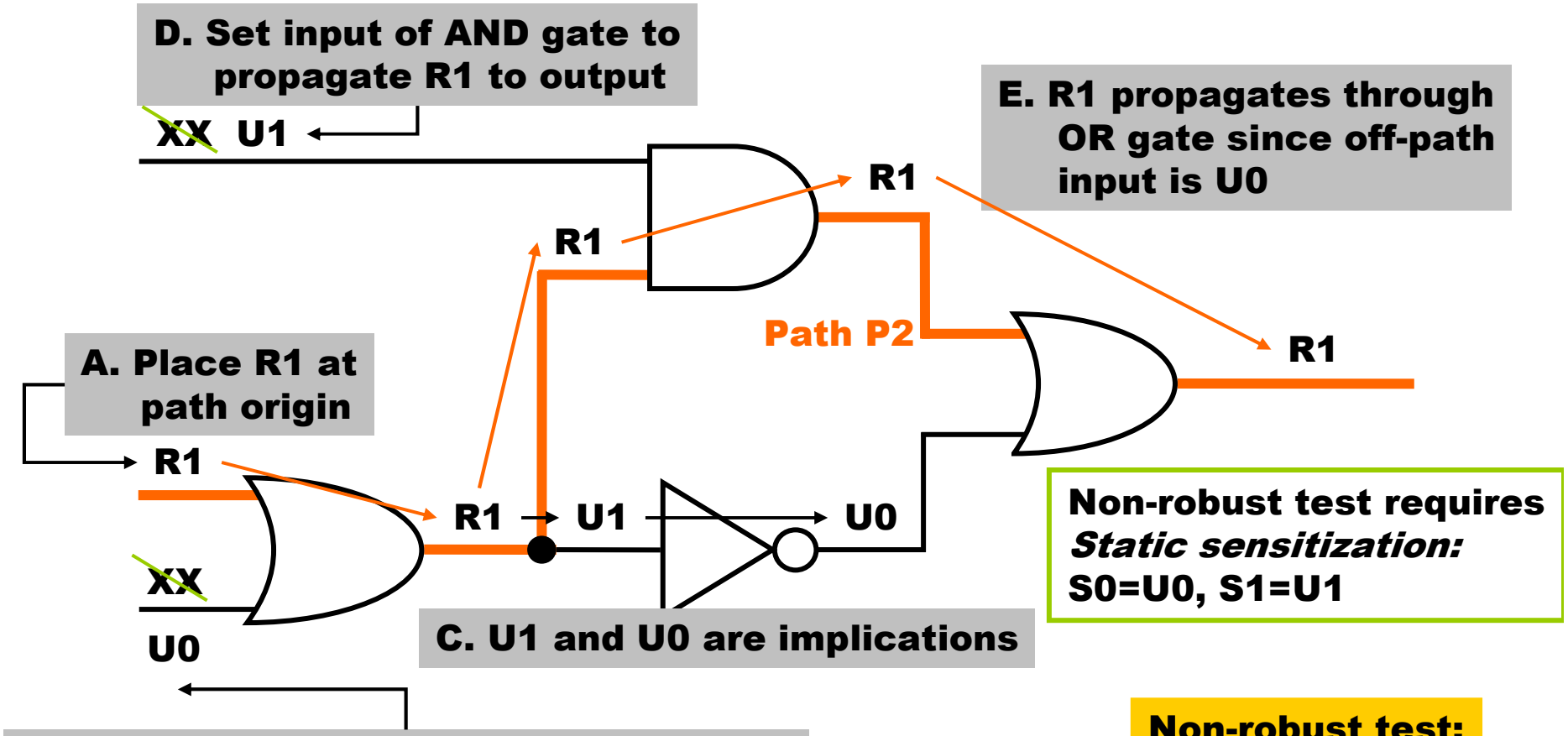
Path delay test…..Robust Test Generation

Test for falling transition through path P3: Steps A through E



Path delay test … Non-Robust Test Generation

Test for rising transition through **path P2** has no robust test.



Other Delay Fault Models

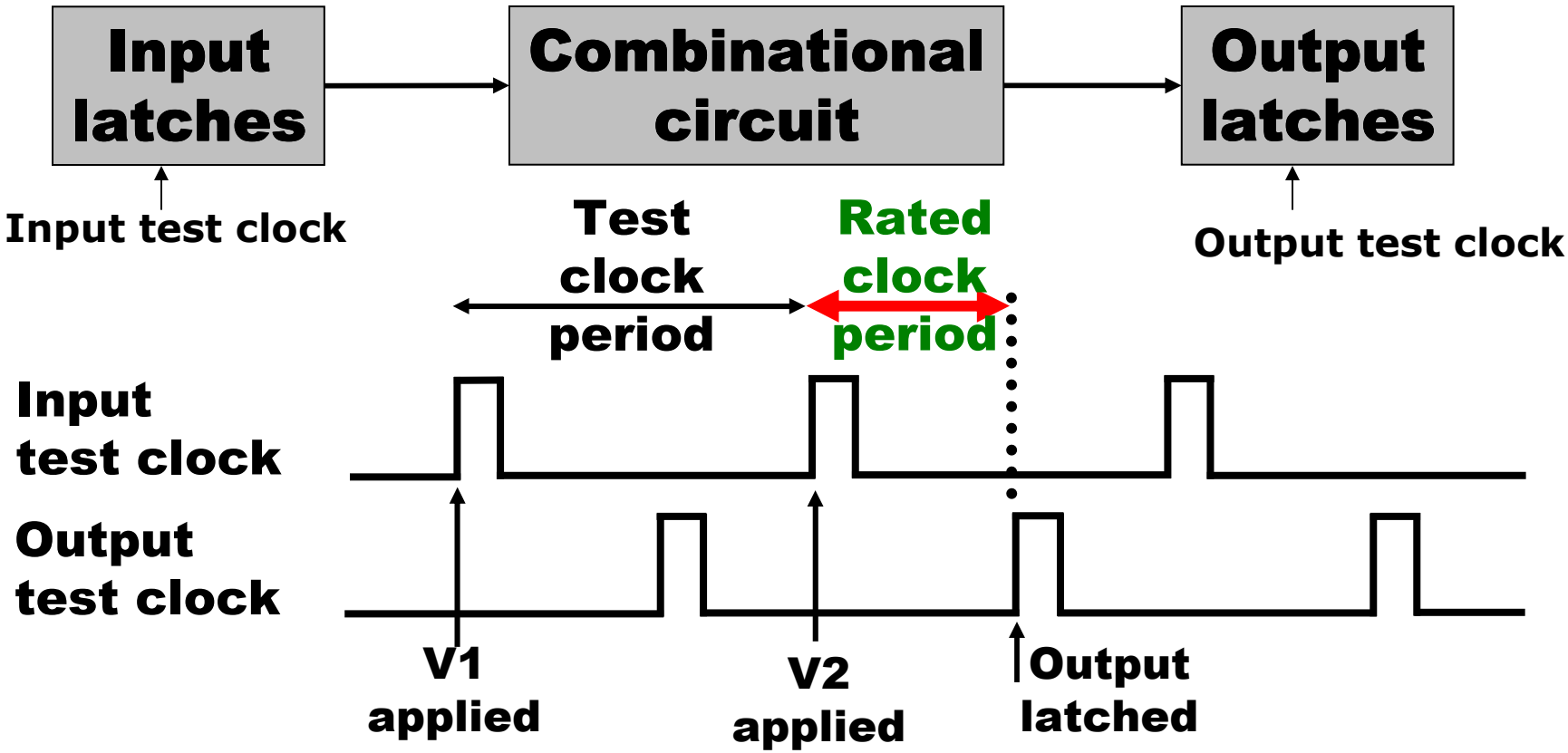
- ***Transition* fault:** -- A segment-delay fault with segment of unit length (single gate)
  - Makes the signal change slow (Models spot/gross delay defects)
- Two faults per gate: slow-to-rise &slow-to-fall
- Tests are similar to stuck-at fault tests.
- E.g., To test for slow-to-rise fault test for SA0
  1. Initialize the line to 0 (v1)
  2. Test for s-a-0 to detect slow-to-rise transition fault (v2)
  - Test vector (v1,v2) created
- Other models
  - Gate delay
  - Line delay
  - Segment-delay

Delay Test Methodologies

- Three methodologies
  - Slow-Clock Combinational Test
    - Useful when ATE cannot apply the vectors at speed test
    - Applies only with circuits with special architecture
  - Enhanced-Scan Test
    - Full flexibility of combinational circuits
    - Test time similar to full scan design
  - Normal-Scan Sequential Test
    - Fault coverage cannot guaranteed and depends on the circuit due to the correlation between the two vectors

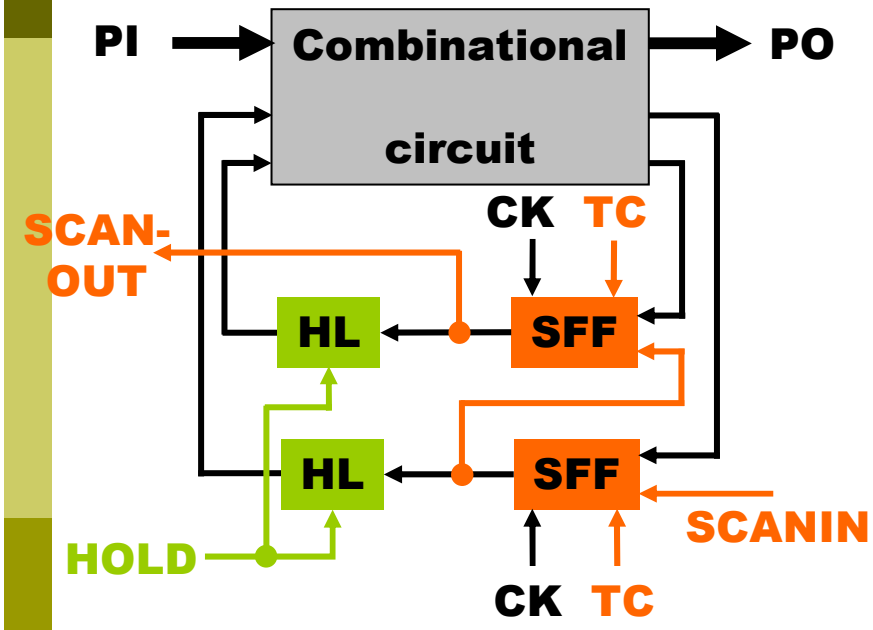
Delay Test Methodologies…. Slow-Clock Test

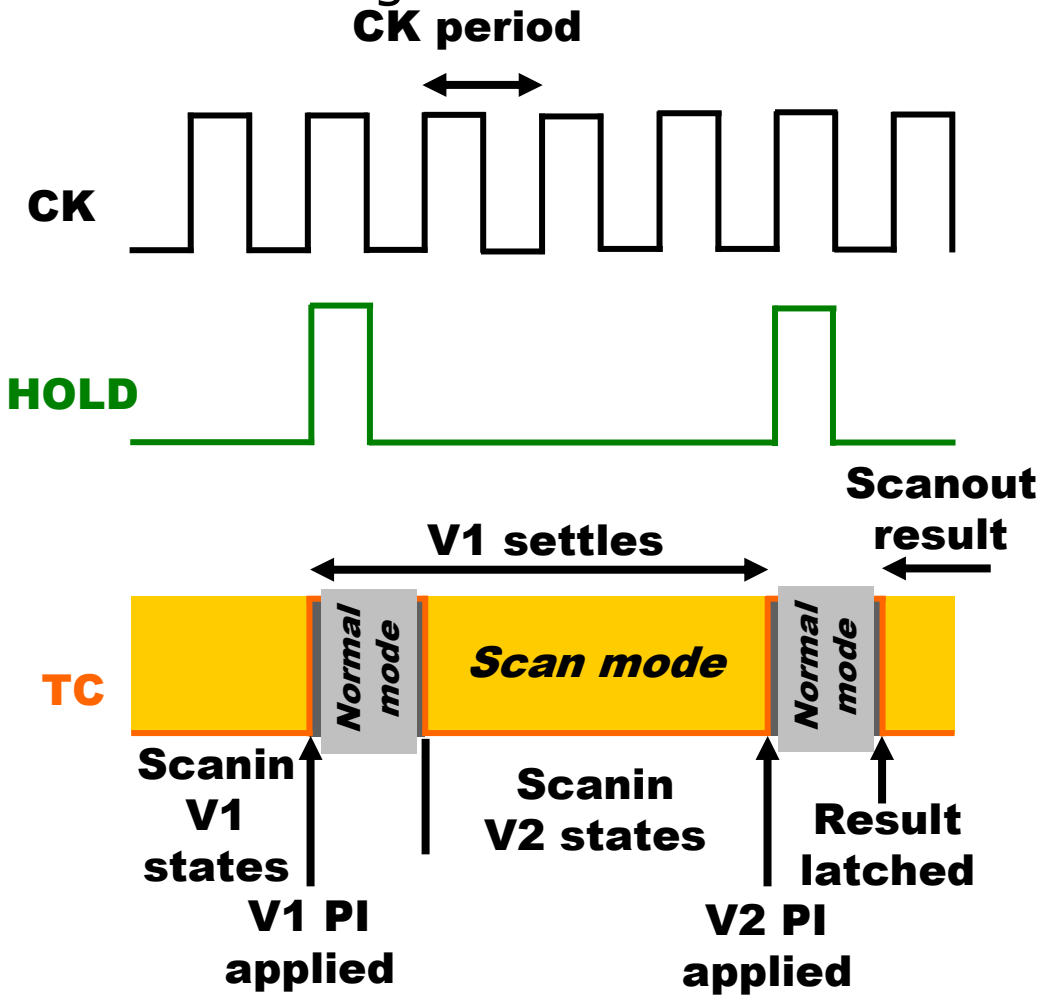
- Applicable to
  - Combinational circuits
  - Sequential circuits with FFs only at PIs and Pos
- Clocks should be independently controllable to allow phase delays and skews



Delay Test Methodologies … Enhanced-Scan

- Applicable to sequential circuits
- Any arbitrary vector-pair can be applied
- Tests can be generated by considering comb. circuit only
- Hold latches HL and additional Hold signal

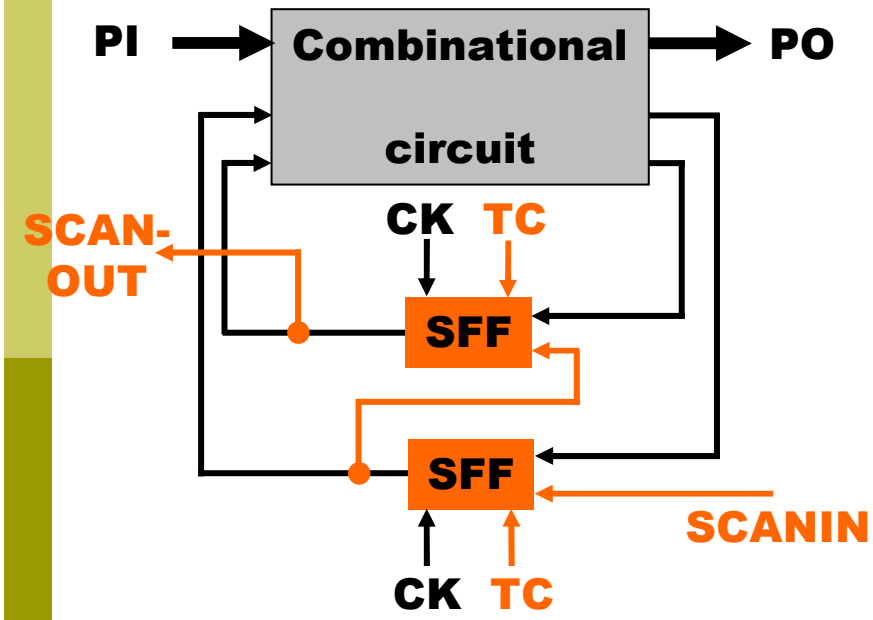




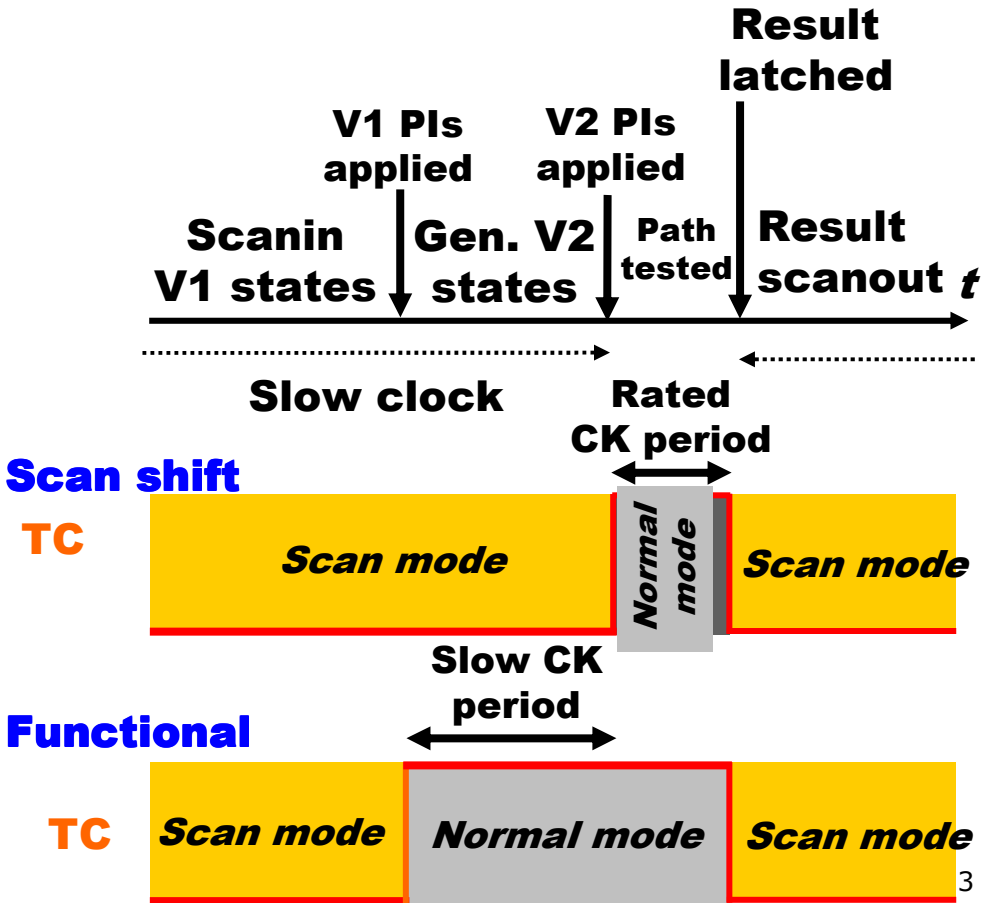
CK: system clock
TC: test control
HOLD: hold signal
SFF: scan flip-flop
HL: hold latch

Delay Test Methodologies … Normal-Scan

- Requires special generation of vector-pair
- Two options to generate V2 state
  - **Scan shift**: state portion of V1 is scanned in. The state portions V1 and V2 have to differ in one bit. So scanning in one bit will provide V2 potion state based on the state portion of V1.
  - **Functional**: state portion of V1 is scanned in.
    - V1 state and its application at PIs produces automatically V2 state



CK: system clock
TC: test control
SFF: scan flip-flop



Some practical issues

- **At speed testing**
  - i.e., application of test vectors at the **rated-clock speed**.

- Two methods:
  - **External test**:
    - Vectors may test one or more functional critical (longest delay) paths and a large percentage (~100%) of transition faults.
    - High-speed testers are expensive/unavailable.
  - ***Built-in self-test* (BIST):**
    - Hardware-generated random vectors applied to combinational or sequential logic.
    - Only clock is externally supplied.
    - Non-functional paths that are longer than the functional critical path can be activated and cause a good circuit to fail.
    - Some circuits have initialization problem.

Some practical issues

- **Timing analysis** examines combinational paths in the circuit topology
  - No signal values used-> Static time analysis (Like Primetime (Synopsys))
- Time analysis improve the design and test
  - **Timing simulation**:
    - Critical paths are identified
    - Timing or circuit-level simulation using designer-generated functional vectors verifies the design.
  - **Layout optimization**: Critical path data are used in placement and routing. Delay parameter extraction, timing simulation and layout are repeated for iterative improvement.
  - **Critical path tests**: Critical path delay determine the clock period.

Summary

- *Delay models*
  - *Path-delay fault* (PDF) models distributed delay defects. It verifies the timing performance of a manufactured circuit.
  - *Transition fault* models spot delay defects and is testable by modified stuck-at fault tests.
- Critical paths of non-scan sequential circuits can be effectively tested by rated-clock tests.
- Robust and non-robust delay test
- Path delay test
  - Requires at speed test
  - Mainly using BIST
  - Different methods (e.g., enhanced scan)