Chapter 3

DETECTION LIMIT DUE TO OFFSET

- ***What is the definition of offset?***
- ***How is offset represented?***
- ***How are the equivalent input sources of offset calculated?***
- ***How is offset in sensors dealt with?***
- ***How does offset in sensor read-out affect the detection limit?***

3.1 Introduction

As is shown in Section 1.5, it is not the achievable system gain, but rather the equivalent parasitic signal level at the input that determines the minimum measurable input signal and thus the detection limit. There are several types of parasitic signals (= sources of uncertainty/source of error) that should be considered. The four different types discussed here are, respectively:

1. Source loading,

2. A (quasi)-DC level,

3. A common-mode signal in a differential measurement and

4. A wideband AC signal.

Source loading in the electrical domain is discussed in section 2.4. A DC parasitic signal is a problem in a low-frequency measurement. A differential measurement set-up should be sensitive only to the differential signal. A parasitic wideband signal is usually referred to as noise and is the most general source of uncertainty. The parasitic signal often acts on the instrument at several nodes.

Due to additive errors acting on the system, finding the detection limit in a particular application involves four steps:

1. Identification of the dominant source of error.
2. Estimation of the magnitudes of the various sources of error, which are distributed throughout the system and contribute to that particular type of error.
3. Calculation of the equivalent input error sources representing the combined effect of those distributed sources of error on the output.
4. Calculation of the minimum measurable signal from (3), while also considering the inaccuracy or SNR specifications.

In a typical design of a read-out circuit or measurement set-up this procedure is carried out several times. The system is adapted (re-designed) in order to achieve the lowest possible detection limit.

In electrical measurements the sources of equivalent input error are voltage and current sources. The equivalent input error sources should be specified in terms of the non-electrical source of error in the case of an instrument used for a non-electrical quantity, to enable the direct comparison between the desired and error signals in the fourth step. In e.g. an accelerometer this error is an equivalent acceleration.

In this chapter **offset** is discussed as the main detection-limiting mechanism in the case of a DC-operated system. Offset is a deterministic sources of error and, therefore, the approach for finding the equivalent input error sources as a function of the distributed sources using the rules for error propagation is discussed first.

3.2 Calculation of equivalent input sources of error

3.2.1 General input sources of error

Figure 3.1 shows the approach used to calculate the equivalent input-referred error voltage as a function of distributed deterministic additive errors. Error signals are generated at many nodes throughout the system as shown schematically in Fig. 3.1a. The approach is explained for the read-out of an input voltage source without source impedance using a voltage amplifier with gain G, but is generally applicable. The output voltage, U_o, is non-zero, despite the fact that $U_i = 0$, which is due to the additional error signals, $U_{\varepsilon,i}$ that are generated.

The convention that is generally used for indicating a non-ideal component or system is to apply a hatched patch or a grey-scale to the inner area of the circuit symbol. As shown in Fig. 3.1, the grey-scale approach is used here. The component or system is made free of noise by removing the grey-scale and imposing

this to the signal source that represents the non-ideality. In this chapter this approach is used to analyse offset and in chapter 5 to analyse noise.

The transfer functions from the different nodes in the system to the input are considered linear. As a consequence the equivalent deterministic sources of deterministic additive error at the input, $U_{\varepsilon,eq}$, is the linear superposition of the effects of all the distributed sources, back-tracked to the input by calculation, as shown in Fig. 3.1b:

$$U_o = G\left(U_i + U_{\varepsilon,eq}\right) \quad \text{with} \quad U_{\varepsilon,eq} = \frac{1}{G}\sum_{i=1}^{n} G_i U_{\varepsilon,i}, \tag{3-1}$$

where G_i denotes the gain for deterministic error signal, $U_{\varepsilon,i}$, to the output, U_o; $U_{\varepsilon,eq}$ is the equivalent error input signal; and $G = U_o/U_i$ is the overall system gain.

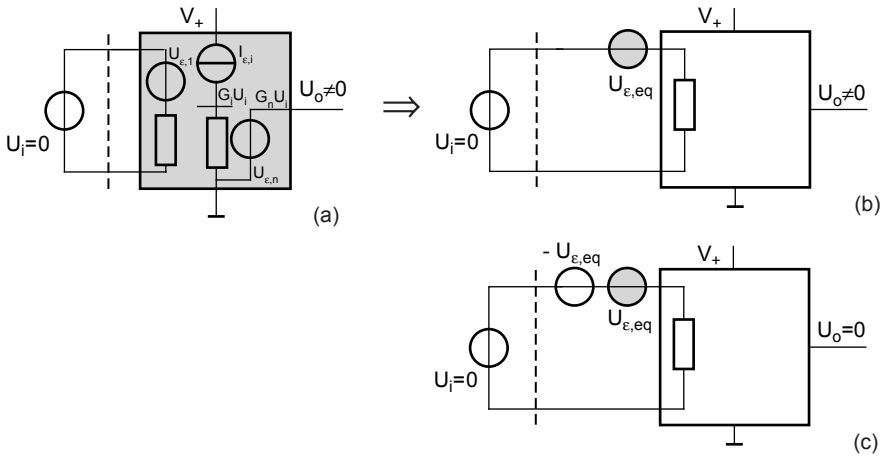

Figure 3.1, System with (a) distributed sources of error, (b) error represented by equivalent input error voltage and (c) compensating for error.

So far the approach applies to any type of error signal. In the case of a deterministic error, such as offset and finite common-mode rejection, for which the value of the signal is predictable at any moment in time, provided that the signal is fully specified, the error can be compensated for by adding the inverse of the equivalent input error to the input circuit, as shown in Fig. 3.1c.

The compensation scheme shown in Fig. 3.1c can be used for actually measuring the deterministic error. Inserting a voltage source and tuning the amplitude until U_o=0 yields $U_{\varepsilon,eq}$.

For stochastic error signals, such as noise and interference, only the statistical parameters can be included in the specification. This makes the prediction of any momentary amplitude impossible and, therefore, such a compensation is not possible.

It should be emphasised that Fig. 3.1. shows a highly simplified system. Firstly, it is assumed that the voltage source connected to the input is ideal (no source impedance). Secondly, the system transfer function is considered fully characterised by one factor: the linear voltage gain, *G*. Both assumptions are basically incorrect. A practical signal source exhibits a source impedance. Moreover, the relevant signals at the input and output of an electronic system are voltage and current, and the transfer function is described by a 2×2 matrix. Similar considerations apply when reading-out a current source with a current amplifier.

Nevertheless, in the case of a properly designed voltage read-out, the source impedance is much smaller than the input impedance of the voltage amplifier (see Section 2.4.1) and the specification of the transfer function in terms of a simple gain factor is adequate. Moreover, an equivalent input-referred error signal can be described by only one source that is of the same type as the input signal source (i.e. any equivalent input error current source in Fig. 3.1. would be short-circuited by the input voltage source). However, in general:

The equivalent input error of an electronic system should in general be specified using two sources: an equivalent input voltage source plus an equivalent input current source.

3.2.2 Calculation of the equivalent input sources of offset

The source of error discussed in this chapter is offset.

Offset is characterised by a non-zero steady-state (DC) output of a system at a zero steady-state (DC) input level.

In the case of offset in the voltage amplifier shown in Fig. 3.2a, the output voltage is non-zero for a zero input level (short-circuited input).

The equivalent input sources of offset are: the *offset voltage,* $U_{os,eq}$, plus the *bias current*, $I_{bias,eq}$.

These sources are fictitious, yet do include the effect of all distributed sources of offset within the system. The main practical cause for the offset voltage is the asymmetry of the electronic components in the differential input stage of the sys-

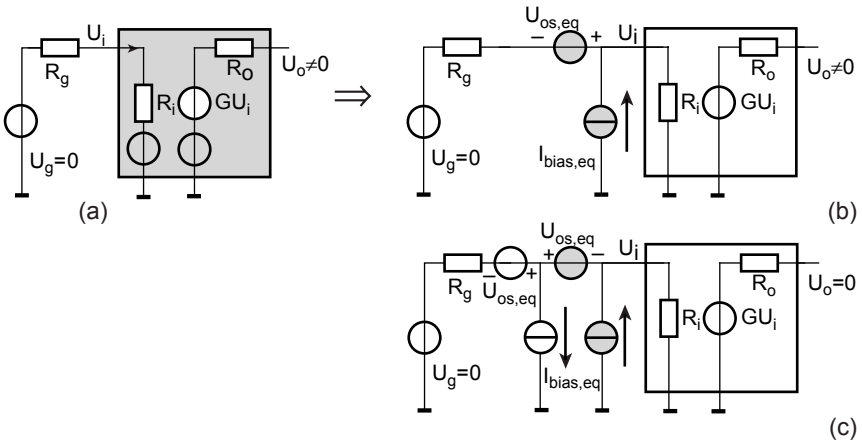

Figure 3.2, System with offset: (a) distributed sources of offset, (b) equivalent input sources of offset with an offset-free system and (c) nulling of U_o.

tem (such as an opamp). The bias current originates from the fact that active electronic components need to be biased for proper operation. Passive components do generally not show offset. Figure 3.2b is equivalent to Fig. 3.2a with the distributed sources of offset represented by the input-referred sources of offset, and the system is considered free of offset.

Figure 3.2c is similar to Fig. 3.1c and refers to the approach used to measure offset. The voltage source within the input circuit (the equivalent input offset of opposite polarity) is required to **trim the output to zero at short-circuited input**. A bias current source in parallel to each of the input terminals is required to supply the current that flows into that input terminal.

Calculating the two equivalent input sources of offset requires two independent expressions. Moreover, the equivalence should necessarily apply to all possible input circuits. This condition can be used to derive two expressions using two extreme conditions, viz.:

- Short-circuited input and
- Open- circuited input.

A short-circuited input closes the loop that includes the input circuit with the input resistance and offset voltage source, while short-circuiting the bias current parallel to the input nodes. This short-circuit prevents the bias current from generating a voltage across the input terminals. Consequently, the bias current is eliminated as a variable, which results in an expression in terms of the offset voltage only.

Alternatively, leaving the input circuit open prevents the offset voltage at the input from generating a current into the input circuit, thus eliminating this offset voltage as a variable and resulting in an expression in terms of equivalent input bias current only.

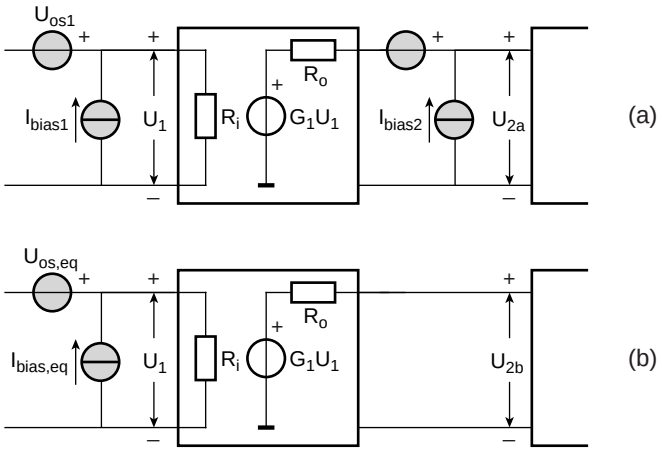

Figure 3.3, Model used for the calculation of the equivalent input offset sources in a cascaded system.

This approach can be applied to calculate the equivalent input offset source in a voltage amplifier that is composed of a cascaded system with two gain stages, each with a well-specified equivalent input offset voltage and bias current, as is shown in Fig. 3.3. The first stage has a gain G_1, an equivalent input offset voltage U_{os1} and a bias current I_{bias1}. The second stage has a gain G_2, an equivalent input offset voltage U_{os2} and a bias current I_{bias2}.

Given the distributed system shown in Fig. 3.3a, the equivalent system in Fig. 3.3b should, by definition, give the same output voltage in all possible operating conditions. The two operating condition extremes mentioned are used to derive expressions for the equivalent sources in terms of the distributed sources. Open input yields:

$$\begin{aligned} U_{2a} &= I_{bias1}R_iG_1 + I_{bias2}R_o + U_{os2} \\ U_{2b} &= I_{bias,eq}R_iG_1, \end{aligned} \tag{3-2}$$

and $U_{2a} = U_{2b}$ results in:

$$I_{bias,eq} = I_{bias1} + \frac{U_{os2} + I_{bias2}R_o}{G_1R_i}. \tag{3-3}$$

Short-circuiting of the input terminals yields:

$$\begin{aligned} U_{2a} &= U_{os1}G_1 + I_{bias2}R_o + U_{os2} \\ U_{2b} &= U_{os,eq}G_1, \end{aligned} \tag{3-4}$$

and U_{2a}= U_{2b} results in:

$$U_{os,eq} = U_{os1} + \frac{U_{os2}}{G_1} + \frac{I_{bias2}R_o}{G_1} \tag{3-5}$$

The above example indicates that a large gain, G_1, in the first stage is beneficial, since it reduces the effect of the second stage. This observation is of general validity for both deterministic and random errors. **The design effort in a low-offset amplifier should be directed to the first stage, which should be low-offset and high-gain**. If these two requirements are met, the cascaded sections have little effect on offset performance.

Example 3.1
A voltage amplifier is constructed using a trans-conductance, g_{m1}, and a current-to-voltage converter (trans-resistance), R_{m2}, as shown in Fig. 3.4. Both sub-circuits exhibit offset.

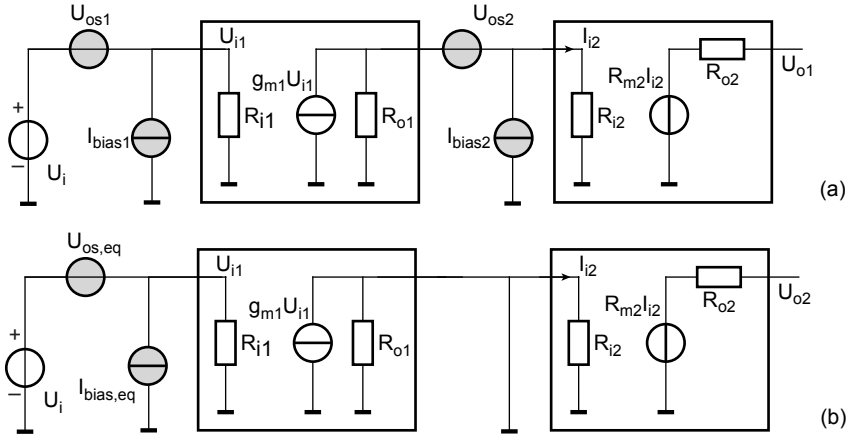

Figure 3.4, Voltage amplifier using a trans-conductance circuit in series with a trans-resistance circuit both (a) with equivalent input sources of offset specified and (b) with equivalent sources of offset at the input.

The equivalent input offset sources are specified as: U_{os1}= 1mV, U_{os2}= 10 mV, I_{bias1}= 1 nA and I_{bias2}= 100 nA.

In a first attempt to calculate the equivalent input offset sources of the cascaded sub-circuits, the following assumptions are made: $R_{i1}= R_{o1} \rightarrow \infty$ and $R_{i2}= R_{o2} = 100\ \Omega$, $g_{m1}= 100$ mA/V and $R_{m2}= 1000$ V/A. Calculate the equivalent input offset sources, $U_{os,eq}$ and $I_{bias,eq}$.

Solution:
The overall transfer function is a voltage gain of $G_v= 100$ mA/V×1000 V/A= 10. Open input yields:

$$\begin{aligned} U_{o1} &= I_{bias1}R_{i1}\times g_{m1}\times\frac{R_{o1}}{R_{o1}+R_{i2}}\times R_{m2}+I_{bias2}\times\frac{R_{o1}}{R_{o1}+R_{i2}}\times R_{m2}+\frac{U_{os2}}{R_{o1}+R_{i2}}\times R_{m2} \\ U_{o2} &= I_{bias,eq}R_{i1}\times g_{m1}\times\frac{R_{o1}}{R_{o1}+R_{i2}}\times R_{m2}, \end{aligned} \tag{3-6}$$

and $U_{o1}= U_{o2}$ results in:

$$I_{bias,eq} = I_{bias1}+\frac{U_{os2}+I_{bias2}R_{o1}}{g_{m1}R_{i1}R_{o1}}. \tag{3-7}$$

Short-circuiting of the input terminals yields:

$$\begin{aligned} U_{o1} &= U_{os1}\times g_{m1}\times\frac{R_{o1}}{R_{o1}+R_{i2}}\times R_{m2}+I_{bias2}\times\frac{R_{o1}}{R_{o1}+R_{i2}}\times R_{m2}+\frac{U_{os2}}{R_{o1}+R_{i2}}\times R_{m2} \\ U_{o2} &= U_{os,eq}\times g_{m1}\times\frac{R_{o1}}{R_{o1}+R_{i2}}\times R_{m2}, \end{aligned} \tag{3-8}$$

and $U_{o1}= U_{o2}$ results in:

$$U_{os,eq} = U_{os1}+\frac{U_{os2}+I_{bias2}R_{o1}}{g_{m1}R_{o1}}. \tag{3-9}$$

In the case of $R_{i1}= R_{o1}\rightarrow\infty$:
$U_{os,eq}= U_{os1}+ I_{bias2}/g_{m1}= 1.001$ mV and $I_{bias,eq}= I_{bias1}= 1$ nA.

In a more practical assessment of the circuit, the equivalent input offset sources and impedances of the trans-impedance amplifier remain unchanged ($U_{os1}= 1$mV, $U_{os2}= 10$ mV, $I_{bias1}= 1$ nA, $I_{bias2}= 100$ nA, $R_{i2}= R_{o2}= 100\ \Omega$, $g_{m1}= 10$ mA/V and $R_{m2}= 10\ \Omega$); however, $R_{i1}= 100$ kΩ and $R_{o1}= 10$ kΩ.

Calculate the equivalent input offset sources, $U_{os,eq}$ and $I_{bias,eq}$.

Solution:
Applying R_{i1}= 100 kΩ and R_{o1}= 10 kΩ to equations 3.7 and 3.9 yields:
$U_{os,eq}$= 1.01 mV and $I_{bias,eq}$= 1.11 nA.

The calculation can be significantly simplified for the read-out of an ideal voltage source, since any equivalent input bias current would be short-circuited. Only the equivalent input voltage source needs to be calculated. Similarly, the read-out of an ideal current source is equivalent to the open input circuit, and any equivalent input offset voltage is insignificant.

Offset is an issue in both the sensor and the read-out circuit. Offset in read-out circuits is discussed in Section 3.3, while the effect of offset on sensor performance is discussed in Section 3.4.

3.3 Offset in read-out circuits

3.3.1 Offset in read-out circuits with a differential input

Analog circuits for sensor read-out are usually equipped with a differential input (with U_+ as the non-inverting input, U_- as the inverting input and U_o= $G(U_+$-U_-)), which enables the measurement of differential signals (see Chapter 4). This feature requires modifying of the representation of offset in terms of equivalent input sources of offset, as discussed in the previous section, and results in Fig. 3.5a.

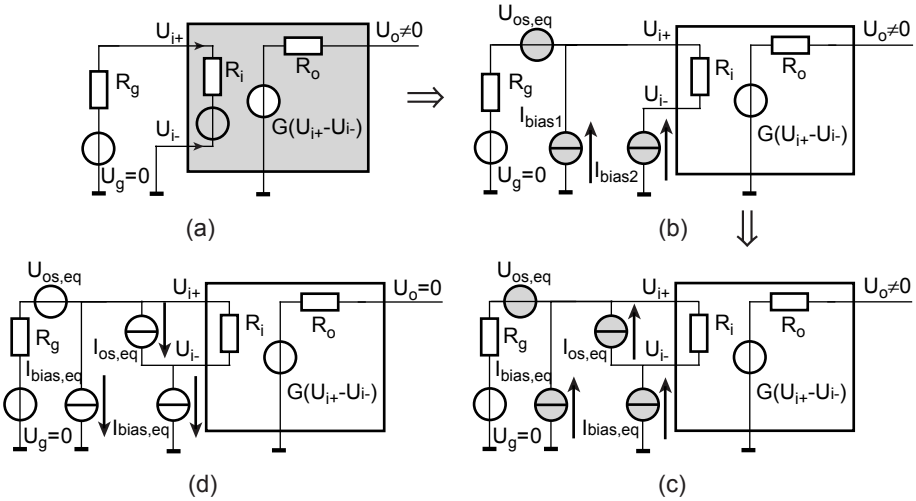

Figure 3.5, Input referred offset in a system with a differential input: (a) non-ideal system with distributed sources of offset, (b) ideal system with external equivalent input sources of offset, (c) system with bias current and offset current, and (d) compensating offset.

The offset of both inputs should be represented by an offset voltage and bias current. The two offset voltages can be combined into one, as shown in Fig. 3.5b. The bias current flowing into the non-inverting input is not equal to that flowing into the inverting input. In practice a system with a differential input is specified using:

- One offset voltage, U_{os},
- A common bias current, which is the average of I_{bias1} and I_{bias2}: I_{bias}= (I_{bias1}+I_{bias2})/2, and
- The offset current, which is the difference: I_{os}= (I_{bias2}-I_{bias1})/2, as shown in Fig. 3.5c (I_{bias1}= I_{bias}- I_{os} and I_{bias2}= I_{bias}+ I_{os}).

Finally, the system can be made free of offset (U_o= 0) when applying the offset voltage and current source of inverse polarity to the input circuit, as is shown in Fig. 3d.

It should be noted that the offset current is sometimes specified as: I_{os}= I_{bias2}-I_{bias1}. Of course, this is not fundamentally different from the definition on page 66. However, the definitions of I_{bias} and the value of the current sources in Fig. 3.5 would have to be adjusted for consistency.

3.3.2 The effect of source impedance on offset

So far the equivalent input offset sources have been discussed without considering the effect of source resistance R_g. This is a fundamental issue. **Since offset is a property of the system (read-out circuit), offset has to be specified independently from the source used to drive that system**.

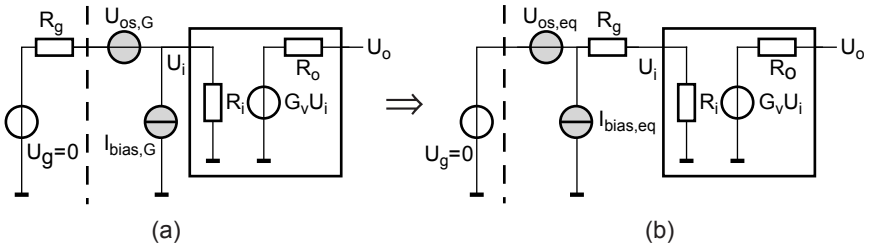

Figure 3.6, Increased offset due to source impedance.

Therefore, the calculation of the equivalent offset voltage and the bias current can be carried out using the technique presented in the previous section. However the short-circuiting of the input should include the source impedance. This is demonstrated by considering the voltage amplifier in Fig. 3.6a. The amplifier with voltage gain G_v has the equivalent input offset sources, which are specified

as: $U_{os,G}$ and $I_{bias,G}$. The effect of R_g can be calculated by making this resistor part of the read-out circuit, as shown in Fig. 3.6b, and calculating the equivalent input offset sources, $U_{os,G}$ and $I_{bias,G}$, of this extended circuit.

In the case of open input terminals, the output voltage is expressed as:

$$\left.\begin{array}{ll}(a) & U_o = G_v I_{bias,G} R_i \\ (b) & U_o = G_v I_{bias,eq} R_i \end{array}\right\} \rightarrow I_{bias,eq} = I_{bias,G} \tag{3-10}$$

The case of short-circuited input terminals yields:

$$\left.\begin{array}{ll}(a) & U_o = G_v (U_{os,G} + I_{bias,G} R_g) \dfrac{R_i}{R_i + R_g} \\ (b) & U_o = G_v U_{os,eq} \dfrac{R_i}{R_i + R_g} \end{array}\right\} \rightarrow U_{os,eq} = U_{os,G} + I_{bias,G} R_g \tag{3-11}$$

The offset voltage dominates in the case of read-out of a voltage source with a relatively small R_g, thus requiring a read-out circuit with a low equivalent input offset voltage. The bias current is relatively unimportant, which could be an advantage when selecting the most suitable amplifier.

Although the source impedance is not considered in the calculation of the equivalent input offset sources, the practical source impedance does adversely affect the detection limit due to offset. In the case of the read-out of a voltage with a relatively large source resistance, R_g, the voltage drop across this resistor due to the bias current ($I_{bias}R_g$) becomes comparable to U_{os} and the offset performance is reduced. A similar result can be obtained or read-out of a current source with finite source impedance using a current amplifier or trans-impedance circuit with offset.

3.3.3 Offset in opamp-based circuits

Any commercially available operational amplifier has the input offset sources specified. When used in a feedback circuit the equivalent input offset sources of the entire circuit can be derived. Figure 3.7a shows a non-inverting amplifier with nominal voltage gain $G_{nom} = (R_s+R_f)/R_s$ ($A(\omega) \rightarrow \infty$).

The trans-impedance transfer function of the ideal open-loop opamp can be considered as: $U_o/I_i \rightarrow \infty$. Hence, $I_{bias,eq} = I_{bias2}$, and the transfer for short-circuited input results in the following expression for $U_{os,eq}$:

$$U_{o1} = \frac{R_s + R_f}{R_s} U_{os} - \left(I_{bias1} \frac{R_s R_f}{R_s + R_f} \right) \frac{R_s + R_f}{R_s}$$

$$U_{o2} = \frac{R_s + R_f}{R_s} U_{os,eq} \qquad U_{o1} = U_{o2} \rightarrow U_{os,eq} = U_{os} - I_{bias1} \frac{R_s R_f}{R_s + R_f} \tag{3-12}$$

Note that this derivation benefits from the output voltage $U_o = 0$ when the appropriate equivalent input offset voltage and bias current are applied by considering R_s to be in parallel to R_f between the inverting input node and ground. Moreover, any voltage directly in series with the inverting input can be 'shifted' through the opamp input towards the non-inverting input with inversion of polarity.

For $I_{bias1} = I_{bias2} = I_{bias}$ the equivalent input offset voltage is as follows: $U_{os,eq} = U_{os} - I_{bias} R_s R_f/(R_s+R_f)$. For $G_{nom} \gg 1$ ($R_f \gg R_s$) the equivalent input offset voltage can be approximated by: $U_{os,eq} = U_{os} - I_{bias} R_s$. Although the circuit is a voltage amplifier, the opamp input bias current also contributes to the equivalent input offset voltage, which is due to the feedback components.

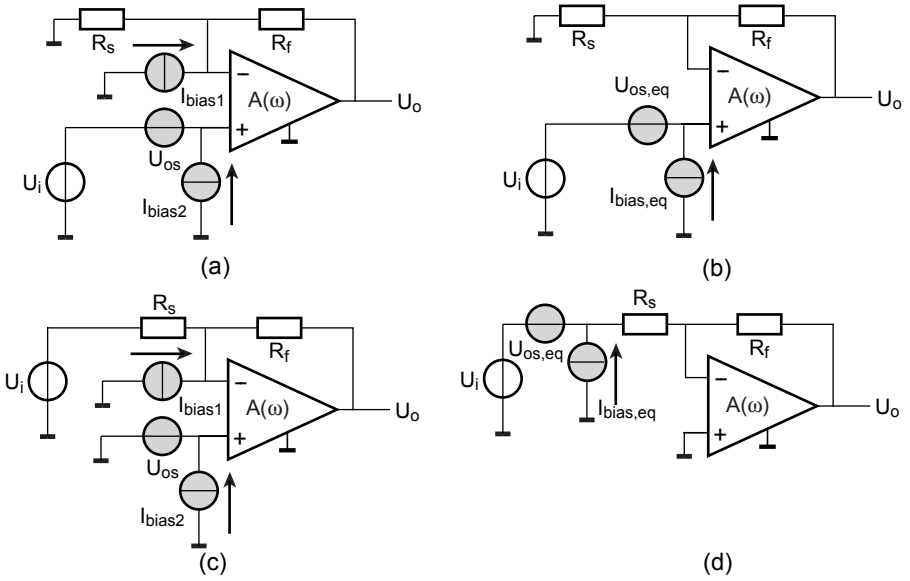

Figure 3.7, Non-inverting amplifier with (a) distributed offset voltage and bias current sources and (b) equivalent input offset voltage and bias current. **Inverting amplifier** with (c) distributed offset voltage and bias current sources and (d) equivalent input offset voltage and bias current.

Figure 3.7c shows the inverting amplifier with distributed offset and bias sources. This amplifier with equivalent offset voltage and bias current is shown

in Fig. 3.7d. There is a subtle, yet essential, difference between the equivalent input offset voltage in the circuit of the non-inverting amplifier (Fig. 3.7b) and that in the inverting amplifier (Fig. 3.7d). As a general rule the equivalent input offset voltage should be in series with the signal source to result in the detection limit. Consequently, the offset voltage is in series with the non-inverting input in case of the non-inverting amplifier (Fig. 3.7b), whereas this voltage is in series with the inverting input in the case of the inverting amplifier (Fig. 3.7d). Note, again, that the polarity of the offset voltage is not specified.

Calculating the equivalent input offset voltage and bias current of the inverting amplifier is similar to the case of the non-inverting amplifier:

$$U_{o1} = \frac{R_s + R_f}{R_s} U_{os} - \left(I_{bias1} \frac{R_s R_f}{R_s + R_f} \right) \frac{R_s + R_f}{R_s}$$

$$U_{o2} = -\frac{R_f}{R_s} U_{os,eq} \qquad U_{o1} = U_{o2} \rightarrow U_{os,eq} = -\frac{R_s + R_f}{R_f} U_{os} + I_{bias1} R_s \tag{3-13}$$

Note that I_{bias2} is short-circuited and $I_{\mathrm{bias,eq}} = I_{\mathrm{bias1}}$ is loading the input voltage source, which affects the offset voltage. For $G_{\mathrm{nom}} \gg 1$ ($R_{\mathrm{f}} \gg R_{\mathrm{s}}$), the equivalent input offset voltage can be approximated by: $U_{\mathrm{os,eq}} = -U_{\mathrm{os}} + I_{\mathrm{bias}} R_{\mathrm{s}}$. Since the polarity of the offset voltage is not specified, the offset behaviour of the inverting amplifier is very similar to that of the non-inverting amplifier.

A few issues should be mentioned:

- The offset voltage of a practical opamp can be calibrated to zero. However, an offset drift in time and with temperature remains and should be considered a source of stochastic error.
- Equation 3.12 suggests that the offset voltage can be compensated by the bias current. However, the polarity of offset is not determined (basically the specification should list: $U_{\mathrm{os}} = \pm$ value). Therefore, such a compensation is not possible.
- The bias currents are of the same polarity. Therefore, compensation is possible.
- High offset performance is usually not combined with high bandwidth. Component selection, therefore, strongly depends on the specifications demanded by the application.

Recommendations for minimising offset are:

- Select an opamp with low values for U_{os} and I_{bias}.
- Compensate the bias current.

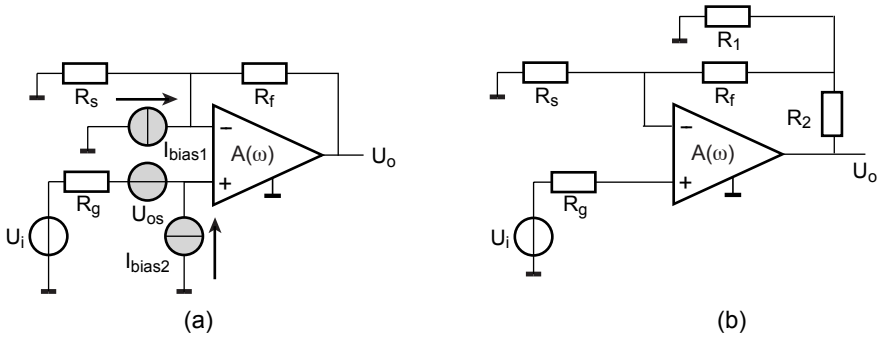

Figure 3.8, Non-inverting amplifier: (a) for read-out of voltage source with source resistance and (b) with bias current compensation using separable gain setting and bias current compensation.

Unlike the offset voltage, the bias current can be compensated in the opamp circuit using a resistor in series to the signal source. As is shown in Chapter 5, adding a resistor to the input circuit is not a good solution for maximising noise performance. However, a practical voltage source has a source resistance, R_g, as shown in Fig. 3.8a. In this case the equivalent input offset voltage of the non-inverting amplifier results in:

$$U_{o1} = \frac{R_s + R_f}{R_s} U_{os} - \left(I_{bias1} \frac{R_s R_f}{R_s + R_f} + I_{bias2} R_g \right) \frac{R_s + R_f}{R_s}$$

$$U_{o2} = \frac{R_s + R_f}{R_s} U_{os,eq} \qquad U_{o1} = U_{o2} \rightarrow U_{os,eq} = U_{os} - I_{bias1} \frac{R_s R_f}{R_s + R_f} + I_{bias2} R_g \tag{3-14}$$

Since, the bias current sources I_{bias1} and I_{bias2} are of the same polarity, compensating the bias currents is possible. Bias current compensation in the non-inverting amplifier involves selecting values for R_s and R_f such that R_f/R_s gives the required gain and simultaneously $(R_s R_f)/(R_s+R_f)$ is equal to the source resistance, R_g. The remaining offset is determined by the opamp offset voltage and the difference between the bias currents (= the offset current, see Fig. 3.5c)

However, the value of R_g is dictated by the sensor used and cannot be changed by the designer of the read-out circuit. The modified non-inverting amplifier shown in Fig. 3.8b is a solution that separates the gain setting from the bias current compensation. For $R_1 \ll R_s+R_f$ the result is:
$G_{nom} = [(R_1+R_2)/R_1] \times [(R_s+R_f)/R_s]$, while $(R_s R_f)/(R_s+R_f)$ should be dimensioned to be equal to R_g to enable bias current compensation.

Example 3.2
Figure 3.9 shows an opamp circuit for the read-out of a Pt-100 resistive temperature sensor. $R(T)= R_o(1+ \alpha T+ \beta T^2)$, with $R_o= 100\ \Omega$ at 0 ^oC, T is the resistor temperature in ^oC, $\alpha= 3.9\times10^{-3}\ K^{-1}$ and $\beta= -5.8\times10^{-7}\ K^{-2}$. The resistance of the connecting wires is indicated as r, and $U_{ref}= 6.40$ V is a reference voltage source connected to resistor $R_s= 1$ kΩ. Unless otherwise indicated:
1. The opamp can be considered ideal (no equivalent input offset or noise sources and infinitely large open-loop gain) and
2. The sensor can be considered perfectly linear ($\beta= 0$).

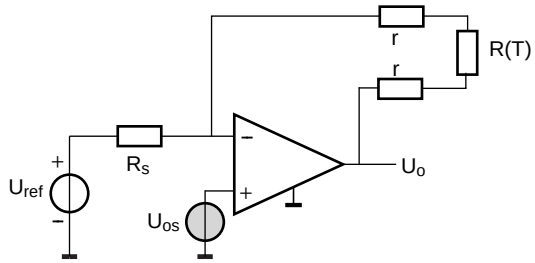

Figure 3.9, Resistive temperature sensor with lead resistor and opamp with offset.

Questions:
1. Show that the nominal sensitivity of the system (i.e. for $r = 0$ and the given component values) is equal to -2.5 mV/K.
2. Calculate the maximum acceptable connecting wire resistance, r, for an uncertainty specification $\Delta T= 0.1\ ^oC$.
3. Calculate the maximum acceptable equivalent input offset voltage, U_{os}, of the opamp ($I_{bias}= 0$) for an inaccuracy specification $\Delta T= 0.1\ ^oC$ at $T_{amb}= 0\ ^oC$, due to offset only.
4. Calculate the required absolute inaccuracy specification of U_{ref} for a temperature uncertainty of $\Delta T= 0.1\ ^oC$ at $T_{amb}= 0\ ^oC$, due to this reference voltage source only.

Solutions:
1. Inverting amplifier: $U_o= -R(T)U_{ref}/R_s= -[R_o(1+\alpha T)/R_s]U_{ref}$.
   $\partial U_o/\partial T= -\alpha R_o U_{ref}/R_s= -3.9\times10^{-3}\times 10^2\times 6.4/10^3= -2.496$ mV/K.
2. Change in resistance due to temperature: $\Delta R(T)= \alpha R_o \Delta T$
   Change in resistance due to r: $\Delta R= 2r$
   $\rightarrow r_{max}= \alpha R_o \Delta T_{max}/2= 3.9\times10^{-3}\times 10^2\times 0.1/2= 19.5$ mΩ.
3. $\Delta U_o= (\partial U_o/\partial T)\Delta T+ (\partial U_o/\partial U_{os})U_{os}= 0$
   $\partial U_o/\partial T= -2.5$ mV/K.
   $U_o/U_{os}= (R(T)+R_s)/R_s \rightarrow \partial U_o/\partial U_{os}= (R(T)+R_s)/R_s$

$\rightarrow 1.1U_{os,max} - 2.5\times10^{-4} = 0$. Hence, $U_{os,max} = 227\ \mu V$.

4. $\Delta U_o = (\partial U_o/\partial T)\Delta T + (\partial U_o/\partial U_{ref})\Delta U_{ref} = 0$
   $\partial U_o/\partial T = -2.5$ mV/K.
   $U_o/U_{ref} = -R(T)/R_s \rightarrow \partial U_o/\partial U_{ref} = -R(T)/R_s$
   $\rightarrow -0.1\Delta U_{ref,max} - 2.5\times10^{-4} = 0$. Hence, $\Delta U_{ref,max} = 2.5$ mV.

Offset in an amplifier sets the detection limit for DC read-out. In other circuits offset could be even more disruptive.

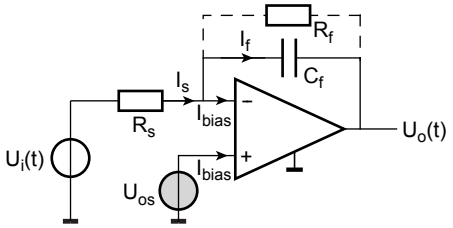

Figure 3.10, Offset in an integrator.

In the integrator shown in Fig. 3.10, care should be taken to avoid the output from saturation at the power supply level resulting from the charging of the feed-back capacitor by the bias current. The transfer function for U_{os}=0 and I_{bias}=0 and without R_f is described by:

$$\begin{aligned} U_- &= U_i = 0 \\ I_s(t) &= \frac{U_i(t)}{R_s} \\ U_o(t) &= -\frac{1}{C_f}\int I_s(t)dt = -\frac{1}{R_s C_f}\int U_i(t)dt \end{aligned} \tag{3-15}$$

The initial charge on C_f can be included by addition of the term $U_o(t_o) = -Q(t_o)/C_f$. However, when including the offset components the output voltage is described by:

$$\begin{aligned} U_- &= U_{os} \\ I_s(t) &= \frac{U_i(t) - U_{os}}{R_s} \\ U_o(t) &= -\frac{1}{C_f}\int \left(I_s(t) - I_{bias}\right)dt = -\frac{1}{R_s C_f}\int \left(U_i(t) - U_{os} - R_s I_{bias}\right)dt \end{aligned} \tag{3-16}$$

I_{bias} cannot be distinguished from I_s (in the case of a DC source) and the virtual ground changes with offset voltage. Therefore, at $U_i(t) = 0$ the output voltage increases linearly in time and can be expressed as: $U_o(t) = [I_{bias} + U_{os}/R_s](t - t_o)/C_f$,

until the output saturates at the power supply voltage level. This effect can be circumvented by connecting a (large-value) resistor R_f in parallel to this feedback capacitor or by a periodic short-circuiting (discharging) of the feedback capacitor using a switch across C_f.

Example 3.3
The integrator shown in Fig. 3.10 is designed for R_sC_f= 1 s and is fabricated using an opamp with the offset specifications: U_{os}= 1 mV and I_{bias}= 10 nA. At time t_o the feedback capacitor C_f is discharged. Analyse the effect of the offset components on the output voltage, U_o.

Solution:
Selecting R_s= 100 kΩ and C_f= 10 µF yields:
$U_o(t) = (10^{-8}+10^{-3}/10^5)/10^{-5}(t-t_o)= 2\times10^{-3}\times(t-t_o)$.

Assume a maximum output voltage at 5 V results in saturation after 2500 s. This effect is circumvented using a resistor R_f connected in parallel to C_f. For R_f= 10 MΩ the maximum output voltage due to offset is equal to:
$U_o = (R_s+R_f)U_{os}/R_s+ R_fI_{bias}$= 201 mV.

The lower limit in the frequency range where this circuit actually performs integration of the input signal is set to $\omega_{min}= (R_fC_f)^{-1}= 10^{-2}$ rad/s.

3.4 Offset in sensor read-out

3.4.1 Offset in Hall plates

The most-popular magnetic field sensor is based on the Hall effect. This effect describes the build-up of an electric field in a direction perpendicular to the flow direction of charged particles and the direction of the magnetic field. Figure 3.11 shows such a Hall plate with a current source, I_{exc}, applied to the current contacts and a Hall voltage, U_H, measured across the voltage contacts.

A charged particle moving through a magnetic field experiences a Lorentz force. If the velocity vector $\underline{v}$, and the magnetic field vector, $\underline{B}$, are orthogonal, as depicted in the figure, the Lorentz force is described by the product of their magnitude and the unit charge: $F_L= -qvB$. The Lorentz force causes a deflection of the particle and thus a charge gradient in the direction perpendicular to the velocity vector. This charge gradient creates a Hall field with such a polarity that it counteracts the Lorentz force. In the steady state, which is reached within femtoseconds, the force due to the Hall field equalises the Lorentz force: $E_H= F_L/q= vB$.

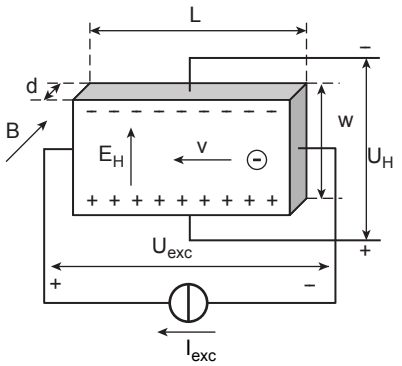

Figure 3.11, Operating principle of the Hall sensor.

In a simplified model it is assumed that due to the Lorentz force electron accumulation initially takes place at the negative Hall voltage contact. The average electron drift velocity is coupled to the current density, $J = I_{exc}/(dw)$, via the definition of current density, which is the amount of charge passing through a certain cross sectional area per unit time: $J = \partial Q/\partial t = -nq/v^{-1} = -nqv$, where n denotes the electron density [m^{-3}]. Therefore, $v = -J/nq$ and $E_H = vB = -JB/(nq)$. Introducing the actual dimensions of a Hall plate as shown in the figure yields:

$$U_H = -E_H \cdot w = \frac{JB}{nq} w = \frac{I}{dw}\frac{B}{nq} w = \frac{1}{nq}\frac{I}{d} B = R_H \frac{I}{d} B, \qquad (3\text{-}17)$$

where R_H denotes a material-dependent Hall constant ($0.8 < R_H < 1.2$). The derivation of expression 3-17 in the solid state is complicated by lattice interaction. Nevertheless, it yields the same expression and the complications are included in the Hall constant.

The most important conclusion to be drawn from expression 3-17 is that the Hall voltage is linearly dependent on both the magnetic field and the current fed through the Hall plate. A consequence is that variations in this excitation current (i.e. bias current) directly affect the measurement result and thus add to the uncertainty. Very stable current sources are available, so this effect usually does not determine the detection limit.

The main problem of the Hall sensor is the offset, which results from two practical constraints:

- The placement of the contacts is critical. Special care must be taken to have the voltage and current contacts exactly opposite each other. Misalignment of the voltage contacts is a cause of offset.
- Any stress gradient in the resistive layer that forms the Hall plate results in offset due to the piezo-resistive effect.

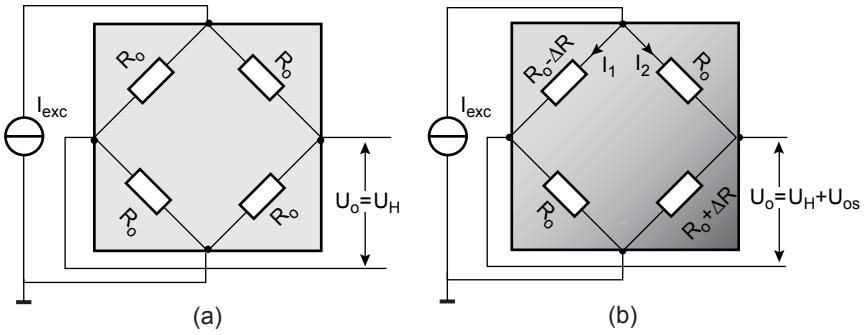

Figure 3.12, (a) The Hall plate represented by a balanced symmetric Wheatstone bridge and (b) modelling of a stress gradient in the material.

These effects result because the Hall plate is actually a Wheatstone bridge. The Hall voltage is measured across the voltage contacts, which are located halfway between the current contacts and perpendicular to the current direction. The ideal Hall plate can, therefore, be considered a fully symmetric Wheatstone bridge with current excitation and voltage read-out, as shown in Fig. 3.12a. For B= 0 T the bridge is balanced (i.e. there is a resistor R_o between every node).

A practical Hall plate, however, usually suffers from an initial imbalance due to contact misalignment and/or gradient in the built-in residual mechanical stress, σ. As a result the nominal values for B= 0 T are not equal, thus yielding the asymmetric Wheatstone bridge. Figure 3.12b shows the circuit assuming a stress gradient from the upper-left corner to lower right corner. It should be noted that a constant residual stress level does not impose a problem, since all four resistors change by the same amount.

In this simplified model only one of the bridge resistors is assumed to depend on mechanical stress via the resulting strain and its piezo-resistivity: $R(\sigma)= R_o(1+\Delta R/R_o)= R_o(1+k_\sigma \Delta L/L)= R_o(1+k_\sigma \sigma/E)$, where E denotes the Young's modulus of the material and L is the length of the resistive layer. In the case of perfect alignment and only a stress gradient in the material, the output voltage of the Hall plate results as a function of the bridge imbalance:

$$I_1 = \frac{2R_o + \Delta R}{4R_o} I_{exc}$$

$$I_2 = \frac{2R_o - \Delta R}{4R_o} I_{exc}$$

$$U_{o,os} = I_2\left(R_o + \Delta R\right) - I_1 R_o = \frac{\left(2R_o - \Delta R\right)\left(R_o + \Delta R\right) - \left(2R_o + \Delta R\right)R_o}{4R_o} I_{exc} \rightarrow \tag{3-18}$$

$$\frac{U_{o,os}}{I_{exc}} = -\frac{R_o}{4}\left(\frac{\Delta R}{R_o}\right)^2 = -\frac{R_o}{4}\left(\frac{k_\sigma \Delta\sigma}{E}\right)^2$$

Combining equations (3-17) and (3-18) yields the expression for $U_o = U_H + U_{os}$.in terms of the magnetic field, B, and the stress gradient, $\Delta\sigma$, which can be used to calculate the detection limit.

3.4.2 Temperature measurement using thermocouples

Some sensors intrinsically lack offset. An example is the thermocouple used for measuring temperature differences. The operation is based on the **Seebeck effect**.

The Seebeck effect is observed when making physical contact between two different (semi)conductor materials, while the two points of contact (the junctions) are at different temperatures and results in a voltage difference proportional to the temperature difference: the Seebeck voltage.

The **Seebeck voltage** is in fact the difference in contact potential at the junctions and is basically due to the temperature-dependent alignment of the different Fermi levels in the different (semi)conductors. The potential difference is solely dependant on the choice of the two materials and, for instance, not on the contact area. The temperature dependence of the contact potential at a junction is a material property and is referred to as the **Seebeck coefficient** of the material, α_{mat}:

$$\alpha_{mat} = \frac{1}{q} \times \frac{dE_F}{dT} \tag{3-19}$$

Typical values are in the ±10 μV/K range. However, this property cannot be directly measured using a Volt meter, since the electrical circuit would have to be closed. As shown in Fig. 3.13a, this would introduce a second material, therefore resulting in a second junction between the same materials at the meter. In the second junction the same potential difference is generated, which is, however, of

opposite polarity. Thus resulting in an overall voltage of zero. Therefore, two different materials with significantly different values for the Seebeck coefficient have to be used, as shown in Fig. 3.13b.

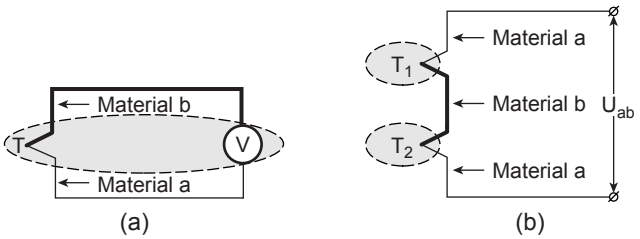

Figure 3.13, Thermocouple formed by the interconnection of two different metals with different Seebeck coefficients.

The output voltage of the thermocouple is described by:

$$U_{ab} = \alpha_{ab}(T_1 - T_2) \tag{3-20}$$

with U_{ab} as the Seebeck voltage. A non-zero Seebeck voltage results only if the junctions are at different temperatures. The junction at the lower temperature is usually referred to as the **cold junction** and the junction at a high temperature as the **hot junction**. The advantage of the thermocouple is its suitability for high-temperature measurement (up to 1500 ^{o}C). The non-linearity of the Seebeck effect is incorporated into the temperature dependence of the Seebeck coefficient.

Although the thermocouple lacks offset when measuring a temperature difference, there are two complications:

- Most applications require an absolute temperature measurement, which can be achieved by establishing a zero-reference at the cold junction (using a beaker with melting ice or, more practically, by measuring the temperature at that junction using a Pt-100 probe). The uncertainty in the temperature measurement at the cold junction results in an offset in the thermal domain.
- The voltage generated is very small and the equivalent input offset voltage of the read-out dominates the performance.

The detection limit of a thermocouple with a sensitivity of α_{ab}= 50 μV/K is at 10 K if a voltage amplifier is used with an equivalent input offset voltage at 0.5 mV. The temperature sensitivity is enhanced by placing several thermocouples electrically in series and across the same temperature difference in a thermopile, as

shown in Fig. 3.14. Consequently, the effect of the equivalent input offset voltage of the read-out is reduced.

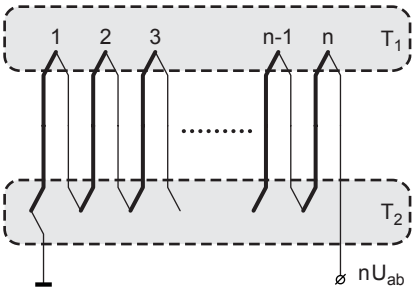

Figure 3.14, Thermopile structure using several thermocouples electrically in series across a temperature difference.

A thermopile composed of *n* thermocouples generates *n*-times the Seebeck voltage of one thermocouple. However, the source impedance is also *n*-times as large, which results in *n*-times the noise power. In addition, the multiple leads between the hot and the cold junction increase the thermal leak and thus results in loading of the measurand, which may not be acceptable in some applications. These issues are addressed in more detail in Chapters 5 and 8, respectively.

3.4.3 Detection limit in the Wheatstone bridge due to offset

Figure 3.15 shows the circuit used to read-out a Wheatstone bridge using a differential amplifier, as discussed in the next chapter.

At this stage it is important to analyse the detectivity due to DC excitation. Since DC signals cannot be distinguished from offset, the effect of offset has to be considered. Assume that the offset of the differential amplifier is specified by the equivalent input offset voltage, U_{os}, and the bias by two bias current sources, I_{bias1} and I_{bias2}. The differential voltage at the input of the amplifier results in:

$$\begin{aligned} U_{id} = U_{oW} + U_{os,eq} &= \frac{\Delta R}{R_o}U_{exc} + \frac{R_1R_4}{R_1+R_4}I_{bias2} - \frac{R_2R_3}{R_2+R_3}I_{bias1} + U_{os} = \\ &\frac{\Delta R}{R_o}U_{exc} + U_{os} + \frac{\left[\left(R_o-\Delta R\right)\left(R_o+\Delta R\right)\right]\left(I_{bias2}-I_{bias1}\right)}{\left(R_o-\Delta R\right)+\left(R_o+\Delta R\right)} = \\ &\frac{\Delta R}{R_o}U_{exc} + U_{os} + \frac{R_o^2-\Delta R^2}{2R_o}\left(I_{bias2}-I_{bias1}\right) \end{aligned} \tag{3-21}$$

Assuming an inaccuracy specification at ε results in a detection limit set by offset at U_{id}=0:

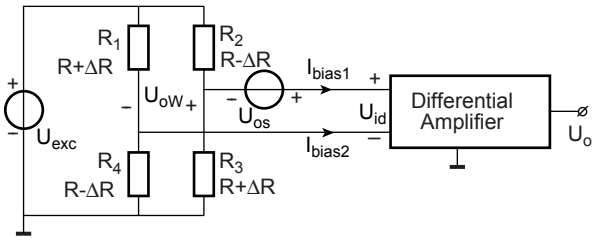

Figure 3.15, Offset in the read-out of a Wheatstone bridge.

$$\left(\frac{\Delta R}{R_o}\right)_{\text{det}} = \frac{1}{\varepsilon}\frac{U_{os,eq}}{U_{exc}} \simeq \frac{U_{os} + R_o I_{os}}{\varepsilon U_{exc}} \tag{3-22}$$

For U_{exc} = 5 V, ΔR= 0.0002×R_{o}, R_{o}= 1 kΩ, U_{os} = 0.5 mV, I_{os}= 1 nA and ε= 1%, the result is: U_{id}= U_{oW}+ $U_{\text{os,eq}}$= 1 μV+ 501 μV and $(\Delta R/R_{\text{o}})_{\text{det}}$= 10^{-2}.

3.5 Exercises

3.1 The specified offset voltage of a voltage source is equal to 3 mV. A Volt meter with an equivalent input offset voltage equal to 1 mV is used for DC voltage measurement. Calculate the total offset of the measurement.

Solution: Linear addition of offset voltages: 3mV+ 1mV = 4mV.

A voltage-to-current converter (trans-conductance), g_{m1}, is cascaded with a current amplifier, as shown in Fig. 3.16, to give an overall trans-conductance equal to: G_{m}= g_{m1}× G_{i2}.

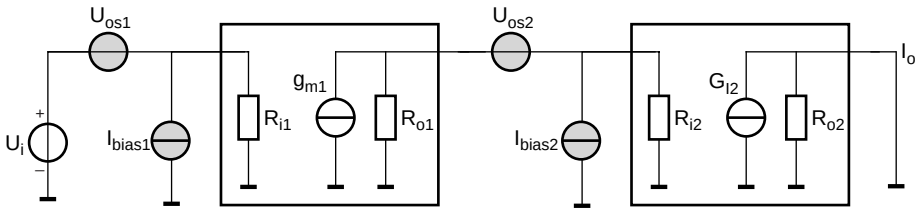

Figure 3.16, Trans-conductance circuit.

The specifications of the equivalent input offset sources of the sub-systems are:

- $U_{os1}= U_{os2}= 1$ mV, $I_{bias1}= I_{bias2}= 10$ μA.
- $R_{i1}= R_{o1}= R_{o2} \rightarrow \infty$, $R_{i2}= 0$,
- $g_{m1}= 100$ mA/V and $G_{i2}= 10$.

3.2 Calculate the equivalent input offset sources, $U_{os,eq}$ and $I_{bias,eq}$.

Solution:
Since $R_{o1} \rightarrow \infty$ and $R_{i2}= 0$, U_{os2} has no effect. The equivalent input offset voltage due to I_{bias2} results from: I_{bias2}/g_{m1} = 10 μA/100 mA/V= 0.1 mV. This offset voltage source is in series with U_{os1}. Hence: $U_{os,eq}= U_{os1}+ 0.1$ mV = 1.1 mV. Similarly, $I_{bias,eq} = I_{bias1}$=10 μA.

3.3 The system transfer function and the specifications of the equivalent input offset voltage sources of the sub-systems in Fig. 3.16 remain unchanged:

- $g_{m1}= 100$ mA/V and $G_{i2}= 10$,
- $U_{os1}= U_{os2}= 1$ mV.

However, more realistic values for the bias currents and input and output impedances are used:

- $I_{bias1}= 1$ nA, $I_{bias2}= 1$ μA,
- $R_{i1}= R_{o1}= R_{o2}= 1$MΩ, $R_{i2}= 100$ Ω.

Calculate the equivalent input offset sources, $U_{os,eq}$ and $I_{bias,eq}$.

Solution:
This is the more general case of the problem presented in the previous question. $U_{os,eq}= U_{os1}+ U_{os2}/[g_{m1}R_{o1}]+ I_{bias2}/g_{m1}$ and $I_{bias,eq}= I_{bias1}+ U_{os2}/[g_{m1}R_{i1}R_{o1}]+ I_{bias2}/[g_{m1}R_{i1}]$. For $R_{i1}= R_{o1}= 1$MΩ: $U_{os,eq}\sim 1.01$ mV and $I_{bias,eq}= 1.01$ nA.