Chapter 2
Dynamic Offset Cancellation Techniques for Operational Amplifiers

At low frequencies, offset, 1/*f* noise and drift are the dominant error sources of operational amplifiers. This is especially true in CMOS technology. This chapter reviews precision techniques that can be used to achieve low 1/*f* noise and low offset in operational amplifiers.

There are three types of CMOS offset cancellation techniques: trimming, chopping, and auto-zeroing. Trimming is usually performed during production to eliminate offset. Auto-zeroing is a sampling technique in which the offset is measured and then subtracted in subsequent clock phases. Chopping, on the other hand, is a continuous-time modulation technique in which the signal and offset are modulated to different frequencies. Due to the modulated offset and 1/*f* noise, a chopper ripple appears at the amplifier output. Since chopping and auto-zeroing are dynamic techniques that continuously reduce offset, they also remove low frequency 1/*f* noise as well as offset drift over temperature or time.

In auto-zeroing amplifiers, the residual offset is mainly caused by charge injection and clock feed-through. While in chopper amplifiers, the residual offset is mainly caused by demodulated clock feed-through spikes. Several techniques can be used to counteract these non-idealities.

Later in this chapter, several dynamic-offset-compensation techniques used in operational amplifiers will be discussed, e.g. ping-pong auto-zeroing, offset stabilization, and specifically, chopper offset stabilization of a low-frequency path in a multi-path amplifier. To suppress chopper ripple, numerous ripple reduction techniques can be used. It will be shown that these all have significant drawbacks, and thus new techniques are required.

R. Wu et al., *Precision Instrumentation Amplifiers and Read-Out Integrated Circuits*, Analog Circuits and Signal Processing, DOI: 10.1007/978-1-4614-3731-4_2,

2.1 Introduction

For sensor applications, the bandwidth of interest is generally a few Hz. In this bandwidth, offset, 1/*f* noise and drift are the dominant error sources. Thus, dynamic offset cancellation techniques are required to mitigate these errors. Before those dynamic offset cancellation techniques are discussed, it is necessary to first understand the nature and origins of these error sources.

2.2 Low Frequency Errors

2.2.1 Offset

In CMOS technology, the worst-case offset of a differential input pair can be as large as 10 mV [1]. This offset is caused by manufacturing variation or uncertainty. For example, MOS devices exhibit threshold voltage (V_{th}) mismatch because V_{th} is a function of the doping levels in MOS channels and the gates, and these parameters vary randomly from one device to another.

On the other hand, the dimensions of MOS devices suffer from random, microscopic, variations during fabrication and hence there is mismatch between the equivalent lengths and widths of nominally identical transistors. This mismatch can be reduced by using large devices. However, this increases chip area and therefore production cost.

2.2.2 1/f Noise

1/*f* noise is mainly caused by the defects in the interface between the gate oxide and the silicon substrate, so it depends on the "cleanness" of the oxide-silicon interface and may be considerably different from one CMOS technology to another [2, 3]. The typical 1/*f* noise corner frequency of CMOStechnology is in the order of several kHz to tens of kHz, making the 1/*f* noise a dominant error source at low frequencies. Related to the lifetime of the carriers, the 1/*f* noise can be modeled as a function of frequency [2], given by:

$$V_n^2 = \frac{K}{WLC_{ox}f} \tag{2.1}$$

where K is a process-dependent constant in the order of $10^{-25}\text{V}^2\text{F}$, W and L are the width and length of the MOS transistor, C_{ox} is the gate capacitance per unit area, and f is the operation frequency. Generally, 1/*f* noise in PMOS is much lower than NMOS in most technologies.

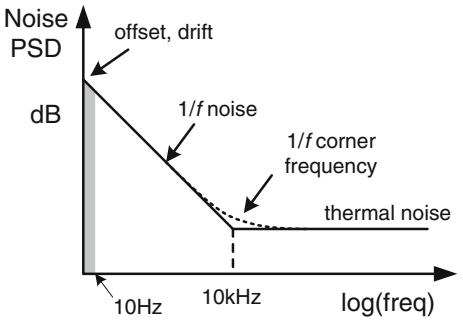

Fig. 2.1 Low frequency noise spectrum for CMOS amplifier

In (2.1), the noise spectral density of the 1/*f* noise is inversely proportional to the frequency. The inverse dependence of (2.1) on the area of the transistor *WL* suggests that to decrease 1/*f* noise, the device area must be increased. However, this again increases chip area.

2.2.3 Drift

Drift is caused by the cross-sensitivity of some error sources to temperature or time. Low drift is a critical requirement for precision temperature measurement (e.g. thermistor bridges and thermocouples), since the drift of the interface electronics can then not be distinguished from the sensor signal itself.

Drift mainly manifests itself as offset drift and gain drift. Thus it can be reduced by suppressing the offset and gain error to a low enough level, and furthermore by dynamically compensating for their temperature drift.

To conclude, Fig. 2.1 depict the low frequency errors in CMOS amplifier. As can be seen in the bandwidth of a few Hz for bridge transducer applications, the main errors are caused by 1/*f* noise, offset, and drift. To mitigate these errors, dynamic offset cancellation techniques can be employed, which will be described in the next section.

2.3 Dynamic Offset Cancellation Techniques

To reduce offset, three types of offset cancellation techniques can be applied: trimming, auto-zeroing, and chopping. Trimming involves measuring and then reducing the offset during production. While this approach can be used to obtain an order-of-magnitude reduction of the offset, it is unable to reduce the initial mV-level offset below a few tens of μV, because offset drift is not compensated for. Moreover, trimming does not eliminate low-frequency noise, such as 1/*f* noise. Dynamic offset cancellation techniques, such as auto-zeroing or chopping are therefore needed to counteract this problem.

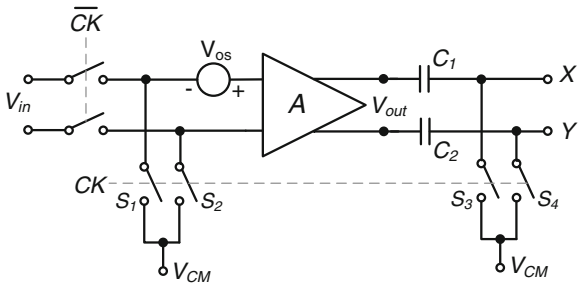

Fig. 2.2 Auto-zeroing with output offset storage

2.3.1 Auto-Zeroing

Auto-zeroing is a discrete-time sampling technique. It involves sampling the offset of the amplifier in one clock phase, and then subtracting it from the input signal in the other clock phase. There are three basic topologies for auto-zeroing [4]: output offset storage (also called open-loop offset cancellation), input offset storage (also called closed-loop offset cancellation) and closed-loop offset cancellation using an auxiliary amplifier.

2.3.1.1 Output Offset Storage

Figure 2.2 depicts an auto-zeroed amplifier with output offset storage. When CK is high, the amplifier is in the auto-zeroing phase in which its inputs are shorted together, driving its output to $V_{\text{out}} = A{\cdot}V_{\text{os}}$. During this period, nodes X and Y are shorted together as well. When all the node voltages are settled, $A{\cdot}V_{\text{os}}$ is stored across C_1 and C_2. When CK turns low, the amplifier enters the amplification phase. The differential input voltage together with Vos is amplified, and stored on C_1 and C_2. Since V_{os} is already stored on C_1 and C_2, V_{X} and V_{Y} does not see V_{os}, which is fully cancelled.

When a switch opens, it injects some charge into the surrounding circuitry. This charge consists of gate-source/drain channel charge and charge injected through the overlap capacitances (also known as clock feed-through). In reality, the charge injection in the switches S_3 and S_4 will not completely cancel. The mismatch charge injection results in a residual offset, given by

$$V_{os,res} = \left(\frac{q_{inj3}}{C_1} - \frac{q_{inj4}}{C_2}\right)/A, \tag{2.2}$$

where q_{inj3} and q_{inj4} are the charge injection caused by switches S_3 and S_4, A is the DC gain of the amplifier. Note that if A is large, $A{\cdot}V_{\text{OS}}$ may saturate the amplifier's output. For this reason, A is typically chosen to be between 10 and 100 [2]. An integrated amplifier with three cascaded auto-zeroed amplifiers with output voltage storage has been described in [4]. In [5], these stages were chopped, resulting in a low drift MOSFET operational amplifier.

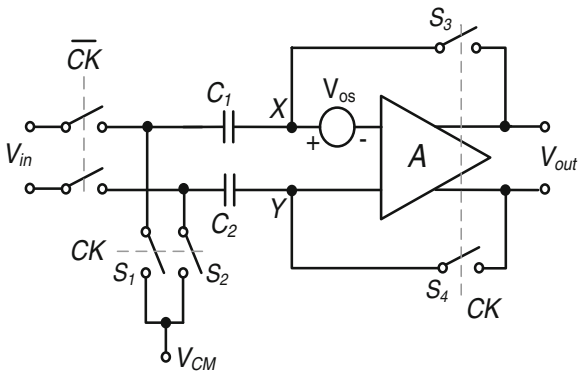

Fig. 2.3 Auto-zeroing with input offset storage

2.3.1.2 Input Offset Storage

The output offset storage technique limits the maximum gain of the amplifier. If a high gain is needed, storing the offset at the input storage capacitance would be a better solution. Figure 2.3 shows the basic principle of input offset storage technique [2]. In the auto-zeroing phase when CK is high, the output and input of the amplifier are shorted together by switches S_1 and S_2, placing the amplifier in a unity-gain configuration.

When the node voltages are settled, the output voltage V_{out} is given by

$$V_{out} = \frac{A}{1+A} \cdot V_{OS}. \tag{2.3}$$

The circuit reproduces the amplifier's offset at nodes X and Y, storing the result on C_1 and C_2. Note that for a zero differential input, the differential output is equal to V_{OS}. Thus, the input-referred offset voltage of the overall circuit equals V_{OS}/A if S_3 and S_4 match perfectly.

If S_3 and S_4 have any mismatch, this will cause mismatch charge injection and, in turn, lead to a residual offset, which is given by

$$V_{res} \approx \frac{V_{OS}}{A+1} + \left(\frac{q_{inj3}}{C_1} - \frac{q_{inj4}}{C_2}\right), \tag{2.4}$$

where q_{inj3} and q_{inj4} are the charge injection caused by switches S_3 and S_4, and A is the DC gain of the amplifier.

From (2.4), the offset V_{os} is suppressed by the gain of the amplifier. The charge injection and the leakage of the capacitors can be reduced by increasing the size of the capacitors, but cannot be suppressed by the gain because the capacitors are directly at the amplifier input.

The drawback of input offset storage and output offset storage is that they introduce capacitors in the signal path. The bottom-plate parasitic of the capacitors decreases the amplifier bandwidth, thus degrading its phase margin and stability.

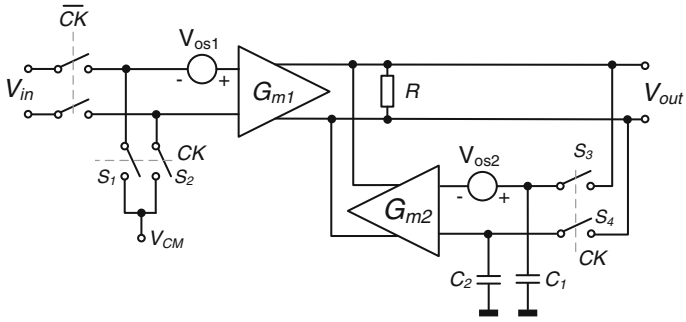

Fig. 2.4 Auxiliary amplifier placed in a feedback loop during offset cancellation

2.3.1.3 Closed-Loop Offset Cancellation with Auxiliary Amplifier

To mitigate the stability issue, closed-loop offset cancellation with an auxiliary amplifier can be used to isolate the offset storage capacitors from the signal path, as shown in Fig. 2.4.

In the auto-zeroing phase, the inputs of G_{m1} are shorted. Thus, the output voltage V_{out} can be calculated as

$$[G_{m1}V_{OS1} - G_{m2}(V_{out} - V_{OS2})]R = V_{out,AZ} \tag{2.5}$$

Thus,

$$V_{out,AZ} = \frac{G_{m1}RV_{OS1} + G_{m2}RV_{OS2}}{1 + G_{m2}R}. \tag{2.6}$$

This voltage is stored on C_1 and C_2 after S_3 and S_4 turn off. The offset voltage referred to the main input is given by

$$V_{OS,res} = \frac{V_{out,AZ}}{G_{m1}R} \approx \frac{V_{OS1}}{G_{m2}R} + \frac{V_{OS2}}{G_{m1}R}. \tag{2.7}$$

The charge injection due to the mismatch of S_3 and S_4 contributes to the offset of G_{m2}. In order to attenuate this charge injection, as seen from (2.7), G_{m2} is usually chosen to be at least 50 times smaller than G_{m1}.

Note that in an auto-zeroed amplifier, half of the clock period is used for auto-zeroing, so the amplified output is only available during part of the clock period. Such amplifiers cannot provide a continuous-time output, unless a ping-pong topology is employed [4, 6].

As seen from the discussion above, these three offset cancellation techniques cancel offset by periodically subtracting the offset obtained during the previous sampling moment. This assumes that the offset does not change too much during the amplification time. Since low-frequency noise and DC offset can not be

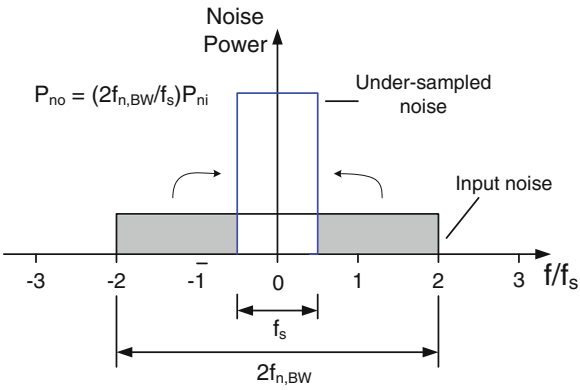

Fig. 2.5 Noise spectrum of a sampled system

distinguished from each other, these techniques also eliminate 1/*f* noise and drift. However, the sampling action of the auto-zeroing techniques affects the amplifier's noise performance at frequencies below the sampling frequency [4].

2.3.1.4 Noise in Auto-Zeroing

As discussed above, auto-zeroing is a sampling technique. To complete settle within a half clock cycle, the noise bandwidth $f_{n,\,BW}$ (determined by the time constant of the system) is usually chosen to be larger than the auto-zeroing frequency f_{AZ}, so that the under-sampled noise folds back to DC, increasing the noise PSD at the baseband.

The amount of folded noise to DC depends on the noise bandwidth $f_{n,\,BW}$ and the auto-zeroing frequency f_{AZ}. An exact quantitative calculation for the folded noise of auto-zeroing can be found in [4, 7]. Since, this is rather complex, a more intuitive explanation of noise folding in auto-zeroing is described here.

The noise folding factor n is defined as the ratio between the noise bandwidth and the auto-zeroing frequency, as given by

$$n = \frac{2f_{n,BW}}{f_{AZ}}. \tag{2.8}$$

Due to under-sampling, the noise power after sampling increases by this factor as compared to that before sampling (Fig. 2.5), thus incurring a noise penalty. This implies that by choosing a small $f_{n,\,BW}$, the folded noise can be restricted. Applying this concept, a slow-settling nulling loop is used in [8, 9] to reduce the noise bandwidth to a fraction of the auto-zeroing frequency. This approach will be discussed in Sect. 2.3.2.

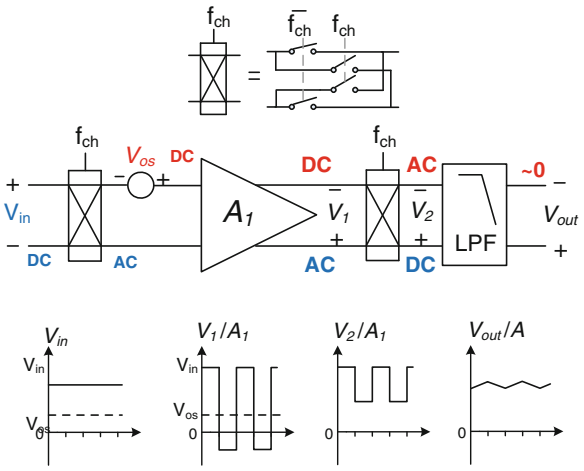

Fig. 2.6 Chopping principle in the time domain

2.3.2 Chopping

Unlike auto-zeroing, chopping is a continuous-time modulation technique that does not cause noise folding. Figure 2.6 shows a chopped amplifier together with its ideal waveforms. The input voltage V_{in} first passes through a chopper driven by a clock at frequency f_{ch}, thus it is converted to a square wave voltage at f_{ch}. Next, the modulated signal is amplified together with its own input offset. The second chopper then demodulates the amplified input signal back to DC, and at the same time modulates the offset to the odd harmonics of f_{ch}, where they are filtered out by a low-pass filter (LPF). This results in an amplified input signal without offset.

Low-frequency errors, such as $1/f$ noise and drift will be modulated and filtered out along with offset. This can be seen in Fig. 2.7, which depicts chopping in the frequency domain. To completely remove the $1/f$ noise, the chopping frequency should be higher than the $1/f$ noise corner frequency. At the beginning, the signal is modulated, and the noise and offset are superposed onto this modulated signal (Fig. 2.7b). After amplification and the second chopper, the modulated signal is demodulated back to DC, while the low-frequency noise and offset are modulated to the harmonics of the chopper frequency, appearing as a chopper ripple at the amplifier output (Fig. 2.7c). A LPF is then used to remove the modulated offset and $1/f$ noise, resulting in a clean low-frequency signal without offset or $1/f$ noise (Fig. 2.7d).

From the above discussion, the offset is amplified by the DC gain of A_1, while the signal is amplified by the effective gain of A_1 at the chopping frequency f_{ch}, To maximize the effective gain of the stage consisting of A_1 and two choppers, the optimum chopping frequency should be around 3 dB bandwidth of A_1 [4].

The amplitude of the chopper ripple can be calculated with the help of the simplified block diagram shown in Fig. 2.8. The chopped offset of the input stage is filtered by the main Miller compensation capacitor C_{M1} and appears as a

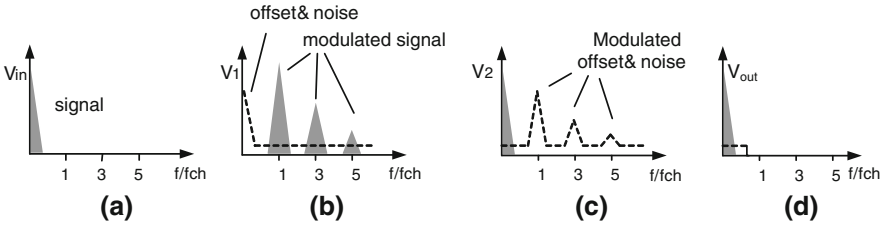

Fig. 2.7 Chopping principle in the frequency domain

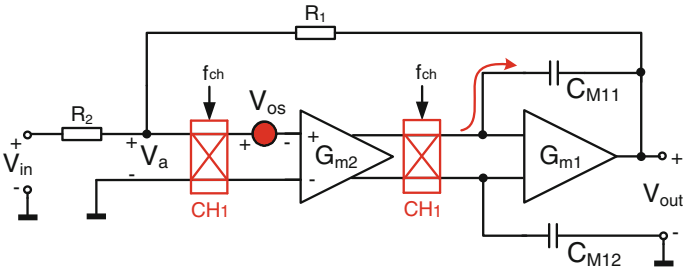

Fig. 2.8 Simplified block diagram of a chopper amplifier

triangular waveform at the output. The peak-to-peak amplitude of the ripple can then be approximated as:

$$V_{out,ripple} = \frac{V_{os} \cdot G_{m2}}{2C_{M1} \cdot f_{ch}}. \tag{2.9}$$

From (2.9), ripple amplitude can be reduced by reducing input-stage offset V_{os} with careful layout, by increasing the chopping frequency f_{ch1} or by increasing the size of the Miller compensation capacitor. For a worst-case 20 mV offset, with $G_{m2} = 250$ μA/V, $C_{M1} = 80$ pF, $V_{DD} = 5$ V, and $f_{ch1} = 40$ kHz, $V_{out,\ ripple} \approx 0.8$ V. This is quite large compared to the amplifier's maximum 5 V output range and so must be suppressed.

2.3.3 Conclusions

Both auto-zeroing and chopping techniques have been introduced. Table 2.1 compares and summarizes these two techniques. Chopping is superior to auto-zeroing because it is a continuous-time modulation technique that does not cause noise folding. However, chopping gives rise to a chopper ripple at the amplifier output. Auto-zeroing does not introduce ripple and its discrete-time nature is well compatible with switched-capacitor circuitry. Since power efficiency is an

Table 2.1 Comparison of auto-zeroing and chopping techniques

	Auto-zeroing	Chopping
Low frequency noise	±	+
Power-noise efficiency	−	+
Ripple	+	−
Residual offset	+	++

Note auto-zeroing removes 1/*f* noise, but causes the noise to fold back to DC, thus auto-zeroing in terms of low-frequency noise is denoted as "±"

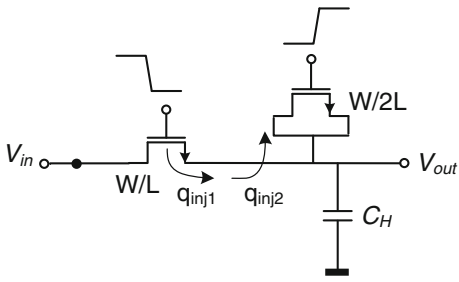

Fig. 2.9 Charge injection compensation using dummy switches

important concern in our work, chopping is applied here. In Sect. 2.5.5, various techniques will be discussed to eliminate the chopper ripple.

2.4 Charge Injection Compensation Techniques in Auto-Zeroed and Chopper Amplifiers

2.4.1 Compensation Techniques for Charge Injection

The residual offset of auto-zeroed amplifiers is mostly determined by charge injection and clock feed-through. To mitigate these two effects in a sampling circuit, several techniques can be applied.

Dummy Switches

Charge injection can be partially compensated for by adding dummy switches that are driven by a complementary clock signal and that inject an amount of charge which compensates for the charge injected by the main switch [10]. The effectiveness of the compensation depends on the matching of the injected charges. A clock signal with a high slew rate can be used to obtain an equal distribution of the channel charge in the main switch's drain and source terminals. A half-size dummy switch can then be used for compensation (Fig. 2.9). However, the assumption of equal splitting of the charge between the source and drain is generally invalid, making this approach less attractive.

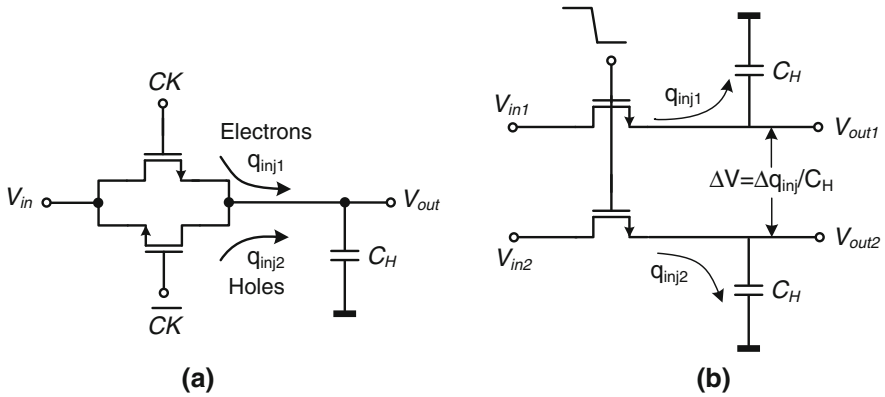

Fig. 2.10 **a** Using complementary switches to reduce charge injection **b** Using differential circuit to suppress charge injection

Using Complementary Switches

Another approach to reduce the charge injection is to use both PMOS and NMOS devices such that the opposite charge packets injected by the two cancel each other (Fig. 2.10a). However, this cancellation is only effective for a limited range of the input signal around half of the supply voltage.

Using a Fully Differential Circuit

The best way to compensate for charge injection is to use fully differential circuitry (Fig. 2.10b). If the charge injection in the two half circuits matches, the charge injection only results in a change in the common-mode voltage. A differential voltage change only results from charge-injection mismatch. With this compensation, a reduction in offset of at least 10 × can be expected.

2.4.2 Charge Injection and Clock Feed-Through in Chopper Amplifiers

For chopper amplifiers, residual offset is mainly caused by the following three issues:

- *Non-idealities in clock timing*
- *Demodulated clock feed-through current spikes*
- *Impedance mismatch between two input nodes*

Firstly, the *non-idealities in the clock timing*, such as clock skew, non-overlap and overlap in chopper clocks introduce residual offset. *Clock skew* is a phenomenon in which the two complementary chopper clocks switch at the different transition moments, as shown in Fig. 2.11a. Assuming the offset is 10 mV and the clock skew is 0.01 %, the resulting offset is 1 μV. To ensure a perfect offset

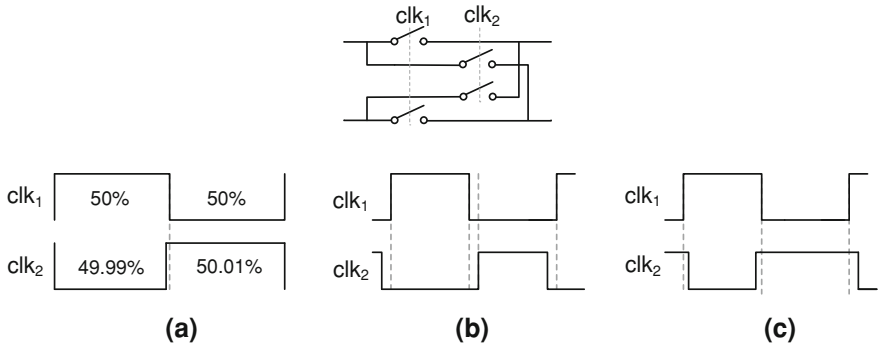

Fig. 2.11 Non-idealities in clock timing **a** Clock skew **b** Non-overlap clock **c** Overlap clock

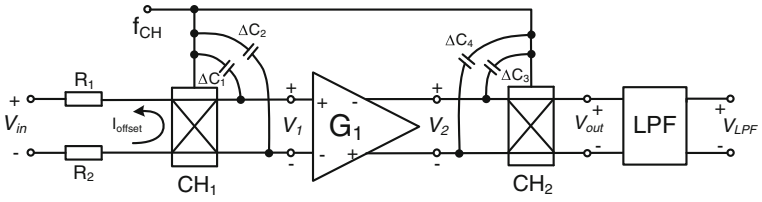

Fig. 2.12 Charge injection model in a chopper amplifier

cancellation, the two complementary chopping clocks must both exhibit 50 % duty cycle and have transitions at the same moments.

Having transitions at the same moment, means that both *non-overlap* and *overlap* of the complementary chopper clocks must be avoided. An NMOS chopper is driven by the non-overlap chopper clocks, as depicted in Fig. 2.11b. A small time gap exists when clk_1 and clk_2 are both low, hence the differential signal paths are being interrupted. This leaves the signal path not attenuated and may cause glitches at the output of the amplifier in between the choppers.

For the overlap chopper clocks (Fig. 2.11c), there is a small time interval when both clocks are high, thus causing a "short circuit" between the differential signal paths. This causes low input impedance and also shorten the amplification time between the choppers. Thus, the effective gain of the amplifier reduces, resulting in increased noise and offset.

Complementary chopper clocks with a 50 % duty cycle and the same transitions can be produced by a non 50 % duty cycle clock and a divider-by-two D-flipflop, as will be described in Sect. 4.6.5. Extra buffers can be added to reduce the rise and fall time.

Secondly, due to *clock feed-through*, the imbalance of parasitic capacitors in the choppers also causes a residual offset [11]. Figure 2.12 illustrates the charge injection due to imbalanced parasitic capacitances of the input and output choppers in a fully-differential chopper amplifier. Figure 2.13 depicts a zoom-in picture of the input and output choppers in which the current spikes caused by imbalanced parasitic capacitances are illustrated.

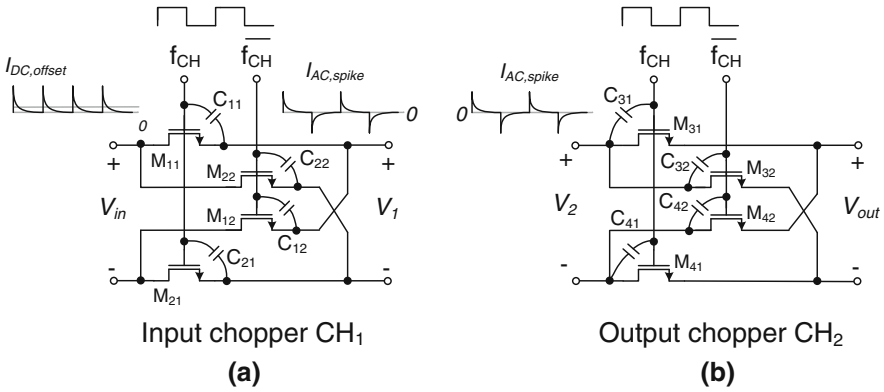

Fig. 2.13 Current spikes caused by imbalanced parasitic capacitances in the input and output choppers CH_1 and CH_2 that give rise to a residue offset

As shown in the input chopper CH_1 (Fig. 2.13a), at the transition moments of the chopper clocks, due to clock feed-through the mismatch between the capacitances C_{11} and C_{12} causes an AC current spike at the node of V_{1+}. For the same reason, the mismatch between C_{21} and C_{22} also leads to another AC current spike at V_{1-}. The difference between these two current spikes results in an AC current spike, as shown in Fig. 2.13a at V_1. This AC current spike is rectified by CH_1, which appears as a DC spike current at the input of CH_1, with an average value given by:

$$I_{offset,DC} = 2(\Delta C_1 - \Delta C_2) \cdot V_{clk} f_{CH} \tag{2.10}$$

where $\Delta C_1 = C_{11} - C_{12}$, and $\Delta C_2 = C_{21} - C_{22}$, V_{clk} is the amplitude of the clock signal, and f_{CH} is the chopper frequency. The DC current spike contributes to the input offset current I_{offset} of the amplifier. This current goes through the series impedance of the chopper and the input signal source, leading to a rectified input voltage spike. The average DC value of the spike results in a residual offset $V_{OS,\ res1}$, as given by:

$$V_{OS,res1} = 2(R_1 + R_2) \cdot (\Delta C_1 - \Delta C_2) \cdot V_{clk} f_{CH} \tag{2.11}$$

where $(R_1 + R_2)$ is the input impedance including on-resistance of the chopper switches and the impedance of the signal source. ΔC_1 and ΔC_2 are the mismatch of clock feed-through capacitances, which is mainly due to the overlap capacitances of the clock line and the source terminals of switches in the input chopper CH_1. If $\Delta C_1 = \Delta C_2$, then no residual offset occurs since it will only result in a common-mode spike.

ΔC_3 and ΔC_4 are the mismatch of clock feed-through capacitances due to the overlap capacitances of the clock lines and the amplifier G_1 output. They will also cause an AC current spike at V_2 (Fig. 2.13b). To provide this AC current spike, the input of G_1 needs to generate an AC voltage spike. This voltage spike is

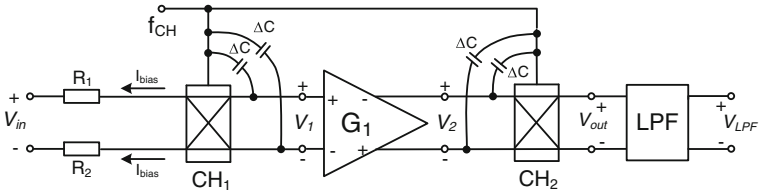

Fig. 2.14 Residual offset due to the bias current and impedance mismatch in a chopper amplifier

demodulated by the input chopper towards the input, resulting in a residual offset $V_{OS,\ res2}$ as given by:

$$V_{OS,res2} = \frac{2(\Delta C_3 - \Delta C_4) V_{clk} f_{CH}}{G_1} \tag{2.12}$$

where $\Delta C_3 = C_{31} - C_{32}$, $\Delta C_4 = C_{41} - C_{42}$, and G_1 is the transconductance of the chopped amplifier. It can be seen that an amplifier with a higher transconductance is less vulnerable to the mismatch of ΔC_3 and ΔC_4. For example, a 10 kHz chopper frequency with $1/G_1 = 5$ kΩ, no source impedance, and a 5 V driving clock voltage would result in a residual offset per unit of capacitance mismatch between ΔC_3 and ΔC_4 of 0.5 μ V/fF. The total residual offset due to clock feed-through is the sum of the offsets given in (2.11) and (2.12).

Thirdly, the *source impedance mismatch* ($\Delta R = R_1 - R_2$) causes another residual offset. The charge injection and clock feed-through due to chopping action cause two s (denoted as I_{bias} in Fig. 2.14) which both flow out of the amplifier's input in the same direction [12]. For bias current calculation, if $\Delta C_1 = \Delta C_2 = \Delta C$ as shown in Fig. 2.14, the average value of the bias current I_{bias} (Fig. 2.14) can be calculated as:

$$I_{bias,DC} = 2\Delta C \cdot V_{clk} \cdot f_{CH} \tag{2.13}$$

The mismatch between input impedances R_1 and R_2 is ΔR, so these two bias currents also generate residual offset, given by:

$$V_{OS,res3} = 2(R_1 - R_2) \cdot \Delta C \cdot V_{clk} \cdot f_{CH} \tag{2.14}$$

If ΔC is 1fF, the chopper frequency f_{CH} is 10 kHz with a 5 V chopper clock, then according to (2.13), the resulting bias current is 0.1 nA. From (2.14), if the mismatch between R_1 and R_2 is 100 kΩ, these two bias currents flow through these two resistors (Fig. 2.14), resulting in an extra residual offset of 10 μV.

It can be seen from (2.11), (2.12) and (2.14) that, the charge injection and clock feed-through of the choppers, cause input bias current, offset current and hence the residual offset. These three errors can be minimized by:

- *Decreasing the chopping frequency*
- *Decreasing the chopper clock amplitude*
- *Balancing or minimizing the overlap capacitors between the clock lines to the input and output terminals of G_1*

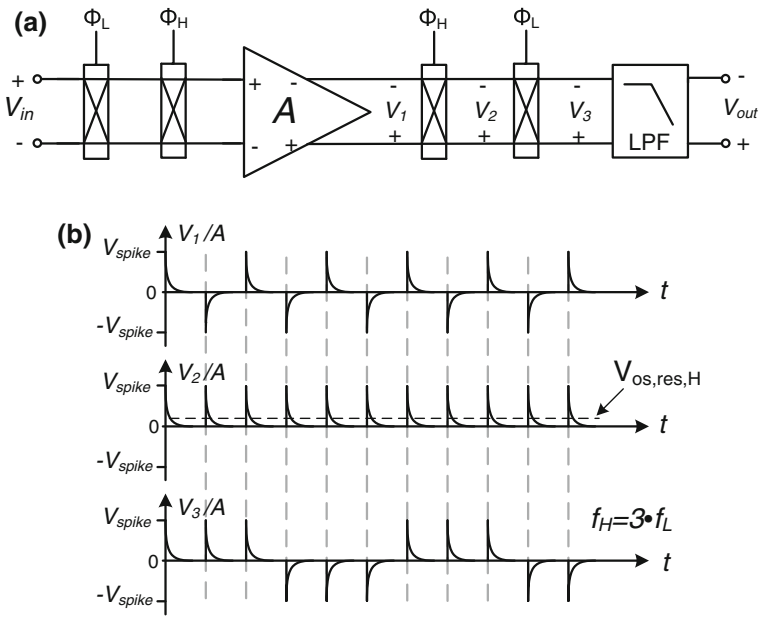

Fig. 2.15 **a** Nested chopper amplifier **b** Charge-injection spikes from the high-frequency choppers are chopped by the low-frequency chopper pair

- *Ensuring matched and balanced input impedance for differential paths reduces residual offset caused by the input bias current*

In Chap. 4, a chopper layout that minimizes the charge injection and clock feed-through will be presented.

2.4.3 Chopper Charge Injection Suppression Techniques

Besides minimizing the charge injection and clock feed-through with the aforementioned methods, there are several techniques that can be used to suppress the demodulated clock feed-through spikes.

Nested-Chopper Technique

Since the residual offset of a chopper amplifier is proportional to the chopper frequency f_{ch}, as expressed by Eqs. (2.11), (2.12) and (2.14), it can be decreased by reducing f_{ch}. However, f_{ch} cannot be lower than the $1/f$ noise corner, otherwise $1/f$ noise can not be completely removed. The nested chopper technique solves this problem by using an extra pair of choppers that run at a much lower frequency. The residual offset of the amplifier chopped by a high frequency chopper clock Φ_H is chopped out by a low-frequency chopper clock Φ_L [13] (Fig. 2.15).

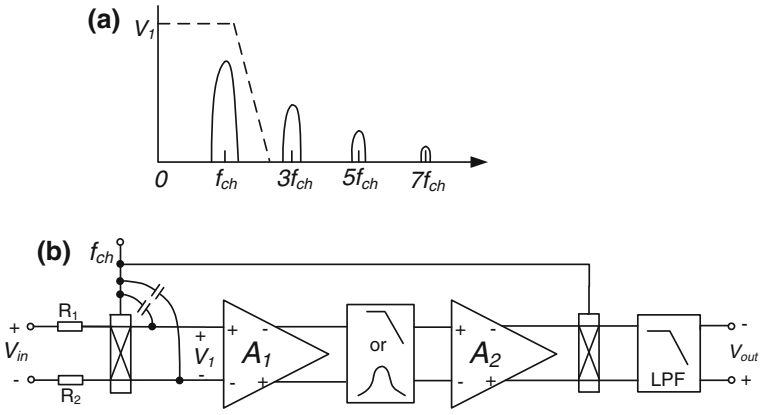

Fig. 2.16 **a** Modulated signal and spike harmonics of V_1 **b** Chopper amplifier with an LP or BP amplifier to remove clock feed-through spikes

The overall residual offset is only limited by the charge injection in the low-frequency chopper, and therefore it is reduced by a factor f_H/f_L, where f_H and f_L are high and low chopping frequencies, respectively.

The implementation of the nested chopper is very simple: only one extra pair of choppers and a low-frequency clock signal are needed. A disadvantage of this approach is that the useable signal bandwidth is reduced, since it is limited by f_L rather than f_H. However, this is not a problem for bridge read-out applications. Nested chopping can be used to chop the complete read-out chain which consists of a preamp and a ΔΣ ADC. The low-frequency chopper spikes at f_L can be filtered out in the decimation filter following the ΔΣ ADC [14]. The nested chopping will be applied to the read-out IC design, as will be discussed in Chap. 5.

Filtering of Spike Harmonics

The chopper clock is a square-wave signal that contains odd harmonics at f_{ch}, $3f_{ch}$, $5f_{ch}$, etc. Most of the energy of the chopper ripple is located at the first harmonics [4]. Therefore, a low-pass (LP) or band-pass (BP) filter can be incorporated between the chopper switches to filter out the chopper harmonics at the high frequencies, at the cost of a small reduction in the signal bandwidth [4] (Fig. 2.16a). A LP filter was implemented in [15] to filter the spikes, achieving a 5 μV offset (Fig. 2.16b). A BP filter implementation is presented in [16] to suppress the DC offset. Here, the chopping frequency is designed to track the center frequency of the BP filter. It achieves an offset of less than 600 nV. However, a disadvantage of this technique is the significant amount of extra circuitry required.

Chopper with Guard Band

Another approach to filter out clock feed-through spikes is to introduce a small guard time in the output chopper switch that prevents the spikes caused by the input chopper from being demodulated, as shown in Fig. 2.17b. This technique has

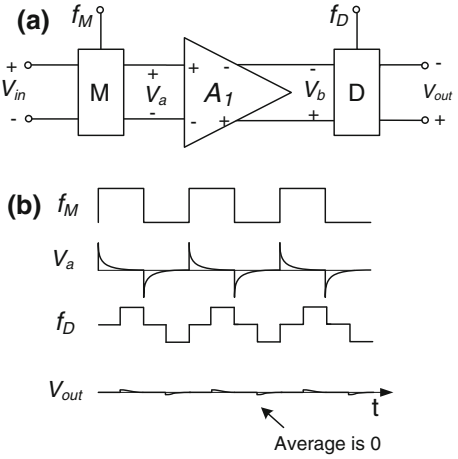

Fig. 2.17 **a** Modulated amplifier **b** Guard band clock diagram

been used in [17–19] for custom sensor interfaces. An average offset of 200 nV has been achieved in [18]. However, the residual offset with the guard band technique is limited by the matching between the shape of the spike and the guard time delay. Moreover, the output signal is no longer continuous-time due to the gap in the guard time since V_{out} just holds the value before the guard time starts, thus incurring a slight loss of gain and noise aliasing.

2.4.4 Conclusions

For the auto-zeroed amplifier, charge injection determines the residual offset. In the chopper amplifier, the residual offset is caused by the non-ideality in clock timing, the demodulated clock feed-through current spikes and the impedance mismatch between two input nodes. *To conclude*, symmetry, matching and balancing the parasitics are essential to achieve low residual offset in chopper amplifier.

2.5 Dynamic Offset Compensated Operational Amplifiers

This section discusses the basic principle of feedback and then reviews several precision operational amplifiers that employ the dynamic offset cancellation techniques discussed above, i.e. auto-zeroing and chopping. These amplifier topologies include ping-pong, offset stabilization and chopper offset stabilization.

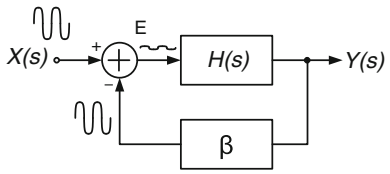

Fig. 2.18 Block diagram of a general feedback system

2.5.1 Feedback

Feedback is a powerful technique that has found wide application in high-precision signal processing. Figure 2.18 shows a negative feedback system, where $H(s)$ and β denote the high gain amplifier and the passive feedback network, respectively. Part of the output signal is redirected back to the input and compared to the incoming signal. The loop accurately controls the output to produce an amplified or processed replica of the input signal.

The error, which is indicated as E in Fig. 2.18, is given by:

$$E(s) = X(s) - \beta Y(s) = X(s)\frac{1}{1 + \beta H(s)} \tag{2.15}$$

From (2.15), the higher the loop gain $\beta H(s)$, the more effectively the error E is minimized. This means that a feedback loop with high loop gain can be applied to reduce an error.

This feedback concept will be used in the work presented in Chaps. 4 and 5 to reduce the offset and gain error of an amplifier. Generally, the feedback concept is used in operational amplifiers to obtain an accurate gain determined by $1/\beta$. The next few sections will review several precision operational amplifier topologies.

2.5.2 Ping-Pong Operational Amplifier

As discussed before, the auto-zeroing technique is not directly suitable for use in a continuous-time general purpose amplifier, since the amplified output signal is only available during one half of the clock period. To obtain a continuous-time output signal, the ping-pong technique can be used. This involves the use of two auto-zeroed amplifiers [6], as shown in Fig. 2.19. When one amplifier is being auto-zeroed, the other is being used to amplify the signal. The same output stage is shared by the two auto-zeroed amplifiers. Furthermore, the combination of auto-zeroing and chopping is employed to achieve a noise PSD of 20 nV/$\sqrt{}$Hz from DC to 1.5 kHz, which rises to 48 nV/$\sqrt{}$Hz at 20 kHz. It consumes a supply current of 800 μA.

Figure 2.20 shows the noise spectrum of chopping, auto-zeroing and the combination of these two. As seen from Fig. 2.20b, chopping modulates low-frequency $1/f$ noise to the chopping frequency, thus achieving a clean and flat noise

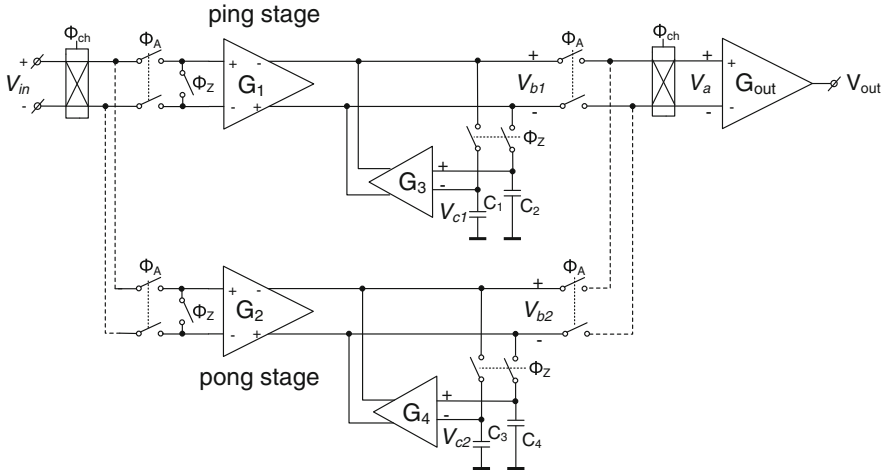

Fig. 2.19 Basic concept of the ping-pong operational amplifier

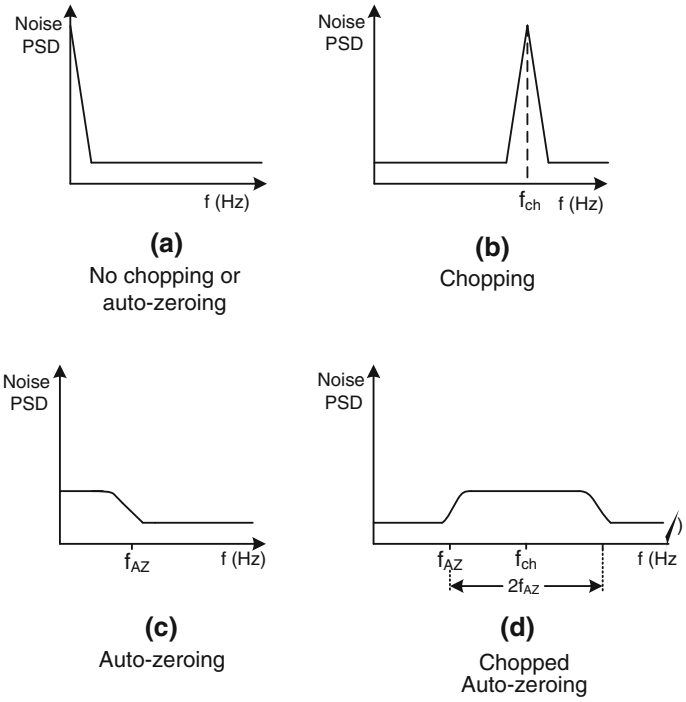

Fig. 2.20 Input-referred noise PSD of chopping, auto-zeroing and the combination of the two ($f_{ch} = 2f_{AZ}$)

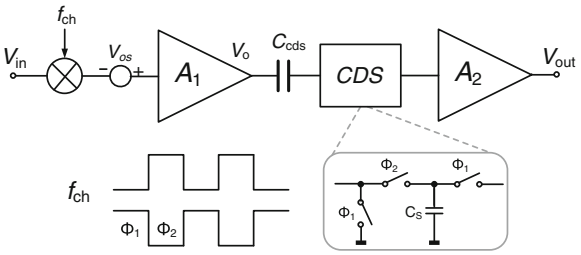

Fig. 2.21 Simplified chopper-CDS block diagram

spectrum at low frequencies, but with ripple at the chopping frequency. Auto-zeroing involves sampling, thus causing increased noise at DC due to aliasing (Fig. 2.20c). In their combination, since the input stage is chopped at twice the auto-zeroing frequency, this noise is then modulated away from DC to f_{ch} (or $2f_{AZ}$) [6] (Fig. 2.20d).

A disadvantage of the ping-pong technique is that spikes are introduced because the voltages V_{b1} and V_{b2} at the output of the first stage amplifiers have to switch between the offset compensating voltages V_{c1}, V_{c2} and the voltage required at the input of the output amplifier V_a. This results in spikes at the output. This effect can be reduced by replacing C_1-C_4 with active integrators with the same input CM voltage as the output stage G_{out} [1]. However, spikes still remain because switching occurs within the signal path.

2.5.3 Chopper-CDS Operational Amplifier

As a hybrid of chopping and auto-zeroing, a ripple-free operational amplifier is proposed in [20] that uses input chopping and correlated double sampling (CDS) for demodulation. As shown in Fig. 2.21, the AC-coupling capacitor C_{cds} is inserted between the first and the second stage, removing the offset from the first stage without causing ripple. The CDS then demodulates the signal back to DC.

Since CDS operates on the modulated input signal, the folded noise spectrum due to sampling is also around the f_{CDS}, which is equal to the chopping frequency. This implies that the gain of A_1 around the chopping frequency f_{ch} should be large since it suppresses the folded noise of CDS. The DC gain of A_1 should be low enough so that the amplified offset and $1/f$ noises do not saturate A_1. A_1 is implemented with a band-pass response that exhibits low gain around DC but high gain at f_{ch}. In the worst case, the amplified offset can still be too large. A band-reject passive feedback network is used that decreases the gain at low and high frequencies, but not at the chopping frequency. In this way, the DC gain of A_1 is reduced further. However, this scheme increases the circuit complexity. It achieves a 2 μV offset and a noise PSD of $37\text{nV}/\sqrt{\text{Hz}}$ with an NEF of 5.5.

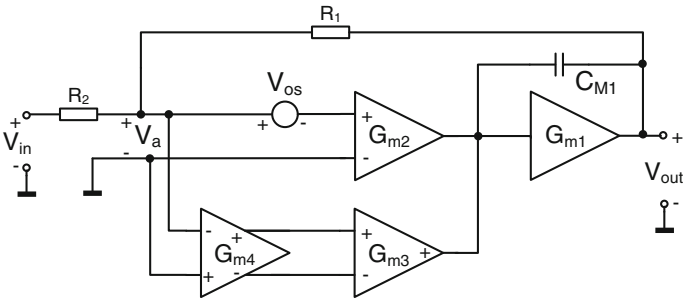

Fig. 2.22 The concept of the offset-stabilized operational amplifier

2.5.4 Offset-Stabilized Operational Amplifiers

Offset stabilization is another technique that can be used to design a precision wideband amplifier. The basic concept of offset-stabilization is shown in Fig. 2.22. A main operational amplifier G_{m2} with an offset V_{os}, is being offset-stabilized by a stabilizing amplifier G_{m4} with a hypothetical zero offset. G_{m3} acts as an auxiliary input of the main amplifier. The stabilizing amplifier G_{m4} applies a voltage to the inputs of G_{m3}, which drives a current to the output of G_{m2} to compensate for its input offset voltage [4]. The feedback resistors R_1 and R_2 determine the gain of the amplifier.

With the negative feedback configuration, the differential input voltage V_a of G_{m2} is approximately equal to the offset V_{os}. The residual offset due to the finite gain of the combined amplifier can then be expressed as:

$$V_{os,res} \approx \frac{A_{m2}}{A_{m4}A_{m3}} V_{os} \tag{2.16}$$

where A_{m4}, A_{m3} and A_{m2} are the DC voltage gains of the stabilizing amplifier G_{m4}, the main amplifier G_{m3}, and the auxiliary input of the main amplifier G_{m2}, respectively. Equation (2.16) indicates that the combined voltage gain of G_{m4} and G_{m3} has to be much larger than the voltage gain of the main amplifier G_{m2}. If G_{m3} is 50 times lower than G_{m2}, then to reduce a 10 mV worse-case offset to 1 μV, G_{m4} must have a minimum voltage gain of 114 dB. To maintain stability, frequency compensation must also be implemented.

This topology can also be seen as a multi-path amplifier in which the cascode of G_{m4}, G_{m3} and G_{m1} form the high-gain low-frequency path, and the main amplifier G_{m2} and G_{m1} form the low-gain high-frequency path. Low-frequency characteristics will, therefore, be determined by the low frequency path. In other words, the low-frequency noise, residual offset and gain accuracy are determined by G_{m4}, while the unity gain frequency is determined by the main amplifier G_{m2}. To achieve μV-level offset, the offset-stabilization loop needs to be chopped or auto-

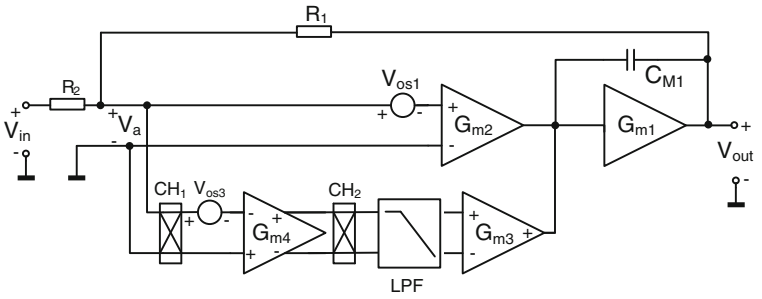

Fig. 2.23 Chopper offset-stabilized amplifier

zeroed. Chopping is more power-efficient than auto-zeroing, therefore chopper offset-stabilized amplifiers will be discussed in the next section.

2.5.5 Chopper Offset-Stabilized Operational Amplifiers

Figure 2.23 shows a chopper offset-stabilized amplifier. Since G_{m4} determines the low-frequency noise and offset of the overall amplifier, G_{m4} is chopped to eliminate its $1/f$ noise and offset. The chopper amplifier composed of chopper CH_1, stabilizing amplifier G_{m4}, and chopper CH_2 senses the offset of the main amplifier G_{m2}. A LPF suppresses the chopper ripple due to the chopped offset of G_{m4}. The residual offset due to finite gain is expressed by (2.16).

The effects of chopping on the noise of chopper offset-stabilized amplifier are depicted in Fig. 2.24. The offset and $1/f$ noise of G_{m4} are modulated to the chopping frequency f_{ch}, and then removed by the LPF. For effective suppression of $1/f$ noise, the bandwidth of the stabilizing loop as well as the chopper frequency f_{ch} should, therefore, be larger than the $1/f$ noise corner frequency of the main amplifier. To let the low-frequency noise be dominated by the low-frequency path, the –3 dB frequency of the LPF should be chosen higher than the $1/f$ corner frequency of the main amplifier G_{m2}, and the chopper frequency should be high enough and thus the chopper ripple can be filtered out properly.

The LPF that filters out the chopper ripple (Fig. 2.23) can be implemented in several ways, e.g. a continuous-time integrator, a sample-and-hold notch filter, or a continuous-time notch filter, which will be described as follows.

2.5.5.1 Continuous-Time Integrator

One way to implement the LPF is by using the integrator composed of G_{m5}, C_{51} and C_{52} to filter out the chopper ripple [21], as shown in Fig. 2.25. It depicts a

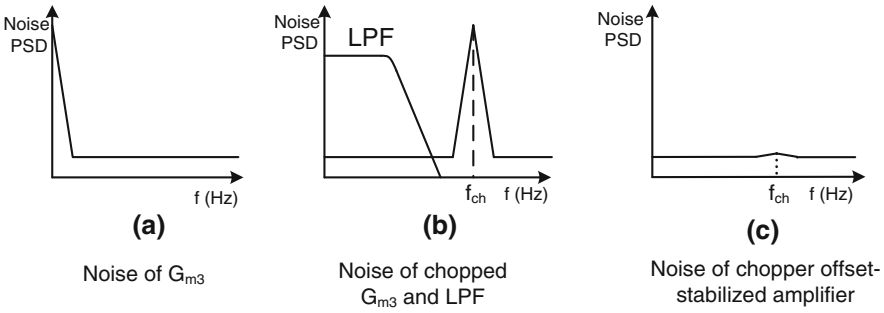

Fig. 2.24 Noise in chopper-stabilized amplifiers

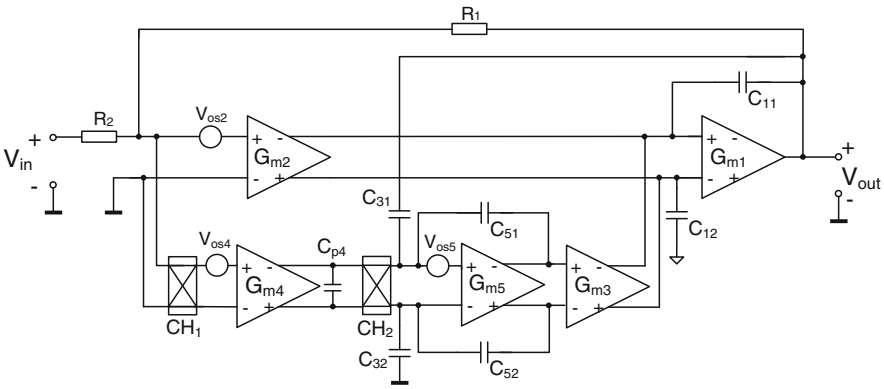

Fig. 2.25 Chopper offset-stabilization amplifier using an active integrator and multi-path hybrid-nested Miller compensation

multi-path architecture that employs this technique in combination with hybrid Miller compensation [22, 23]. The gain stages G_{m2} and G_{m1} form the high-frequency low-gain path, while the transconductances G_{m4}, G_{m5}, G_{m3} and G_{m1} form the high-gain low-frequency path. To realize a frequency response with a smooth roll-off, the unity gain frequency of both paths should be [23].

$$f_{0dB} = \frac{G_{m4}}{2\pi C_3} = \frac{G_{m2}}{2\pi C_1} \tag{2.17}$$

where C_3 and C_1 are the values of capacitors C_{31} (or C_{32}) and C_{11} (or C_{12}), respectively.

The modulated offset V_{os4} of G_{m4} is filtered by the integrator consisting of G_{m5}, C_{51} and C_{52}. However, the integrator needs very large capacitors to obtain a low cut-off frequency. Hence in reality, a residual chopper ripple in the form of a triangular wave appears at the integrator output. Furthermore, due to the action of the chopper CH_2, the offset of G_{m5} (V_{os5}) appears as a square-wave voltage over the capacitor C_{p4}, charging and discharging this capacitor. The resulting

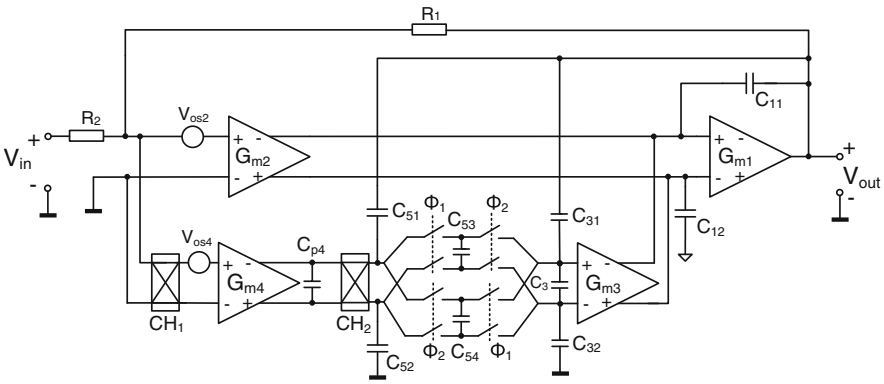

Fig. 2.26 Multi-path operational amplifier with an embedded sample-and-hold circuit

alternating current at the output of G_{m4} is demodulated by chopper CH_1, causing a residual offset.

To eliminate this residual offset, the parasitic capacitor C_{p4}, or the offset V_{os5} of the integrator, must be minimized. The parasitic capacitor C_{p4} can be minimized by choosing small dimensions for the transistors that are connected to the output terminals of G_{m4}. Furthermore, C_{p4} can be minimized to ensure a fully symmetric and balanced layout. To reduce offset V_{os5}, auto-zeroing can be used [21]. However, it increases the complexity and power consumption of the design. Since the focus of this thesis is to design a low- noise amplifier with good noise-power efficiency, the topology with G_{m5} auto-zeroed will not be elaborated further.

2.5.5.2 Sample-and-Hold Notch Filter

An alternative solution for implementing the LPF in Fig. 2.23 are to use a switched-capacitor (SC) sample-and-hold circuit to sample the chopper ripple at the output of the integrator, as shown in Fig. 2.26. It shows an operational amplifier with multi-path hybrid-nested Miller compensation. A LPF is implemented with a SC notch filter consisting of the switches driven by Φ_1 and Φ_2 and the capacitors C_{53} and C_{54} [24]. The switches sample the chopper ripple at the zero-crossing points. The notch positions of the Sinc filter are located at multiples of the chopper frequency, and thus are accurately determined by the chopping clock.

This notch filter acts as a passive integrator. To compensate for the extra pole introduced by the notch filter, the capacitors C_{51} and C_{52} are introduced for the same reason as the hybrid-nested Miller compensation [23]. Capacitors C_{31} and C_{32} are theoretically not needed, but they help to maintain local loop stability. The capacitor C_3 helps to limit the bandwidth of the low-frequency path so that the delay caused by the notch filter does not cause instability [24].

However, this technique still involves sampling, and so still incurs a certain noise-folding. More importantly, the sample-and-hold filter exhibits a Sinc

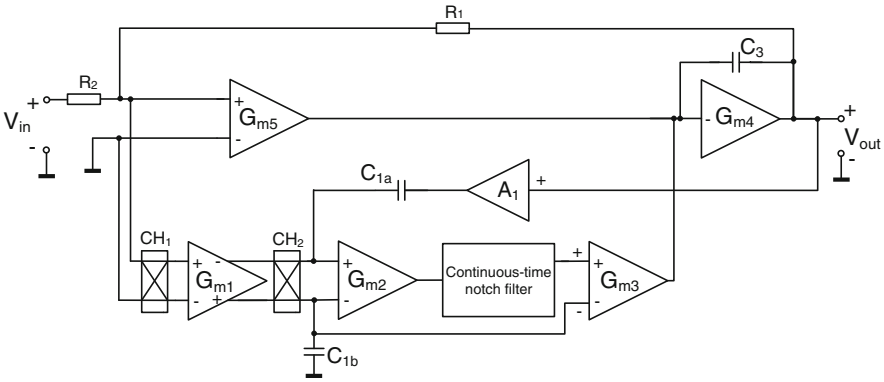

Fig. 2.27 Multi-path operational amplifier with an embedded continuous-time notch filter

filtering response, creating a significant phase shift at the chopping frequency. Overcoming these phase shift complicates the frequency compensation in the amplifier.

2.5.5.3 Continuous-Time Notch Filter

As a counterpart of SC implementation, the notch filter also can be implemented in a continuous-time (CT) fashion. Figure 2.27 shows a CT notch filter incorporated in the low-frequency path to filter out the chopper ripple [25] in a multi-path operational amplifier. Additionally, a buffer A_1 is used to allow feedback through a compensation capacitor C_{1a} for the low-frequency path, thus preventing the chopper ripple at the output of CH_2 from feeding forward through C_{1a} to the output of the amplifier.

The disadvantage of this approach is that the notch filter suppresses the ripple in an open-loop structure. This implies that the chopping frequency derived from the time constant of the on-chip relaxation oscillator needs to be well-matched to the notch position of the CT filter, which is also determined by the product of certain resistors and capacitors. This frequency tracking is not an issue for the SC notch filter [24], since the notch positions are precisely determined by the chopping clock. Furthermore, if a tunable chopping frequency is desired, a phase-locked loop (PLL) is then required to track the external chopping frequency to ensure that the RC time constant of the CT notch filter closely tracks the locking frequency. Otherwise, trimming is required to tune the notch location in the CT notch filter.

2.5.5.4 Auto-Correction Feedback Loop

Another way to suppress the chopper ripple is to use an auto-correction feedback (ACFB) loop to null the offset in a chopper multi-path operational amplifier [26, 27].

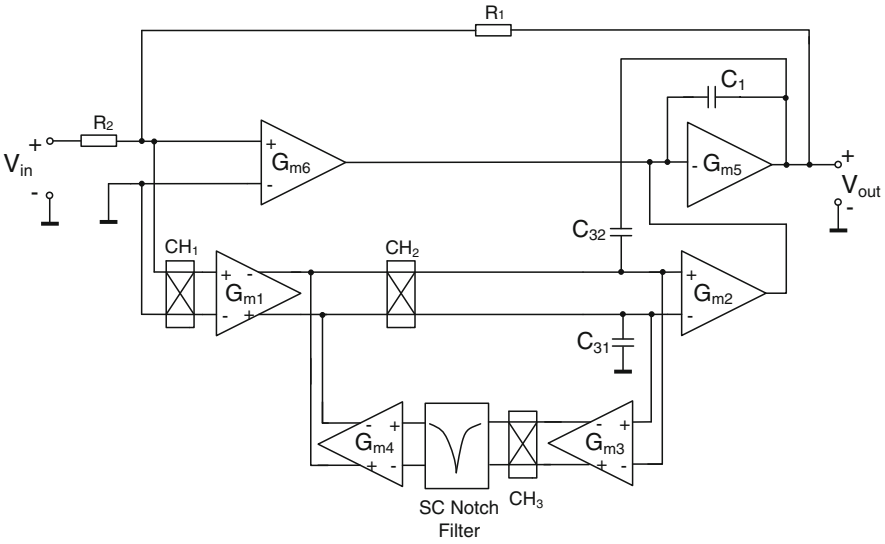

Fig. 2.28 Multi-path operational amplifier with an auto-correction feedback loop

Its block diagram is shown in Fig. 2.28. Unlike the designs presented in [24, 25] which employ notch filters in the signal path to suppress the chopper ripple, this approach uses a feedback loop outside the signal path. Therefore, it does not cause any phase shift in the signal path. However, the stability of the feedback loop itself needs to be taken care of. This is because the notch filter creates a significant phase shift at the chopping frequency, and the unity gain frequency of the ACFB loop must occur well below the chopping frequency to ensure the loop stability. Increasing the unity-gain frequency speeds up the settling of the loop. However, a higher chopping frequency is then required, thus increasing the charge injection and the offset.

Moreover, since the sensing points of the loop are the virtual ground of G_{m2}, they are relatively "quiet". The DC gain of the loop is limited because of the small ripple excitation. A ripple reduction of only 43 dB [26] is achieved. Furthermore, the SC notch filter (NF) causes sampling noise at DC. This noise is modulated by CH_2 and creates a peak output noise PSD around the chopping frequency.

2.6 Conclusions

Table 2.2 summarizes the performances of precision operational amplifiers that achieve μV-level offset. They apply different techniques to suppress chopper ripple. One technique is to use auto-zeroing to reduce the initial offset of the amplifier [6, 21]. However, the increased low-frequency noise due to noise folding leads to a noise penalty, i.e. extra power dissipation is needed to meet a given noise specification (NEF = 21.8 and 153). A band-pass filter can be implemented between the choppers to suppress the DC offset, so as to eliminate the output

Table 2.2 Comparison of precision operational amplifiers

	Tang [6]	Witte [21]	Burt [24]	Kusuda [27]	Belloni [20]
Year	2002	2006	2006	2011	2010
Noise PSD (nV/$\sqrt{}$Hz)	20	15	55	5.9	37
Chopping frequency (kHz)	15	32	125	200	500
Offset (μV)	3	1.5	3	0.78	1.94
Input bias current (pA)	40	–	70	72	–
GBW (kHz)	2500	1370	350	4000	260
Supply current (Iq)(μA)	800	700	17	1470	14.4
Die area(mm^2)	0.67	3.6	0.7	1.26	1.14
NEF [28]	21.8	153	8.7	8.7	5.5
GBW/Iq (kHz/μA)	3.1	2	20.6	2.7	18
Rail sensing capability	No	Yes	Yes	Yes	Yes
Ripple reduction technique	Auto-zeroing	Auto-zeroed integrator	SC notch filter	Auto feedback loop	Chopper-CDS

chopper ripple [16]. However, the chopping frequency needs to track the center frequency of the band-pass filter, which requires significant amount of extra circuitry.

A switched-capacitor [24] or a continuous-time notch filter [25] can be embedded in a multi-path offset stabilized operational amplifier to reduce the chopper ripple. However, the SC notch filter [24] involves sampling thus causing noise folding. The issue associated with the CT notch filter [25] is that the notch filter suppresses the ripple in an open-loop structure. To effectively suppress the chopper ripple, the notch frequency of the CT filter needs to closely track the chopping frequency, which could be limited by the RC spread in the CT notch filter. Another technique uses an auto-correction feedback loop [26] to suppress the chopper ripple. However, since the ripple sensing points are at the "quiet" virtual grounds of the output stage, the limited loop gain restricts the ripple suppression ratio.

In addition, the notch filters generate excess phase shift, meaning that the chopper clock frequency must be relatively high (> 125 kHz) to maintain stability in the signal path [24, 25] or in the feedback loop [26]. Such a high chopping frequency increases charge injection errors, and hence increases input offset, given the same noise level and process parameters. The chopper-CDS scheme [20] uses an AC-coupled capacitor to block the offset, thus generating no chopper ripple. However, this technique also necessitates a high chopping frequency of 500 kHz, resulting in a relatively low input impedance and a high input bias current.

Therefore, innovative solutions need to be explored to eliminate the chopper ripple without causing the above-mentioned issues: noise aliasing, frequency tracking, limited loop gain, and excess phase shift (high chopping frequencies). To counteract these problems, a new ripple reduction technique will be proposed in Chap. 4.

References

1. Witte JF (2008) Dynamic offset compensated CMOS amplifiers. Ph.D. Thesis, Delft University of Technology, The Netherlands
2. Razavi B (2001) Design of analog CMOS integrated circuits. McGraw-Hill Companies, Inc., New York
3. Sansen WMC (2006) Analog design essentials. Springer, Dordrecht
4. Enz CC, Temes GC (1996) Circuit techniques for reducing the effects of op-amp imperfections: auto-zeroing, correlated double sampling, and chopper stabilization. Proc. IEEE 84(11):1584–1614
5. Poujois R, Borel J (1978) A low drift fully integrated MOSFET operational amplifier. IEEE J Solid-State Circuits 13:499–503
6. Tang ATK (2002) A 3 μV-offset operational amplifier with 20nV/$\sqrt{}$Hz input noise PSD at DC employing both chopping and auto-zeroing. In Proceedings of the IEEE ISSCC, Dig. Tech. Papers, pp 386–387
7. Enz CC (1989) High precision CMOS micropower amplifiers. Ph.D. Thesis, Thesis no. 802, Ecole Polytechnique Federale de Lausanne (EPFL). Available at: http://library.epfl.ch/en/theses/?nr=802,1989
8. Pertijs MAP, Kindt WJ (2009) A 140 dB-CMRR current-feedback instrumentation amplifier employing ping-pong auto-zeroing and chopping. In Proceedings of the IEEE ISSCC, Dig. Tech. Papers, pp 324–325
9. Pertijs MAP, Kindt WJ (2010) A 140 dB-CMRR current-feedback instrumentation amplifier employing ping-pong auto-zeroing and chopping. IEEE J Solid-State Circuits 45(10): 2044–2056
10. Wegmann G, Vittoz EA, Rahali F (1987) Charge injection in analog MOS switches. IEEE J Solid-State Circuits, SC-22(6):1091–1097
11. Witte JF, Makinwa KAA, Huijsing JH (2004) The effect of non-idealities in CMOS chopper amplifiers. In Proceedings of the ProRISC 2004, pp 616–619
12. Fan Q, Huijsing JH, Makinwa KAA (2011) Analysis of input impedance, input bias and offset current of a chopped multi-path current feedback instrumentation amplifier. In Proceedings of the IWASI, pp 61−66
13. Bakker A, Thiele K, Huijsing JH (2000) A CMOS nested-chopper instrumentation amplifier with 100-nV offset. IEEE J Solid-State Circuits 35(12):1877–1883
14. McCartney D, Sherry A, Sherry et al (1997) A low-noise low-drift transducer ADC. IEEE J Solid-State Circuits 32(7):959–967
15. Enz CC, Vittoz EA, Krummenacher F (1987) A CMOS chopper amplifier. IEEE J Solid-State Circuits, SC-22(3):335–342
16. Menolfi C, Huang Q (1999) A fully integrated, untrimmed CMOS instrumentation amplifier with submicrovolt offset. IEEE J Solid-State Circuits 34(3):415–420
17. Bilotti A, Monreal G (1999) Chopper-stabilized amplifier with a track-and-hold signal demodulator. IEEE Trans Circuits Syst I:490–495
18. Huang Q, Menolfi C (2001) A 200nV offset 6.5nV/$\sqrt{}$Hz noise PSD 5.6 kHz chopper instrumentation amplifier in 1 μm digital CMOS. In Proceedings of the IEEE ISSCC, Dig. Tech. Papers, pp 362–363
19. van der Meer JC, Riedijk FR, van Kampen E, Makinwa KAA, Huijsing JH (2005) A fully integrated CMOS hall sensor with a 3.65 μT 3σ offset for compass applications. In Proceedings of the IEEE ISSCC, Digital technical papers, pp 246–247
20. Belloni M, Bonizzoni E et al (2010) A micropower chopper-CDS operational amplifier. IEEE J Solid-State Circuits 45(12):2521–2529
21. Witte JF, Makinwa KA, Huijsing JH (2007) A CMOS chopper offset-stabilized opamp. IEEE J Solid-State Circuits 42(7):1529–1535
22. Huijsing JH, Fonderie MJ, Shahi B (2007) Frequency stabilization of chopper-stabilized amplifiers. United States Patent Nr. 7,209,000, Apr. 2007

23. Huijsing JH (2011) Operational amplifiers theory and design, 2nd Edition, Springer, Berlin
24. Burt R, Zhang J (2006) A micropower chopper-stabilized operational amplifier using a SC notch filter with synchronous integration inside the continuous-time signal path. IEEE J. Solid-State Circuits 41(12):2729–2736
25. Luff GF (2010) Chopper stabilized amplifier. United States Patent, US 7724080:B2, May 2010
26. Kusuda Y (2010) Auto correction feedback for ripple suppression in a chopper amplifier. IEEE J Solid-State Circuits 45(8):1436–1445
27. Kusuda Y (2011) A 5.9nV/$\sqrt{}$Hz chopper operational amplifier with 0.78 μV maximum offset and 28.3nV/°C offset drift. In Proceedings of the IEEE ISSCC, Dig. Tech. Papers, pp 242–243
28. Steyaert MSJ, Sansen WMC, Chang Z (1987) A micro power low-noise monolithic instrumentation amplifier for medical purposes. IEEE J Solid-State Circ SC-22(6):1163–1168