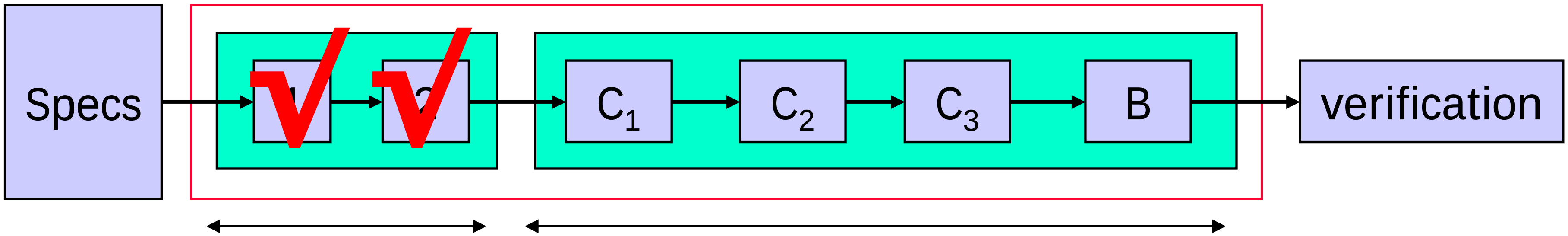
Structured Electronic Design

Building the nullor: Noise

What we did so far



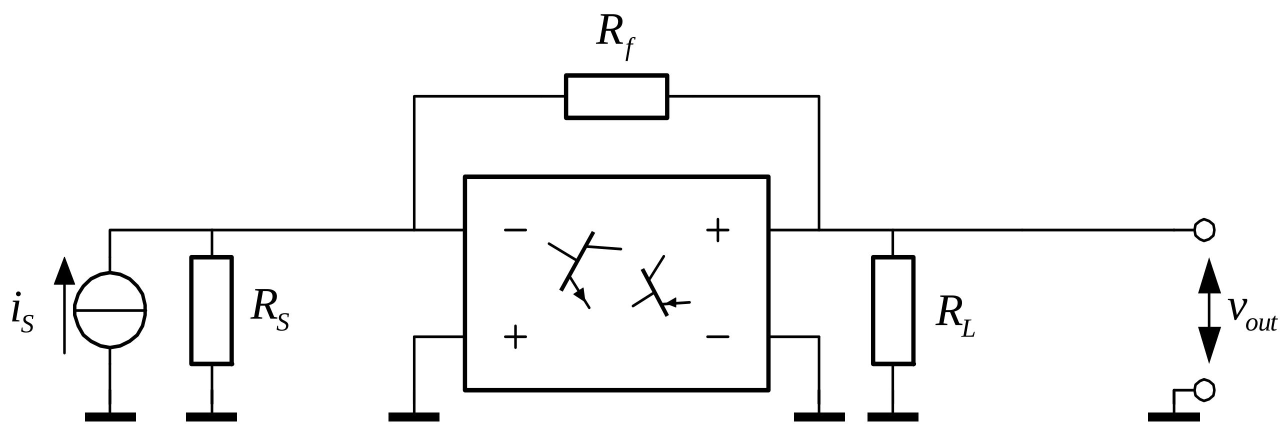
Known:

Nullor design

- Topology
- Best nullor implementation
- Voltage and current swing
- Power consumption
- Noise level

$$A_t = \boxed{A_{t\infty}} \frac{-L}{1-L}$$

The nullor becomes a circuit



$$C = B\ {}^{2}\log\frac{S+N}{N}$$

bandwidth – noise – distortion

bandwidth – distortion - noise

noise - bandwidth – distortion

noise – distortion - bandwidth

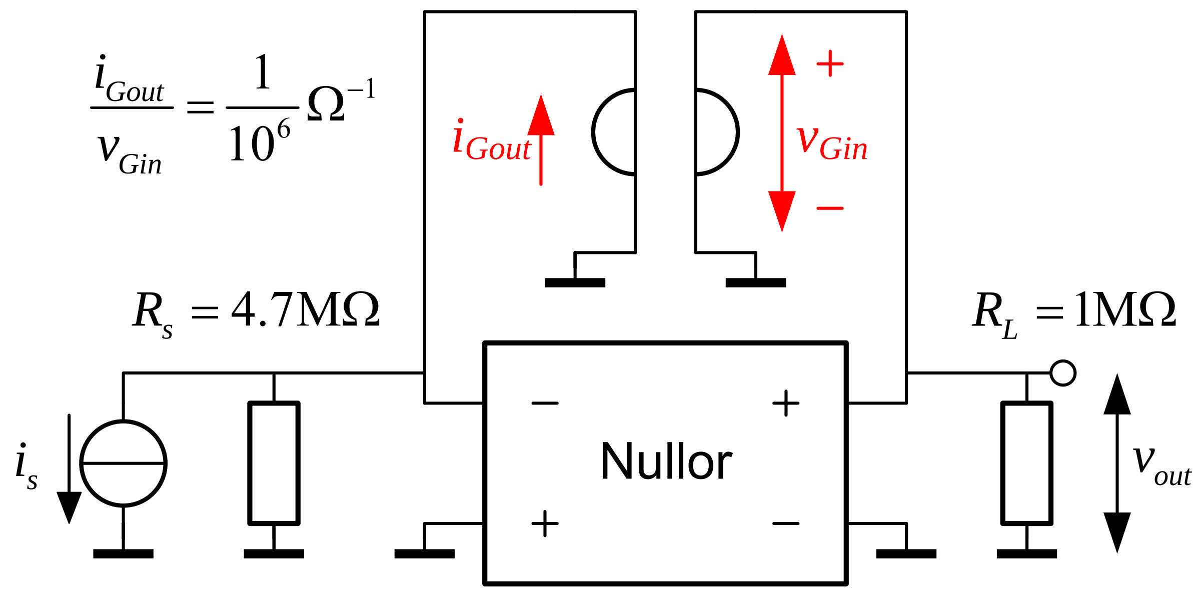
distortion - noise – bandwidth

distortion – bandwidth - noise

Trans-impedance amplifier

- Source
  - Current
  - Amplitude 1mA
  - $R_S = 4.7\text{M}\Omega$
- Load
  - Voltage
  - $R_L = 1\ \text{M}\ \Omega$
- Transfer
  - $\dfrac{v_{out}}{i_s} = 1\text{M}\Omega$
  - ……..

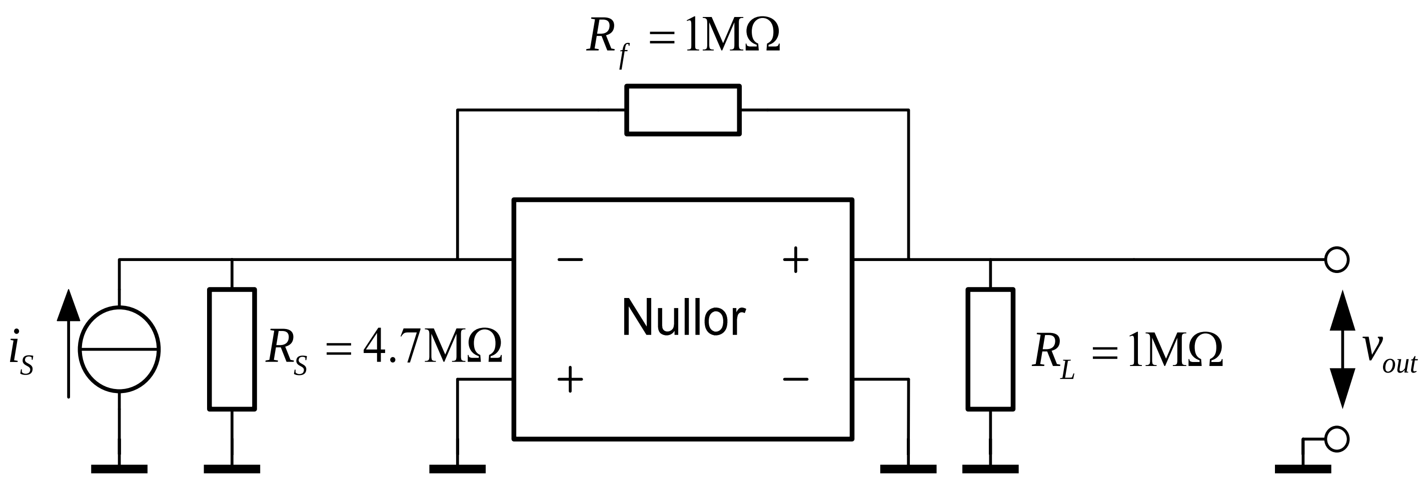
$$\frac{i_{Gout}}{v_{Gin}} = \frac{1}{10^6}\Omega^{-1}$$



Noise measured at the **output**:

$$S_{out} = \frac{4kT}{4.7M}10^{12} \Rightarrow 60\frac{\text{nV}}{\sqrt{\text{Hz}}}$$

Trans-impedance amplifier



Noise measured at the **output**:

$$S_{out} = \frac{4\text{kT}}{4.7\text{M}} 10^{12} \Rightarrow 60 \frac{\text{nV}}{\sqrt{\text{Hz}}}$$

$$S_{out} = \frac{4\text{kT}}{4.7\text{M}} 10^{12} + \frac{4\text{kT}}{1\text{M}} 10^{12} \Rightarrow 144 \frac{\text{nV}}{\sqrt{\text{Hz}}}$$

- Noise: 144 $\text{nV}/\sqrt{\text{Hz}}$
- Infinite bandwidth
- No distortion

Sequence ?

bandwidth – noise – distortion

bandwidth – distortion - noise

noise - bandwidth – distortion

noise – distortion - bandwidth

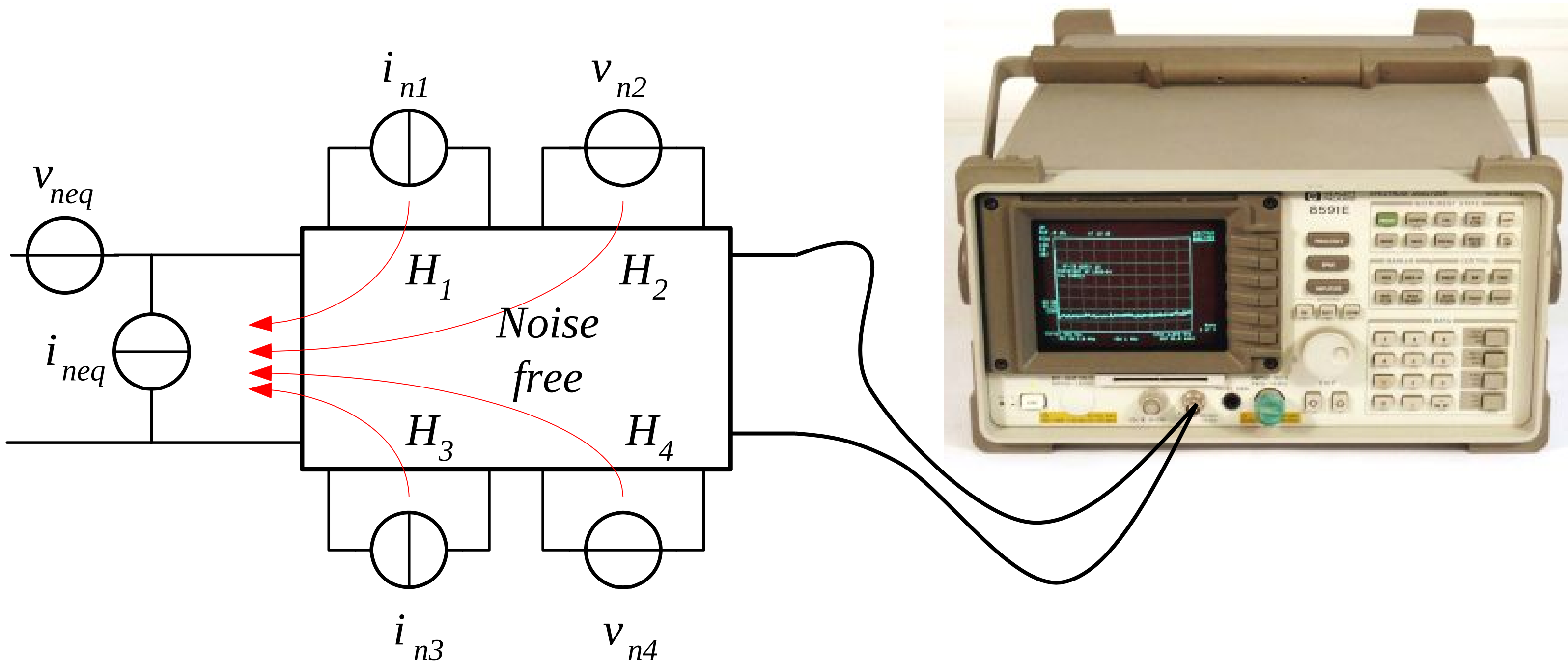
distortion - noise – bandwidth

distortion – bandwidth - noise

- Noise: 144 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$
- Infinite bandwidth
- No distortion

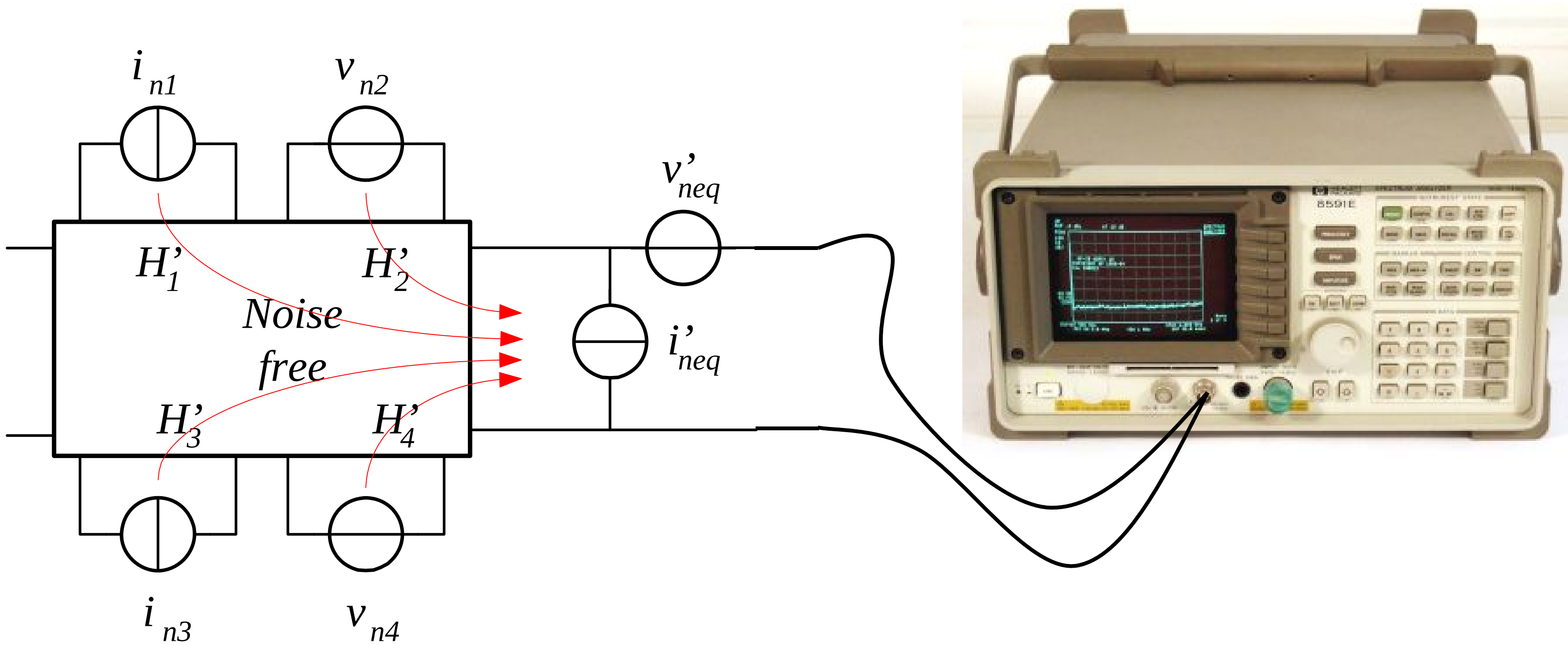
Noise behavior can be analyzed in the presence of a nullor

Modeling the noise of the active circuit



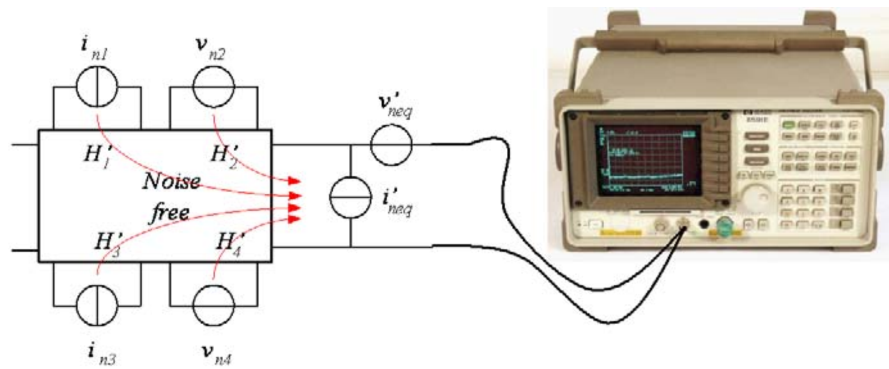
Equivalent sources at the input

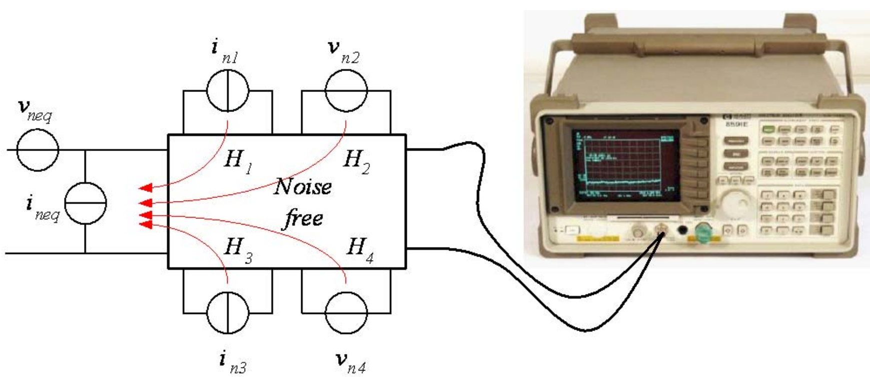
Modeling the noise of the active circuit



Equivalent sources at the output

Equivalent sources at the output

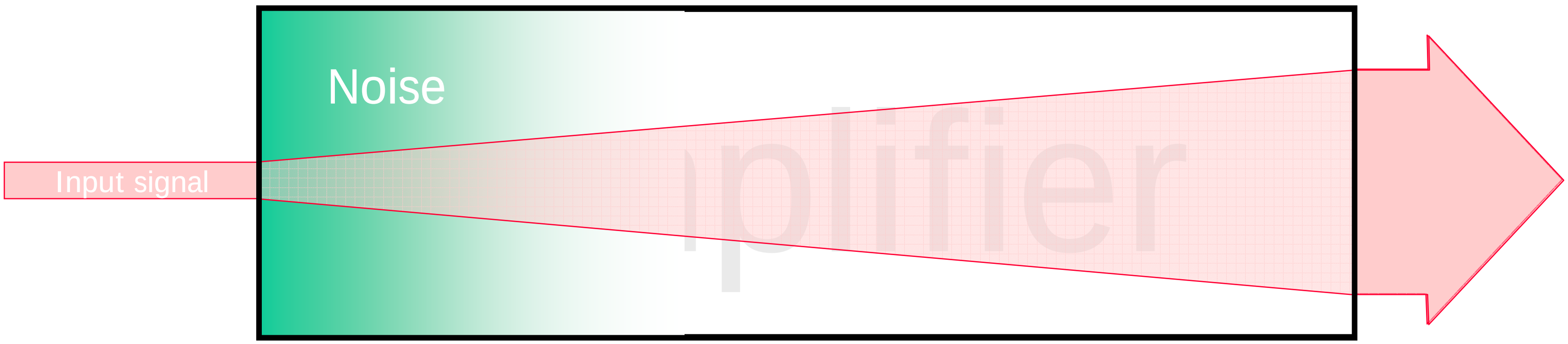




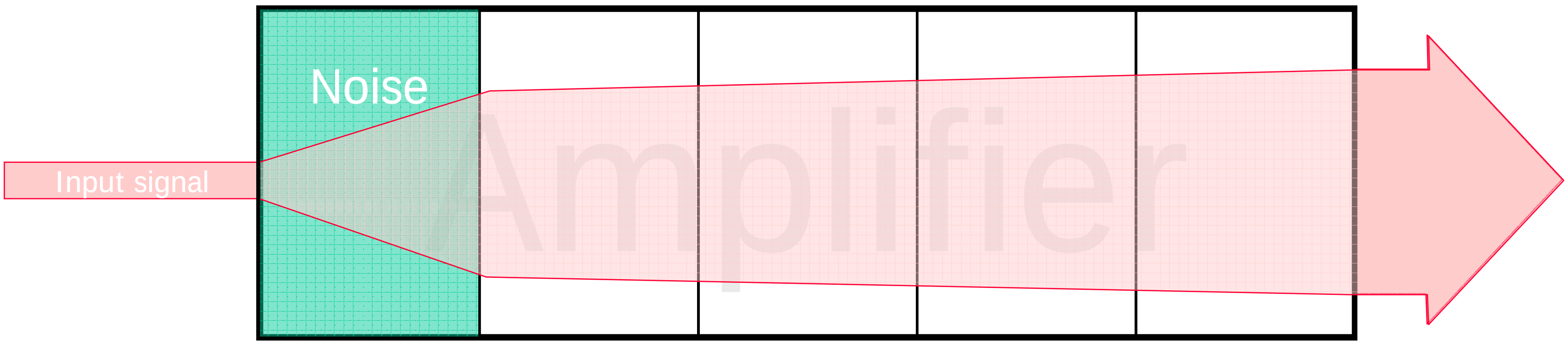
Calculated at

- input
  - easily compared to source
- output
  - can be measured

Noise optimization and Orthogonality

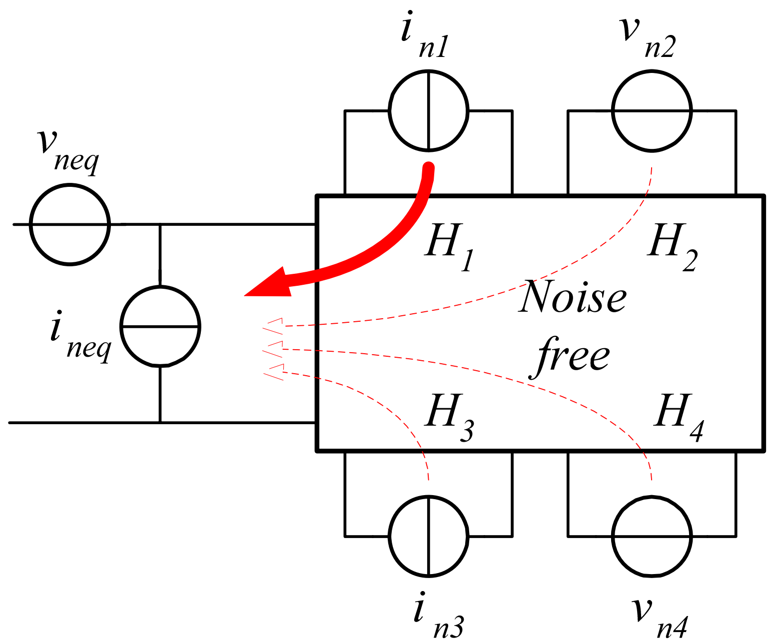


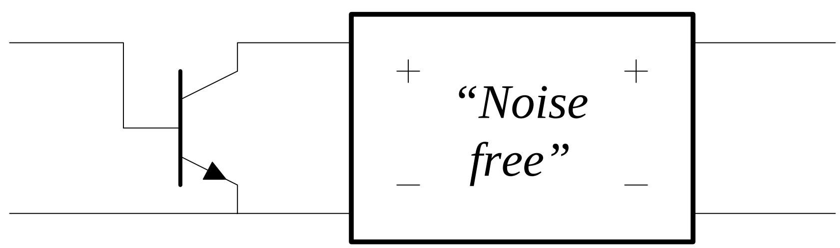
Orthogonality by design



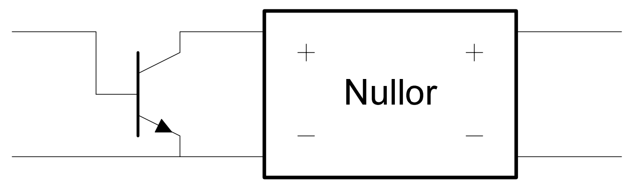
IF the first stage has a large gain,
then the noise contribution of the following stages is negligible

IF the first stage has a large gain...





Orthogonal noise design is possible



When optimizing bandwidth:
- No non-linearity
- No noise

When optimizing noise behavior:
- ☺ No non-linearity
- ☺ No bandwidth details

Noise behavior can be analyzed in the presence of a nullor

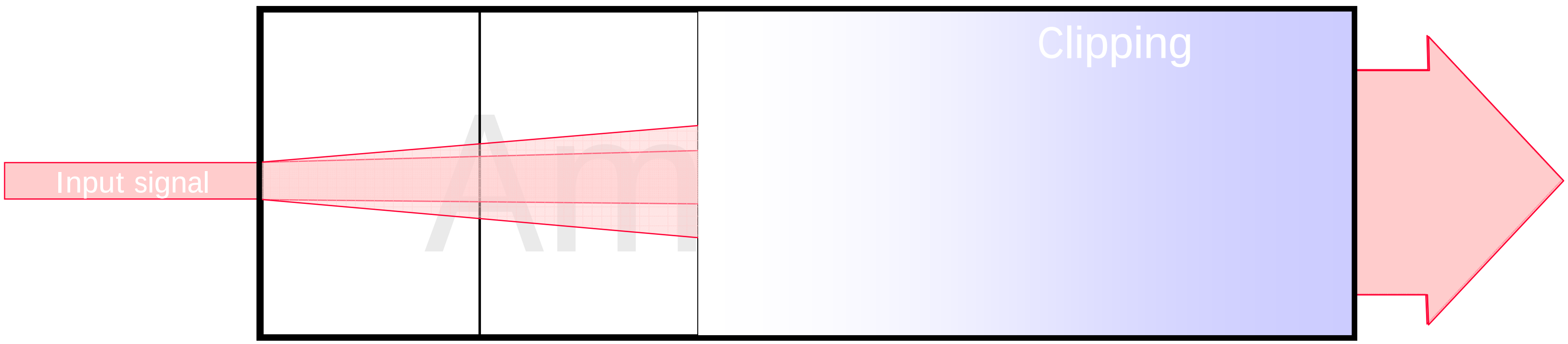
When optimizing non-linear behavior (distortion):
- No dynamic (bandwidth) effects
- No noise

EXAM

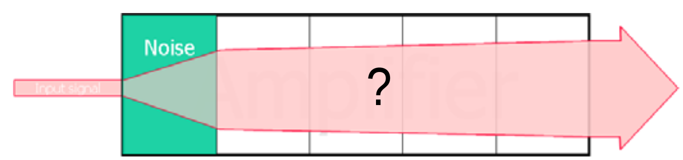
Why is it sufficient to consider the design of the first stage only during noise optimization?

a) Because at the input the noise is the largest
b) Because at the input the signal is the smallest
c) Because the gain of the first stage is large
d) Because the equivalent noise source is at the input

Orthogonality by design: distortion

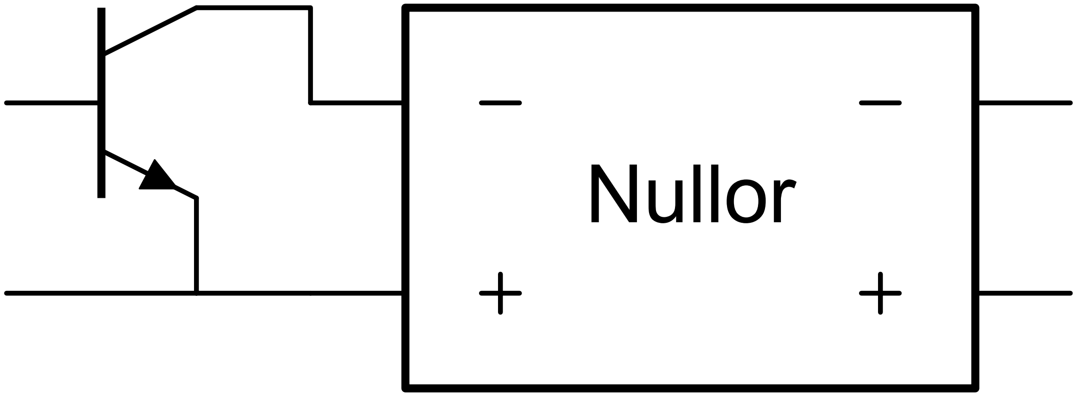


bandwidth – noise – distortion
bandwidth – distortion - noise
noise - bandwidth – distortion
noise – distortion - bandwidth
distortion - noise – bandwidth
distortion – bandwidth - noise

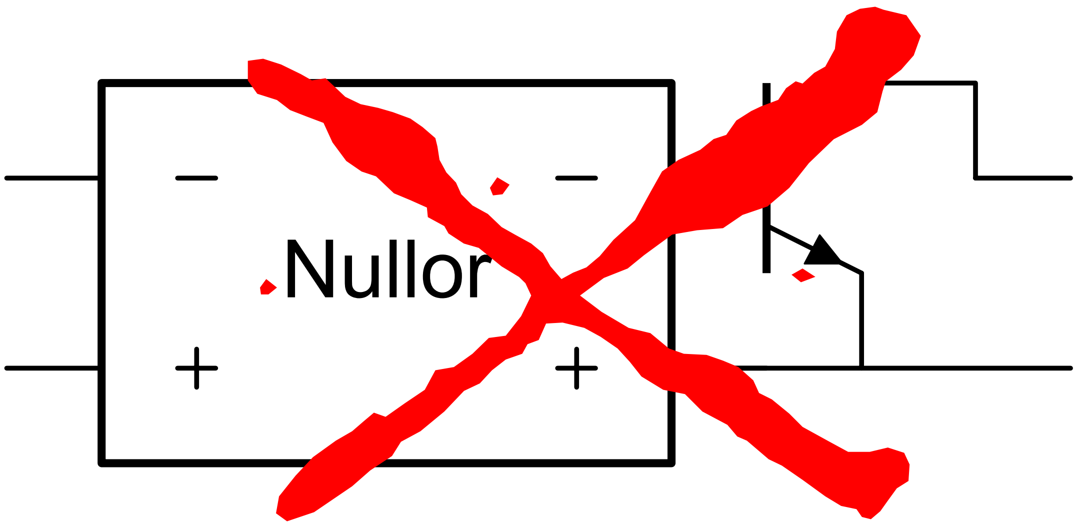


IF the last stage has a large gain,
then the clipping hazard for the preceding stages is negligible

Noise optimization is possible **with nullor in the loop**

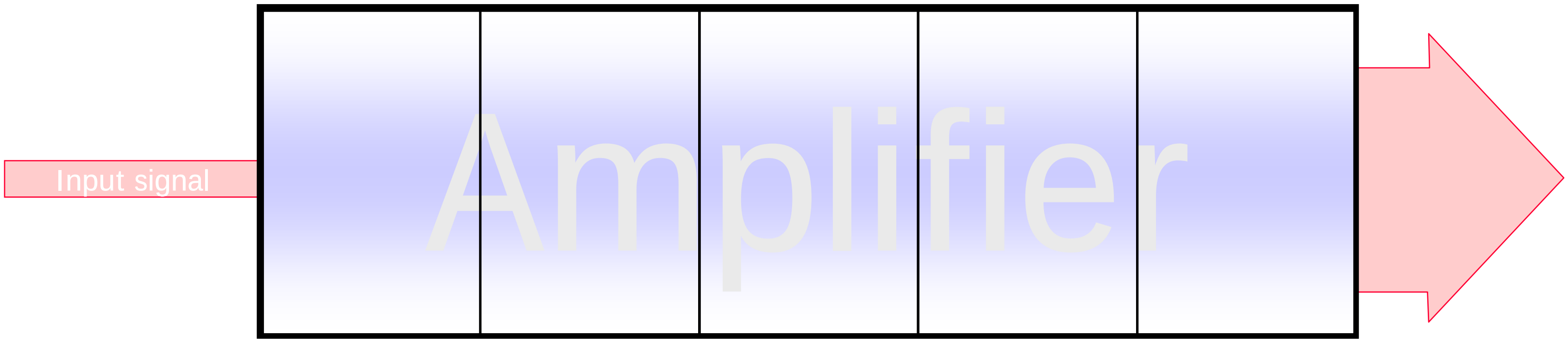


Noise : present
Bandwidth : infinite
Distortion : none



Noise : none
Bandwidth : infinite
Distortion : none

Bandwidth...



- **All** stages contribute to frequency behaviour
- Frequency behaviour can be improved **anywhere**
  - Not necessarily at input stage
  - Not necessarily at output stage
  - Bandwidth optimization is done last

Most orthogonal sequence: NDB

bandwidth – noise – distortion

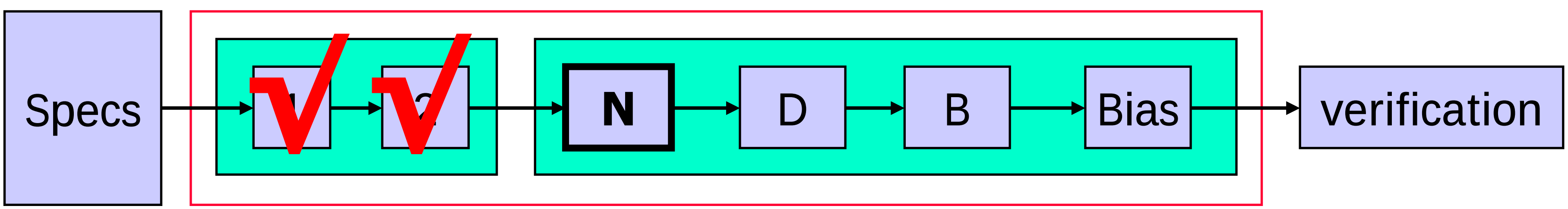
bandwidth – dist

noise - bandwidth

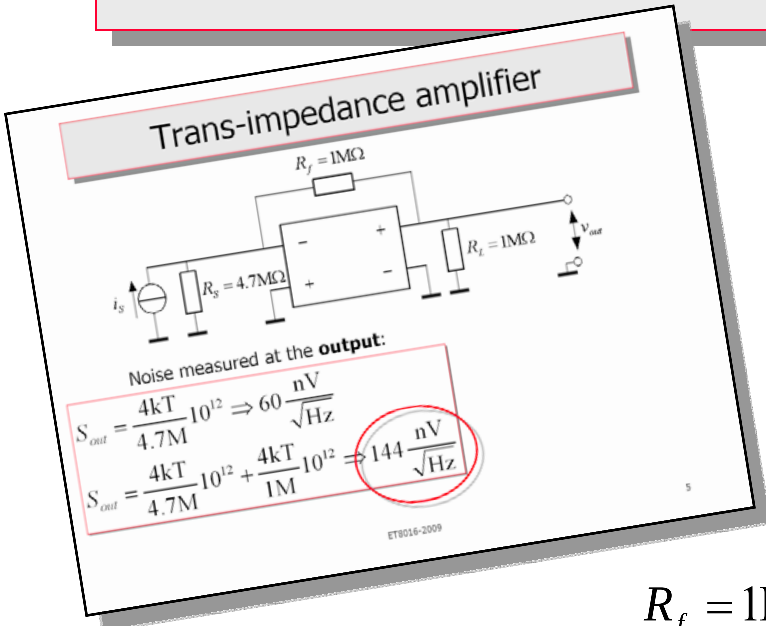
noise – distortio

distortion - noise –

distortion – bandwidth - noise



The first stage..



Trans-impedance amplifier

Noise measured at the **output**:

$$S_{out} = \frac{4kT}{4.7M}10^{12} \Rightarrow 60\frac{nV}{\sqrt{Hz}}$$

$$S_{out} = \frac{4kT}{4.7M}10^{12} + \frac{4kT}{1M}10^{12} \Rightarrow 144\frac{nV}{\sqrt{Hz}}$$

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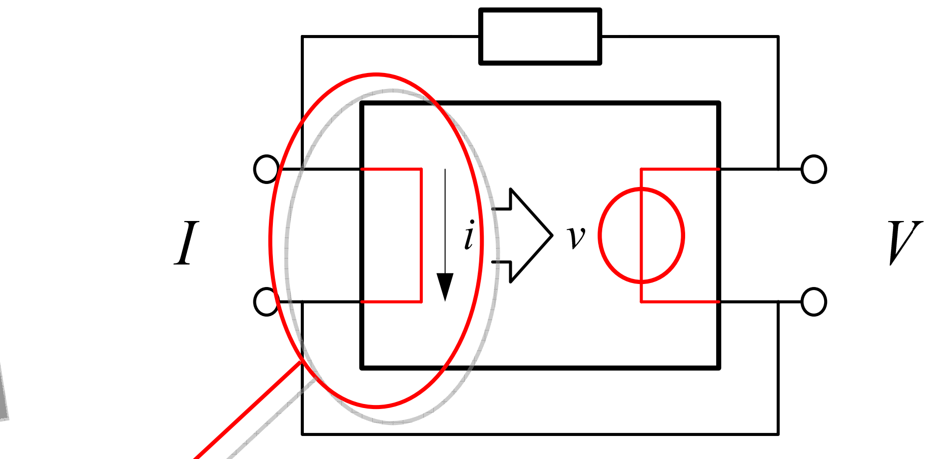
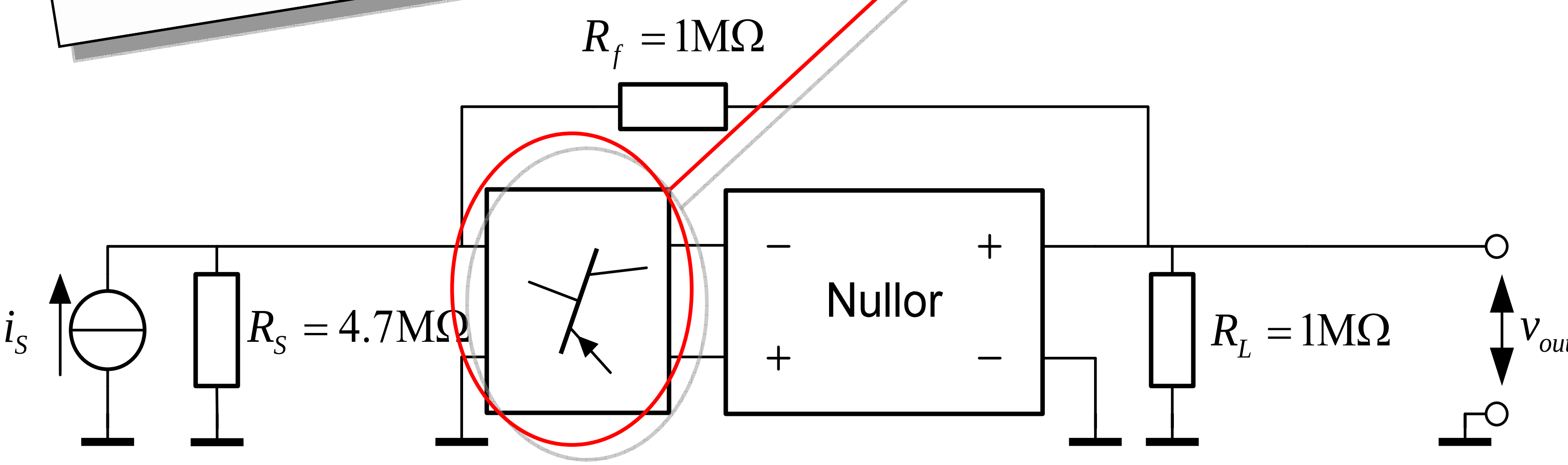
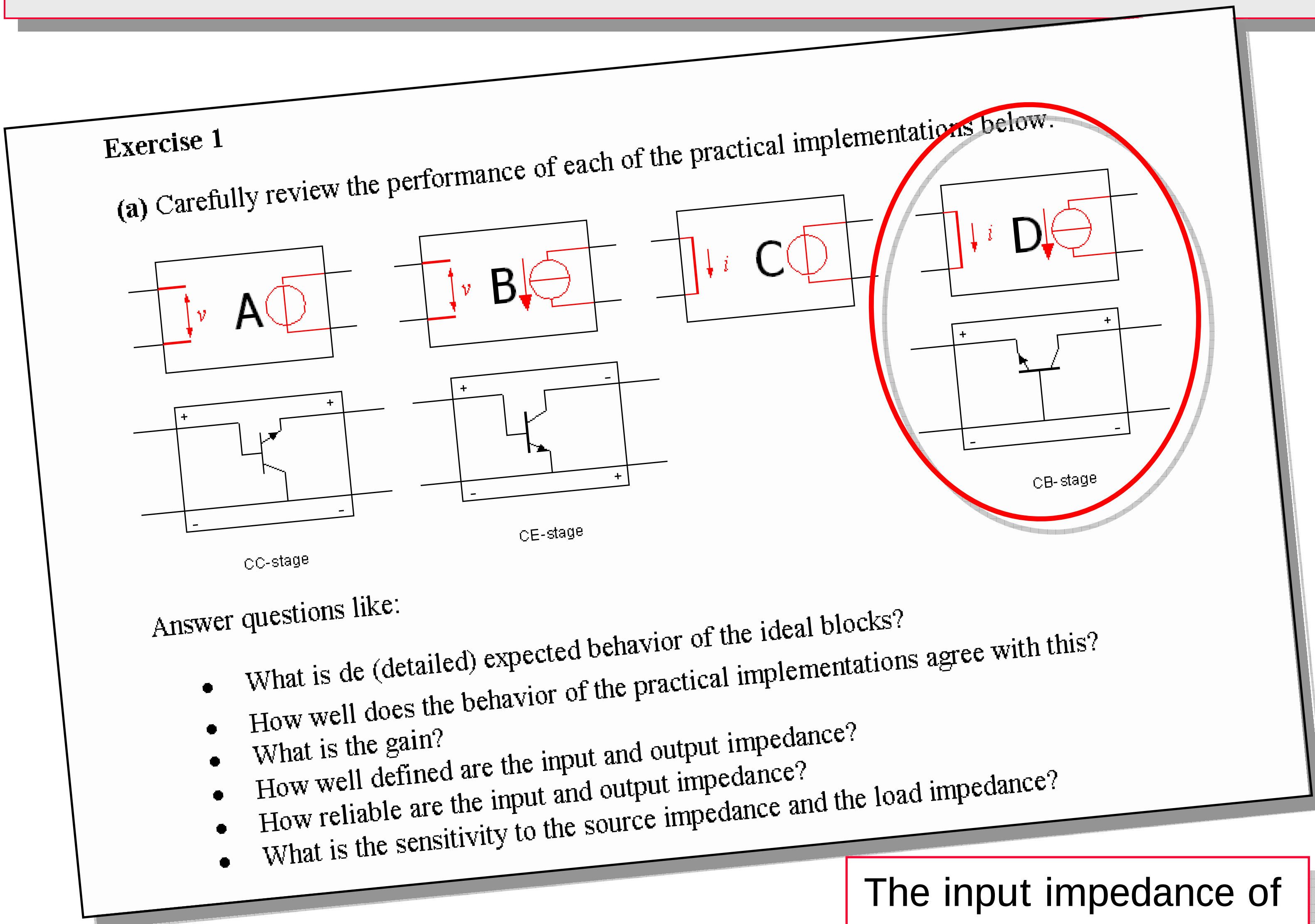




The first stage...



Exercise 1

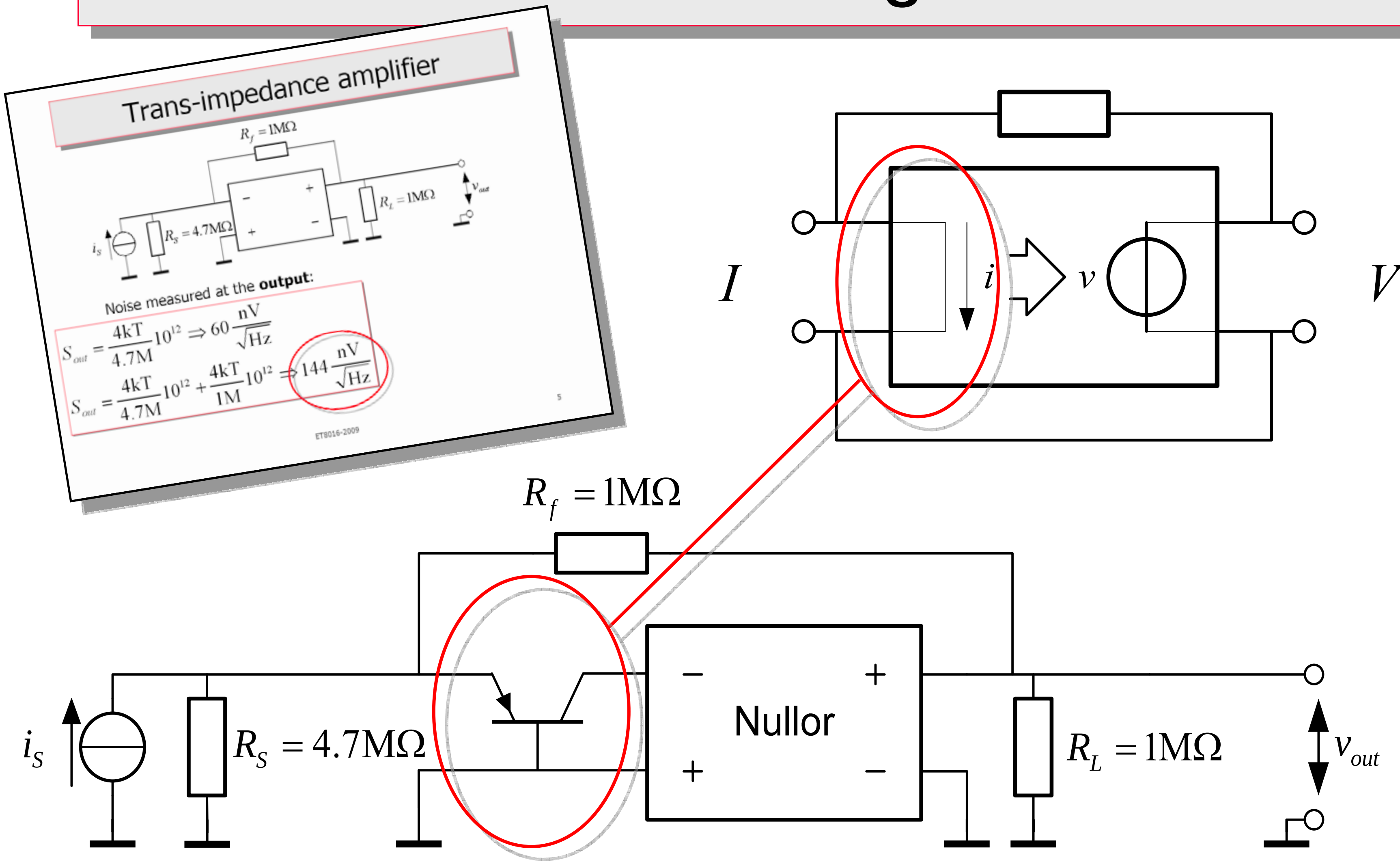
(a) Carefully review the performance of each of the practical implementations below.

Answer questions like:

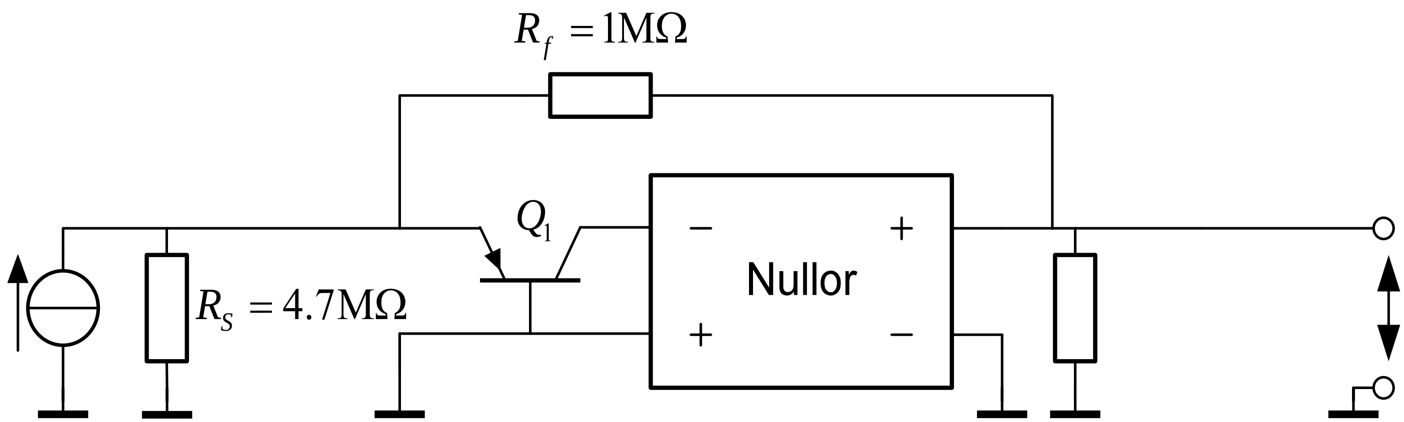
- What is de (detailed) expected behavior of the ideal blocks?
- How well does the behavior of the practical implementations agree with this?
- What is the gain?
- How well defined are the input and output impedance?
- How reliable are the input and output impedance?
- What is the sensitivity to the source impedance and the load impedance?

The input impedance of a CB stage is the lowest

The first stage..



Noise at the output via PSPICE



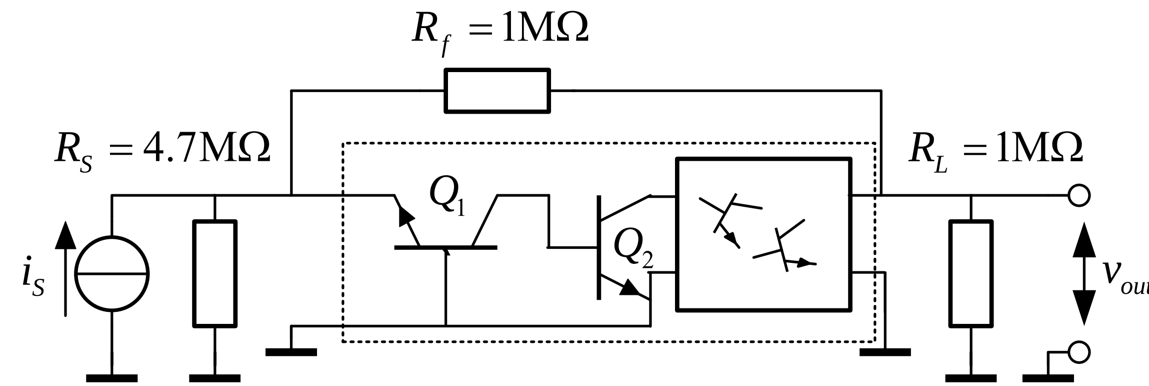
$$
\begin{aligned}
R_s &: 60 \ \text{nV}/\sqrt{\text{Hz}} \\
R_f &: 128 \ \text{nV}/\sqrt{\text{Hz}} \\
R_{bQ1} &: 0.4 \ \text{nV}/\sqrt{\text{Hz}} \\
I_{cQ1} &: 14 \ \text{nV}/\sqrt{\text{Hz}} \\
I_{bQ1} &: 130 \ \text{nV}/\sqrt{\text{Hz}} \\
\hline
& \ \ 193 \ \text{nV}/\sqrt{\text{Hz}}
\end{aligned}
$$

Gyrator: $60 \frac{\text{nV}}{\sqrt{\text{Hz}}}$

Resistor feedback: $144 \frac{\text{nV}}{\sqrt{\text{Hz}}}$

Input transistor: $193 \frac{\text{nV}}{\sqrt{\text{Hz}}}$

Influence second stage



R_s	:	60	nV/√Hz
R_f	:	128	nV/√Hz
R_{bQ1}	:	0.4	nV/√Hz
I_{cQ1}	:	14	nV/√Hz
I_{bQ1}	:	130	nV/√Hz
R_{bQ2}	:	0.0024	nV/√Hz
I_{cQ2}	:	95	nV/√Hz
I_{bQ2}	**:**	**1300.0**	**nV/√Hz**
		1314	nV/√Hz

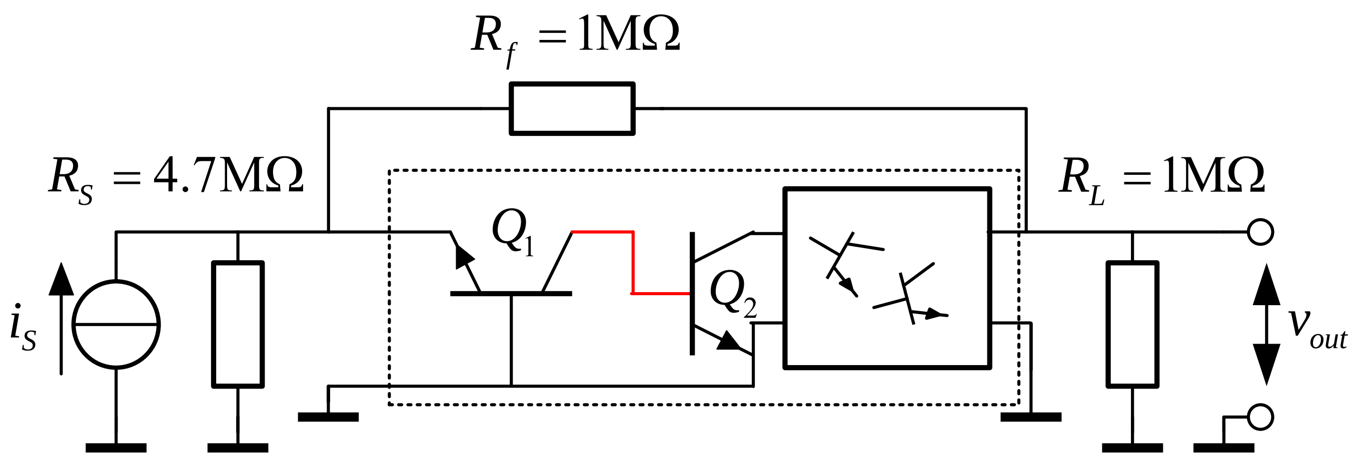
Gyrator: $60 \frac{\text{nV}}{\sqrt{\text{Hz}}}$

Resistor feedback: $144 \frac{\text{nV}}{\sqrt{\text{Hz}}}$

Input transistor: $193 \frac{\text{nV}}{\sqrt{\text{Hz}}}$

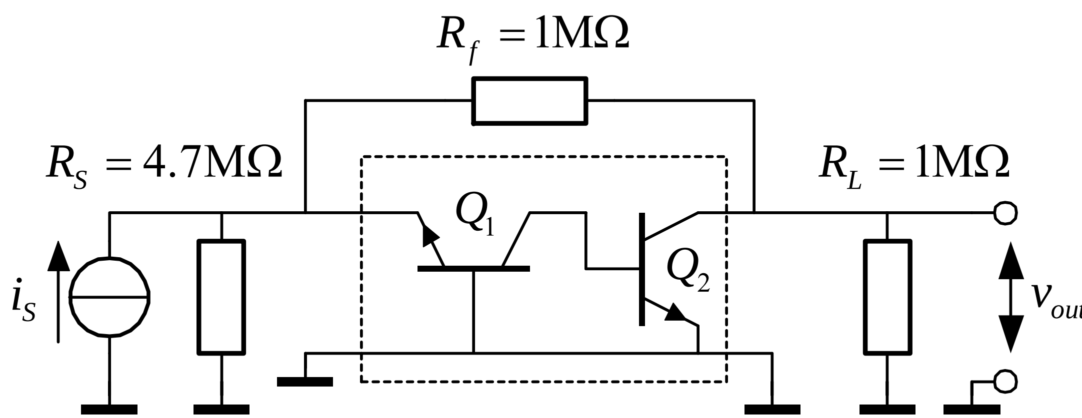
Reduction of the noise contribution of Q_2.

$2qI_b$ lower



Biasing Q_2 lower $\Rightarrow$ noise lower

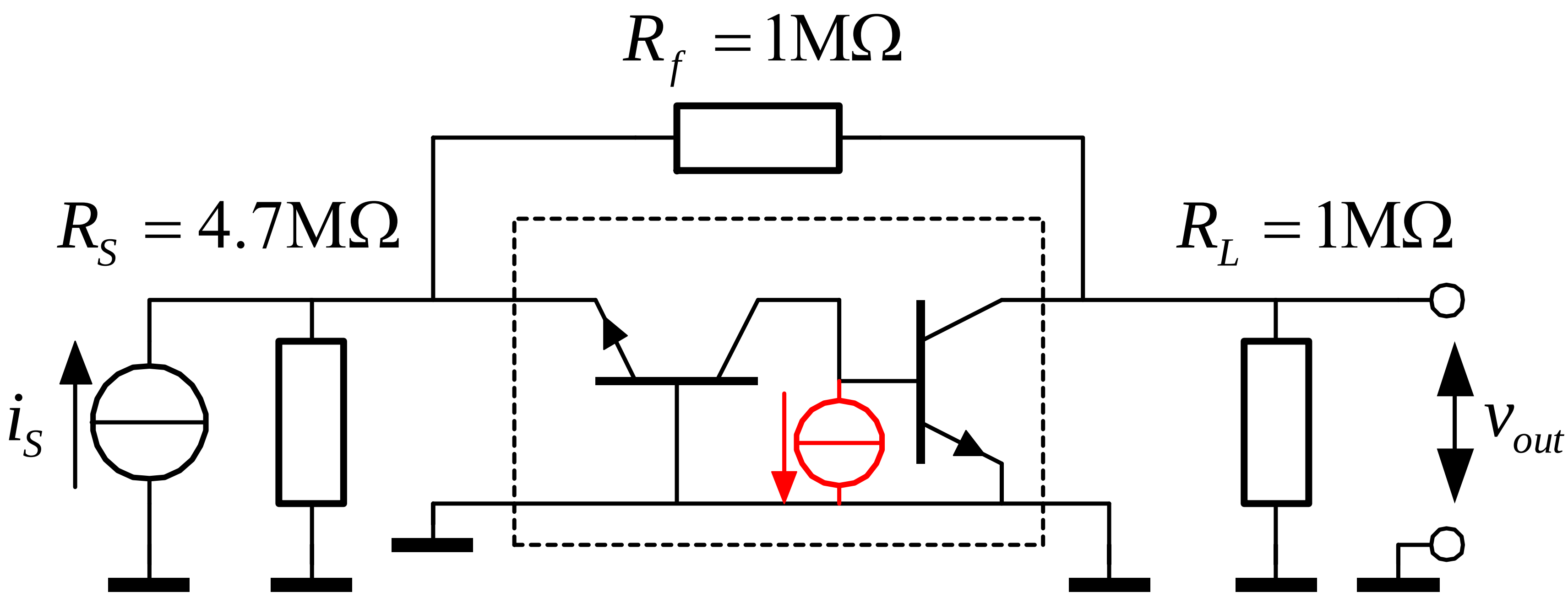
Noise



Distortion

Orthogonality!!

The real cause of the problem?

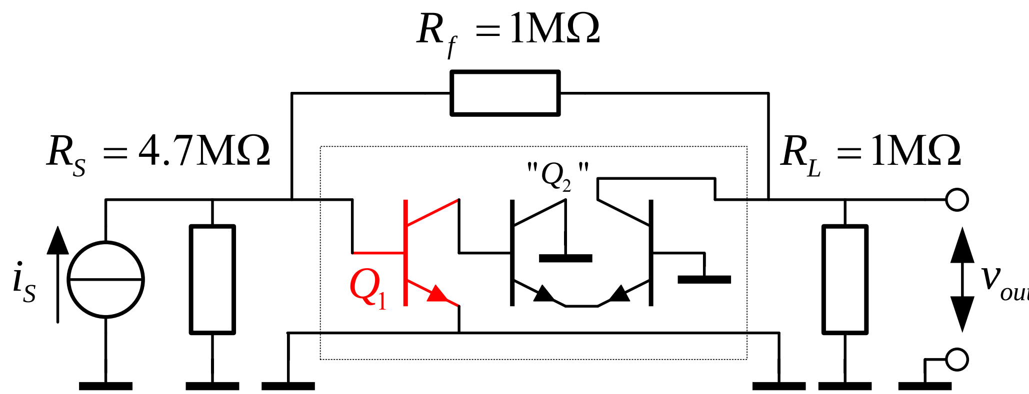


$$D_{Q1} = 1$$

Noise with CE input stage

R_s	:	54	nV/√Hz
R_f	:	120	nV/√Hz
R_L	:	0.7	nV/√Hz
R_{bQ1}	:	0.4	nV/√Hz
I_{cQ1}	:	14	nV/√Hz
I_{bQ1}	:	130	nV/√Hz
R_{bQ2}	:	0.0024	nV/√Hz
I_{cQ2}	:	95	nV/√Hz
I_{bQ2}	:	13.0	nV/√Hz

208 nV/√Hz

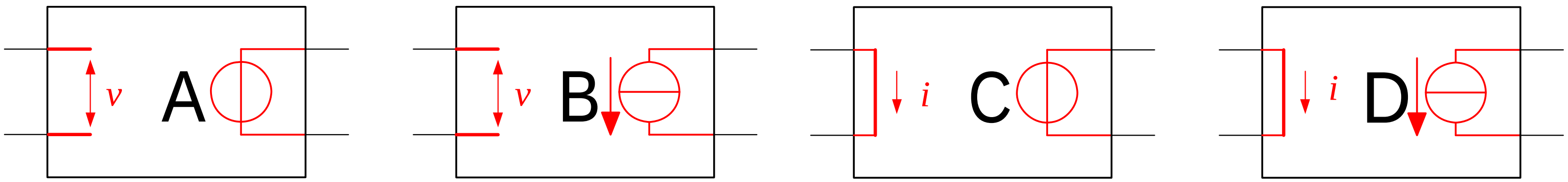


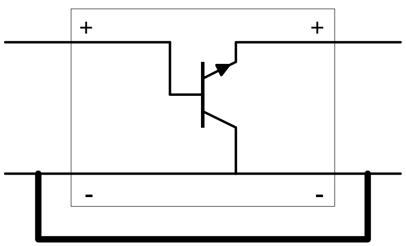
Gyrator: $60 \frac{\text{nV}}{\sqrt{\text{Hz}}}$

Resistor feedback: $144 \frac{\text{nV}}{\sqrt{\text{Hz}}}$

Input transistor: $193 \frac{\text{nV}}{\sqrt{\text{Hz}}}$

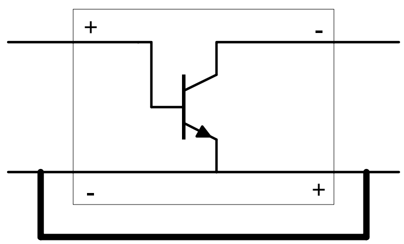
The first stage...





a

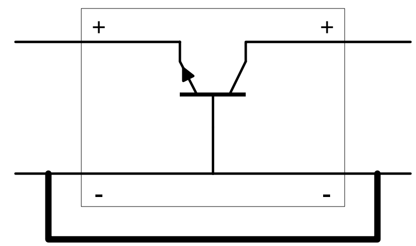
$$\begin{pmatrix} 1 & \approx 0 \\ \approx 0 & \approx 0 \end{pmatrix}$$



CE-stage

$$\begin{pmatrix} \approx 0 & \approx 0 \\ \approx 0 & \approx 0 \end{pmatrix}$$

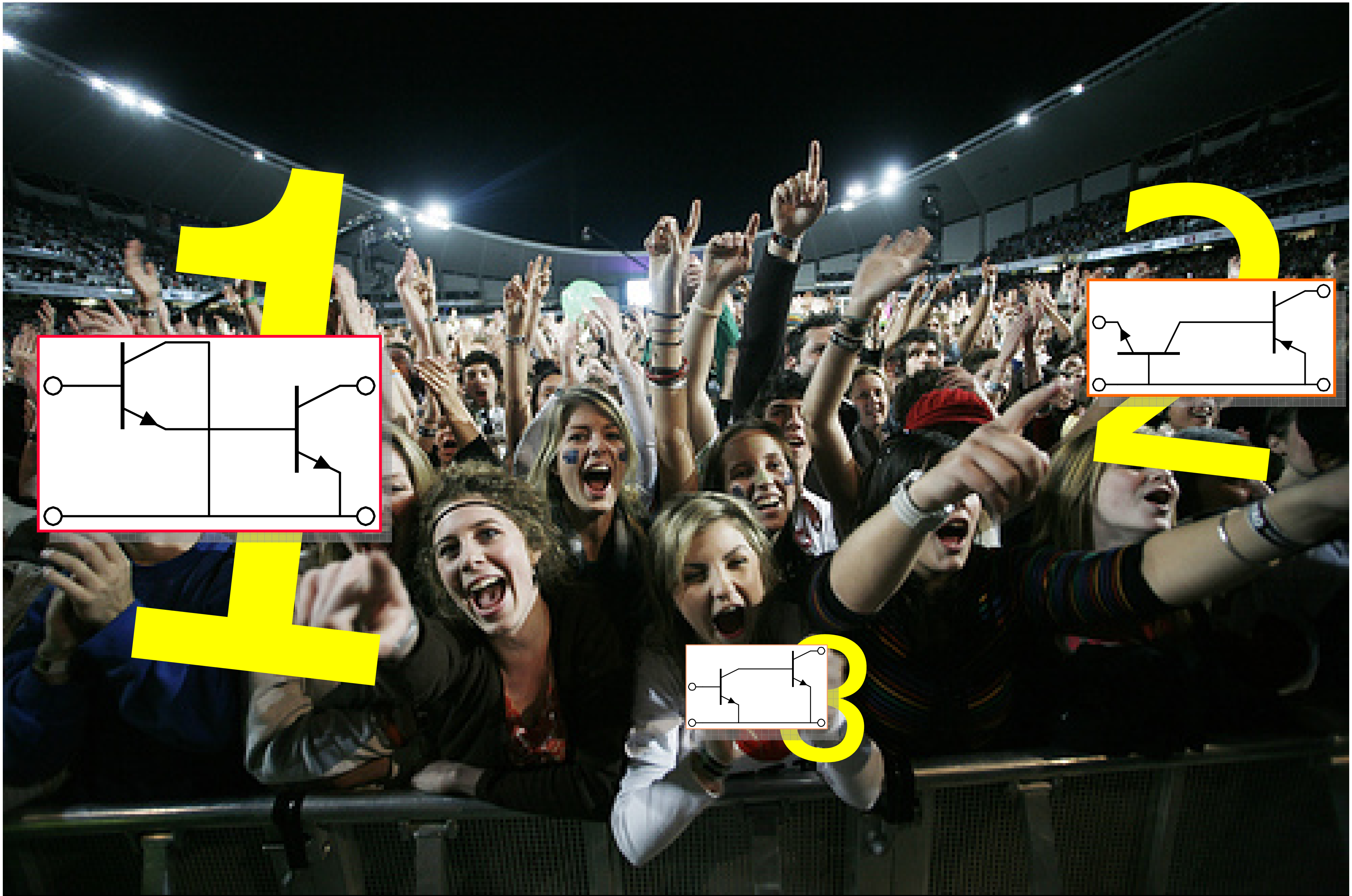
$$\begin{pmatrix} ? & ? \\ ? & ? \end{pmatrix}$$



CB-stage

$$\begin{pmatrix} \approx 0 & \approx 0 \\ \approx 0 & 1 \end{pmatrix}$$

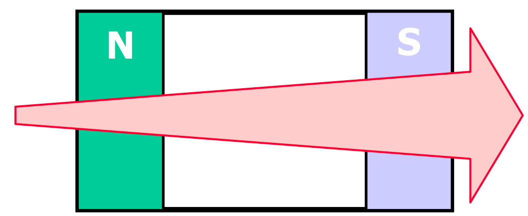
Gain is most important!



There is no right or wrong, just best, second best, ...

Design rule for noise

1st stage large gain



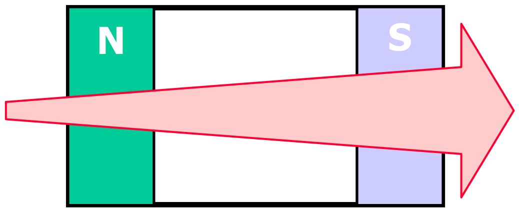
Noise behavior dominated by 1st stage

Orthogonality

Design rule for distortion

Last stage large gain

Clipping only in last stage



Orthogonality

Design rule for bandwidth

- Effects at any place in the loop
- Not necessarily at input
- Not necessarily at output

After steps noise and distortion

The most orthogonal sequence

~~bandwidth – noise – distortion~~

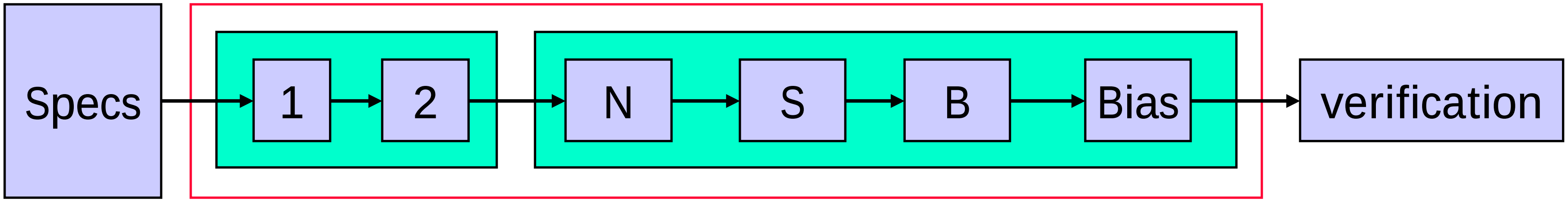
~~bandwidth – distortion - noise~~

~~noise - bandwidth – distortion~~

noise – distortion - bandwidth

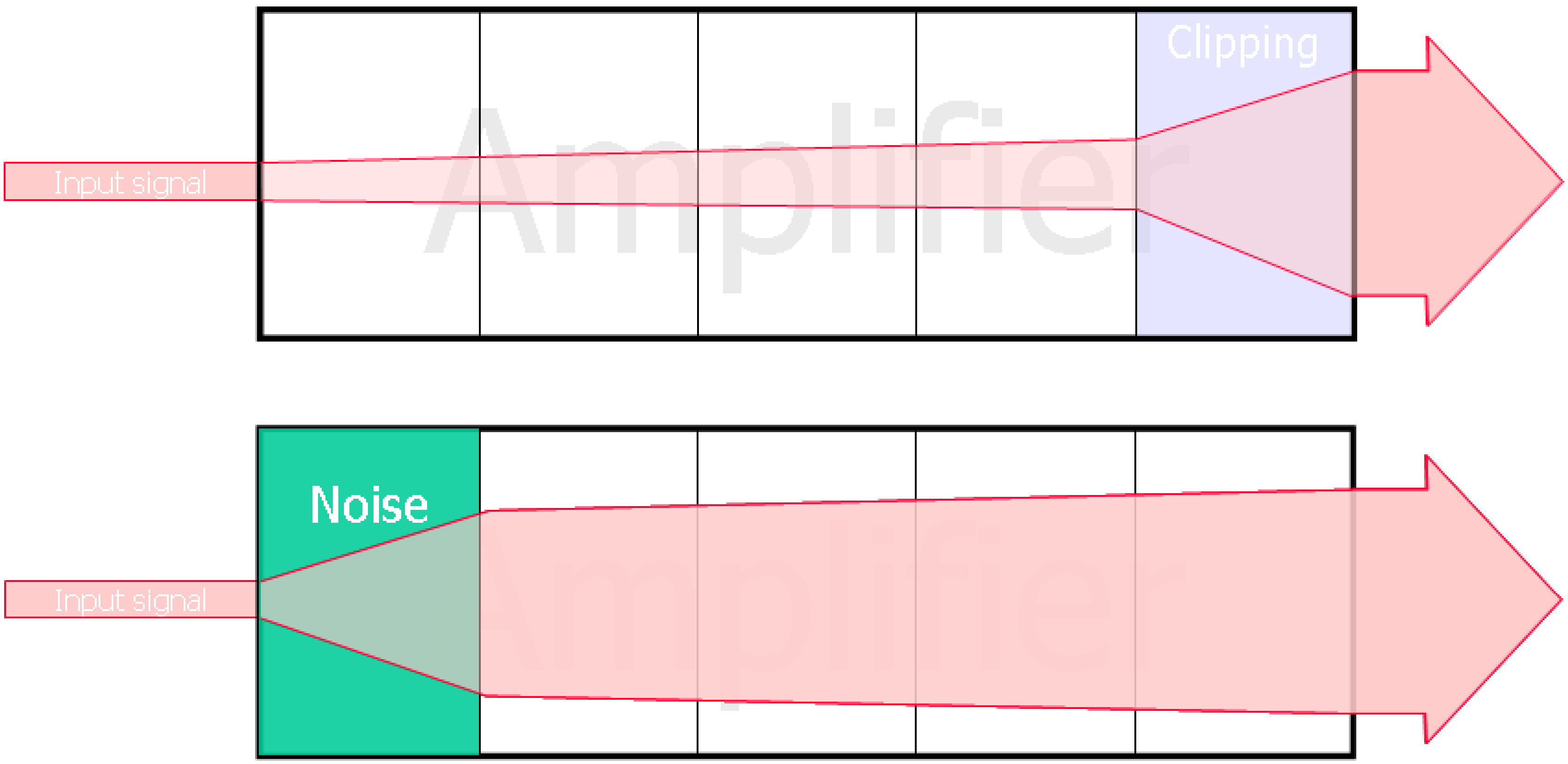
~~distortion - noise – bandwidth~~

~~distortion – bandwidth - noise~~

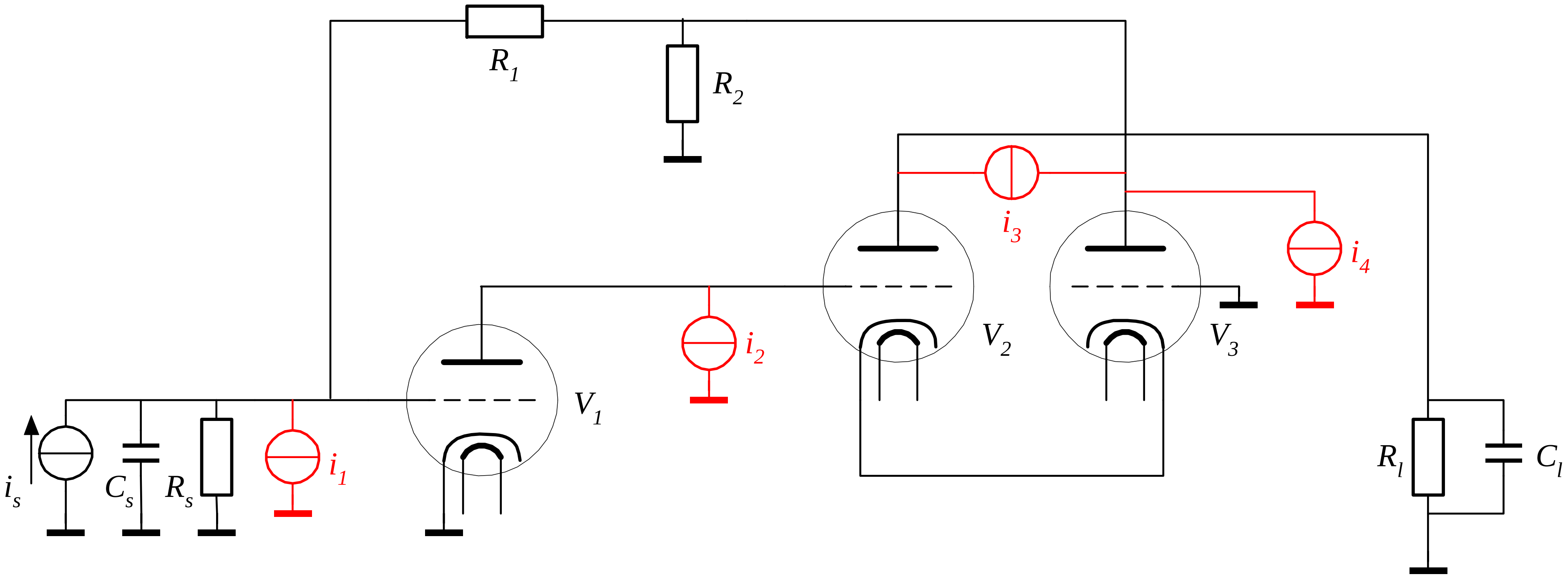


We want it all...

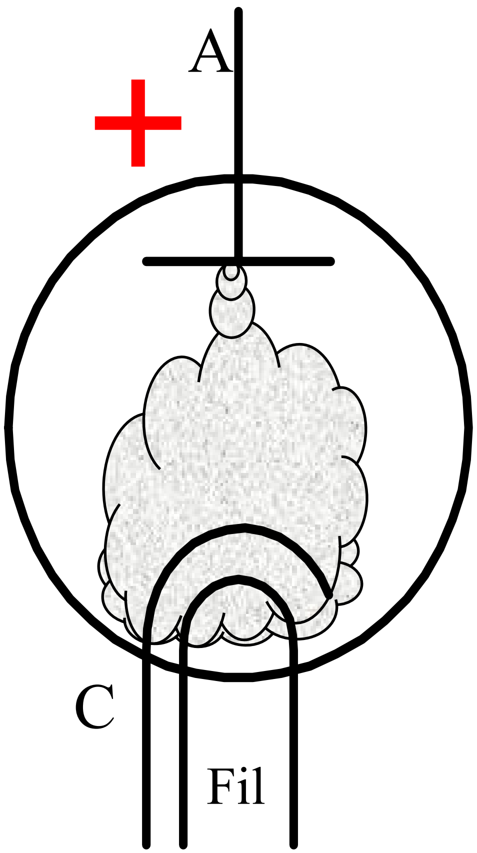
Input and output magnitude are fixed



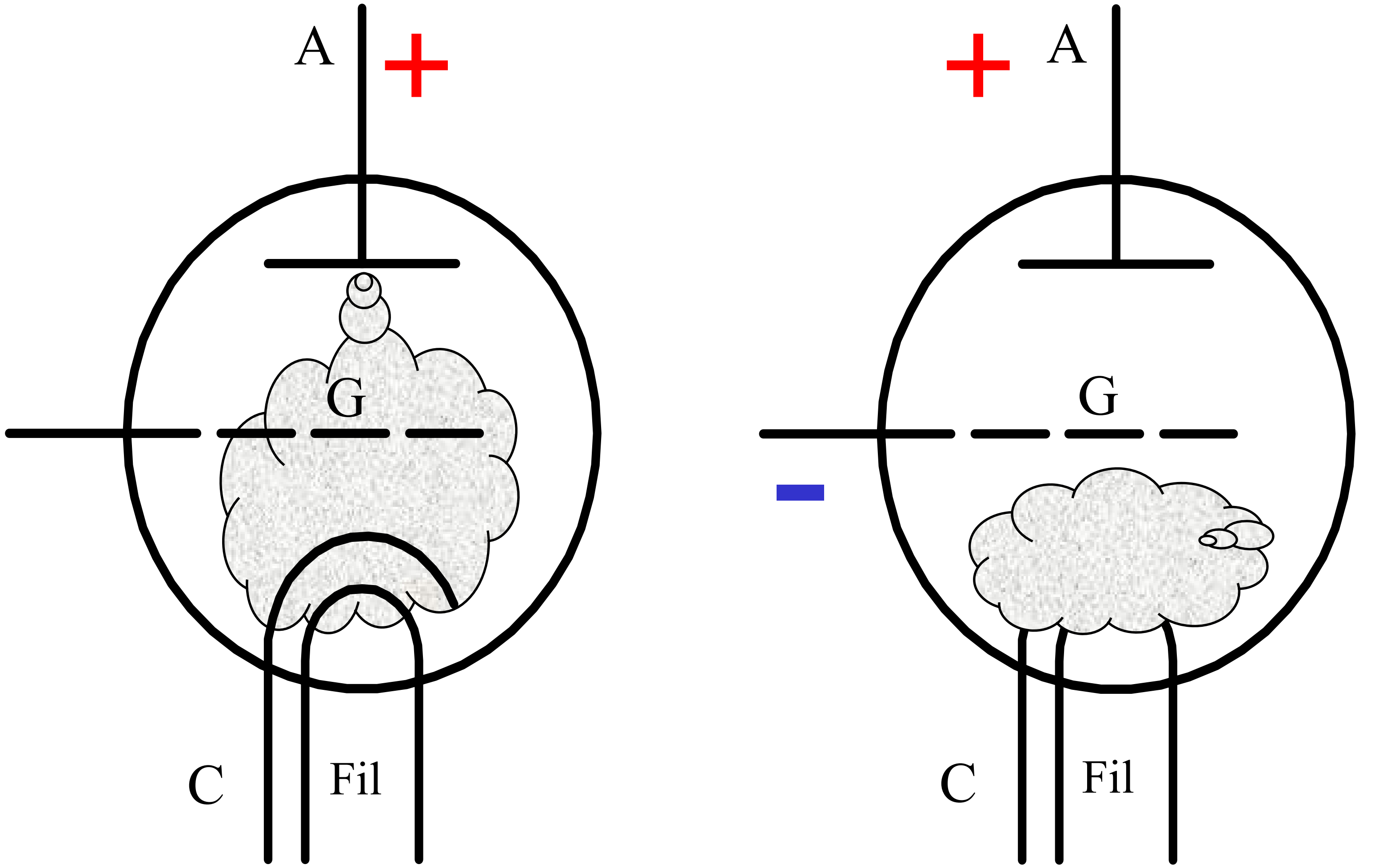
Demonstration



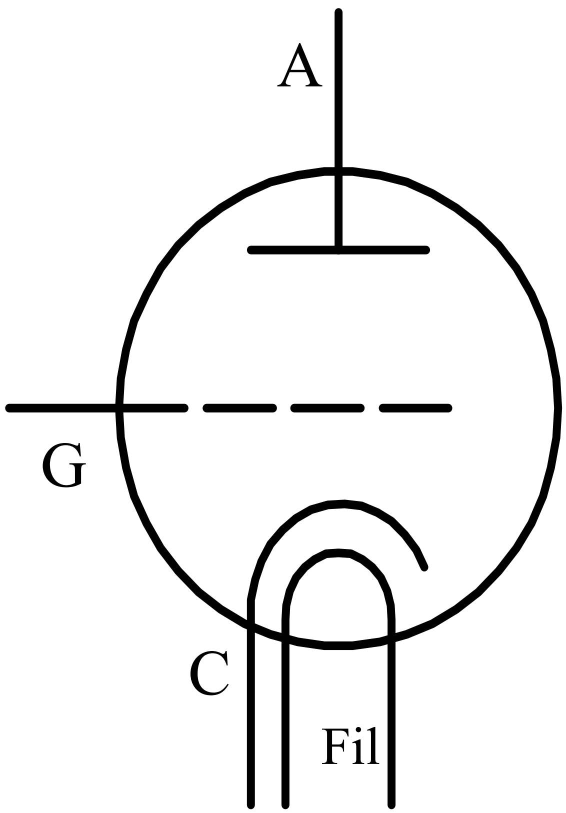
Vacuum tubes

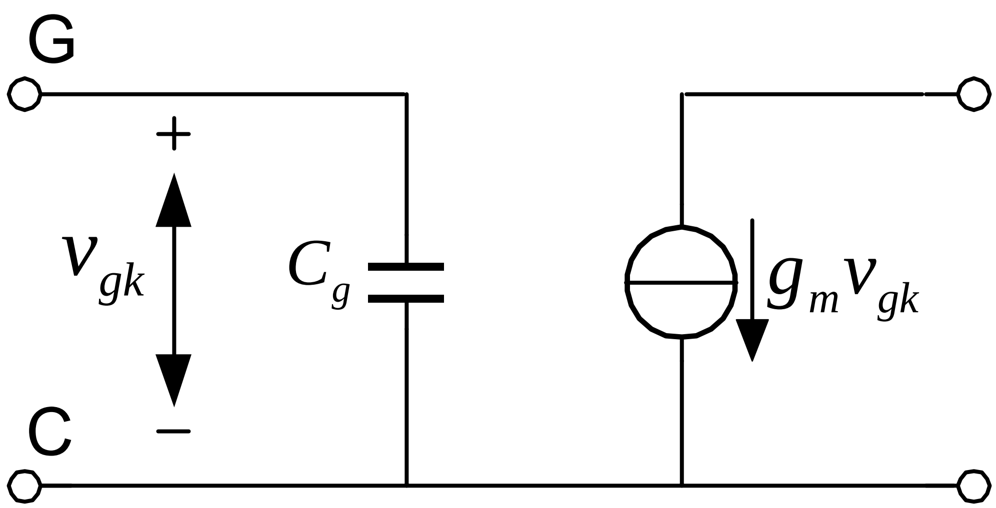


Triode

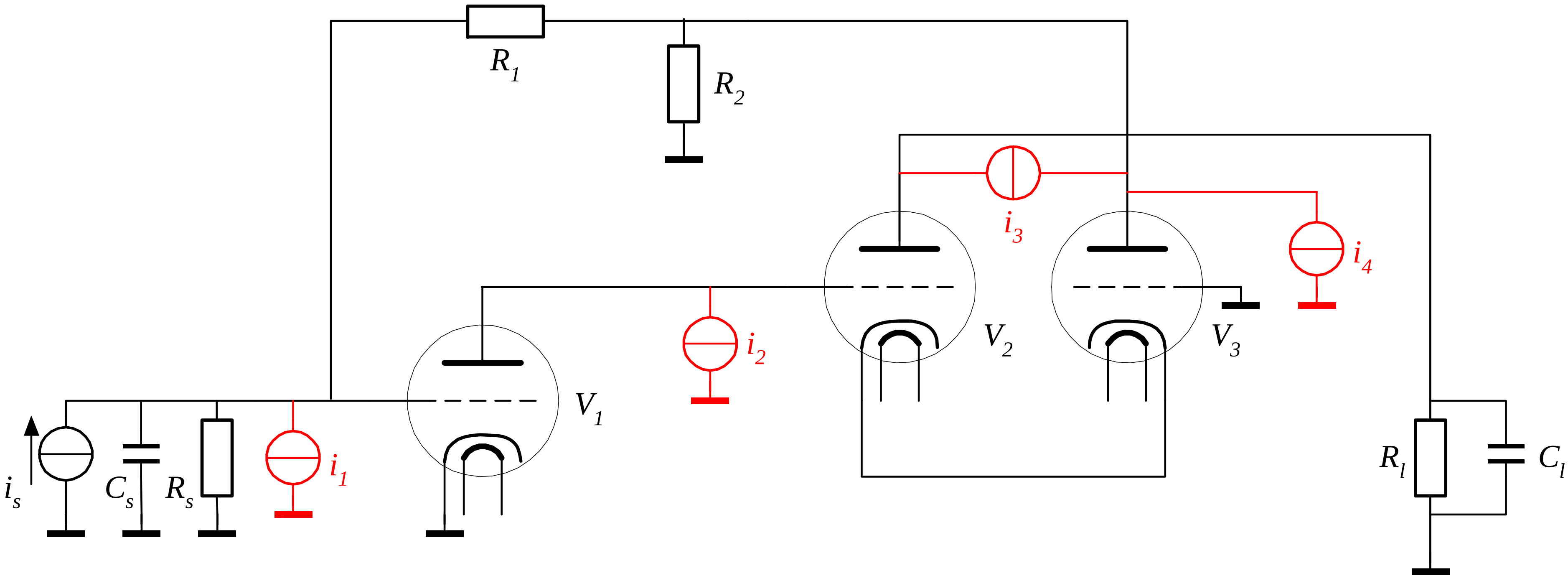


Small-signal model

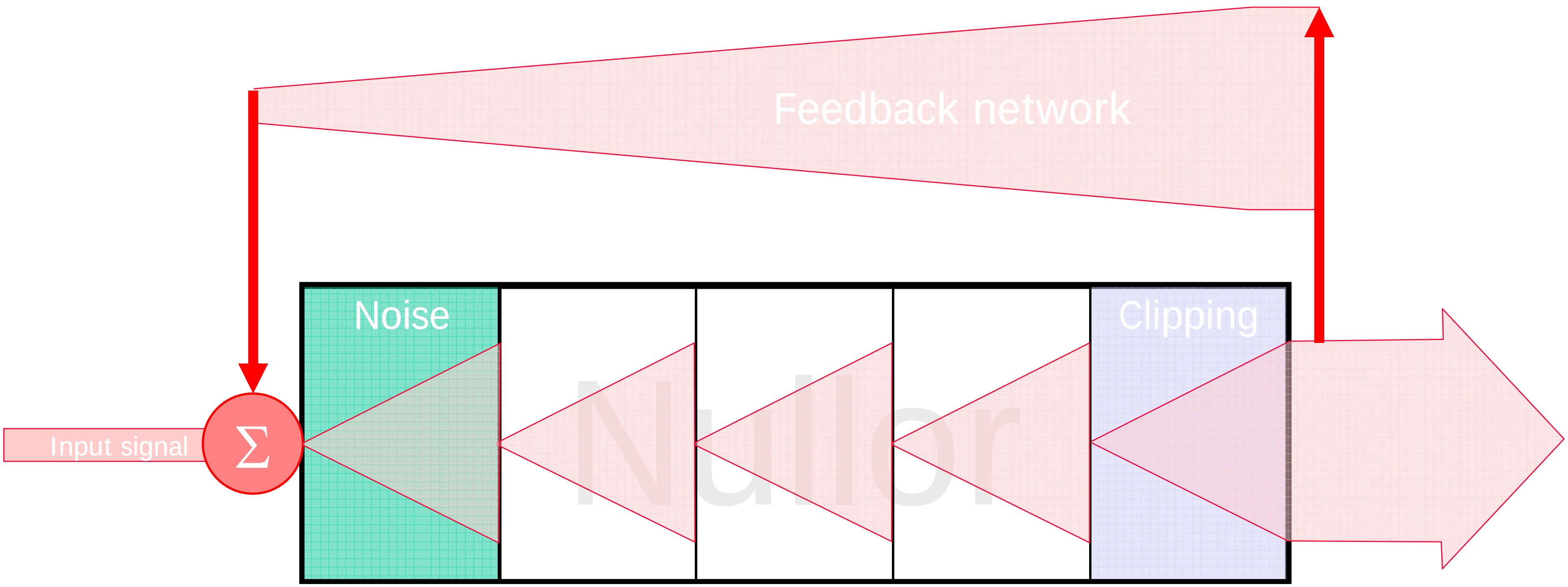




Demonstration



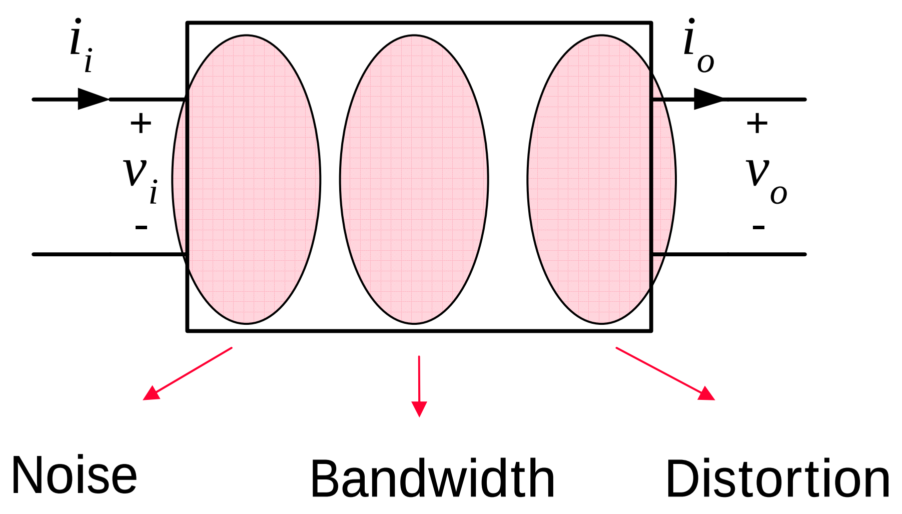
Negative feedback gives orthogonality



Total gain of active part is not limited to overall gain
All stages can have unlimited gain

Conclusions

- All stages should have maximal gain (CE CS)
- First stage : noise behavior
- Last stage : clipping
- Most orthogonal order: N, D, B

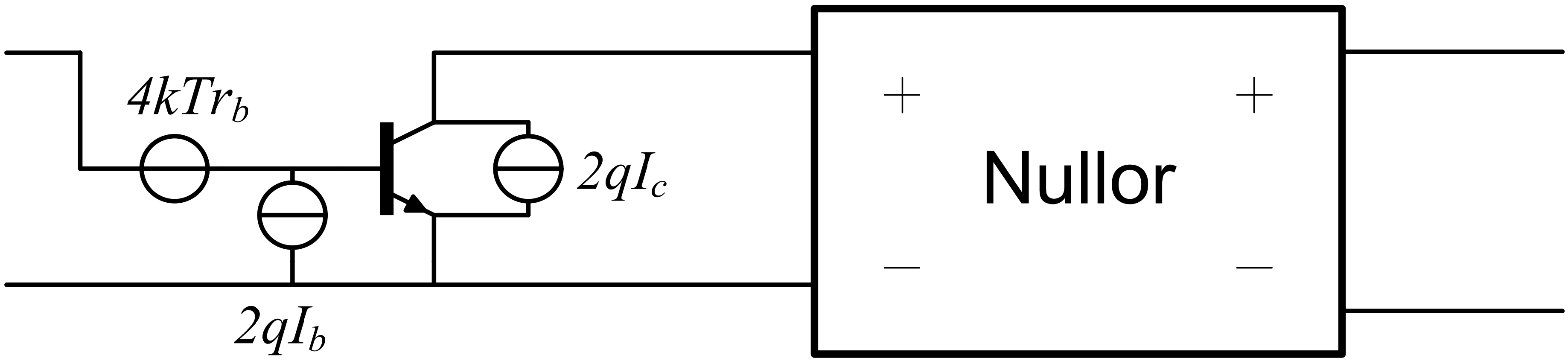


Conclusions

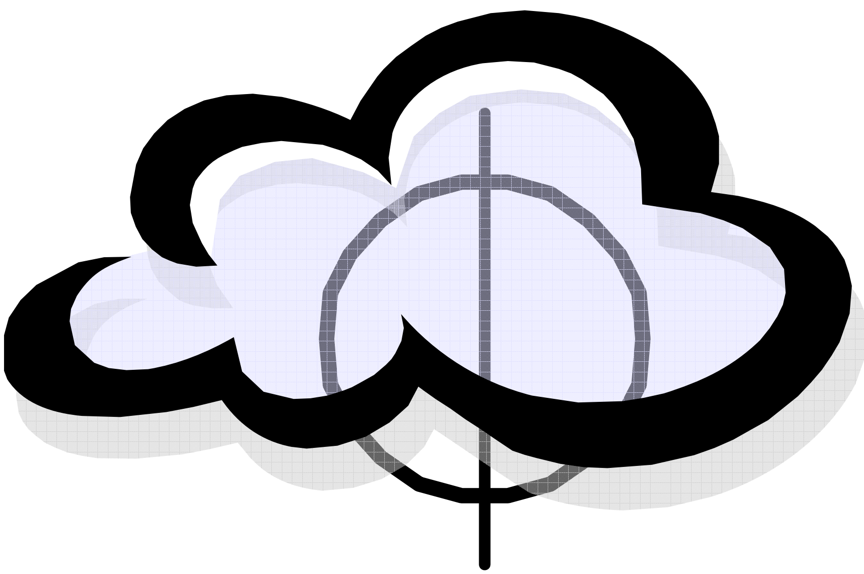
Negative feedback gives superior noise performance because:

1. First stage can be perfectly optimized for noise
2. First stage suppresses noise of cascading stages maximally
   - The Loop Gain can be much higher than the input-to-output gain of the amplifier
   - All stages *can have* maximum gain
3. Input impedance does not depend on first stage

Step 3: Noise design



What do we know about a noise source?

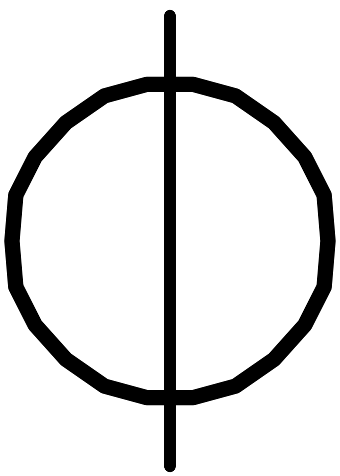


power density

E.g.: $S(v_n) = 4kTR$

$$P_n = \int_{B_{\inf}} S(v_n)\,df = \overline{v_n^2}$$

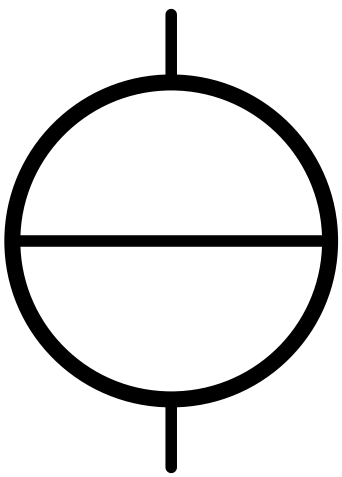
Representation



- Voltage source
  - Use value v_n although only P_n is known
  - Transform them as voltages
  - Shift them as voltages
- Calculate the equivalent power
  - Add correlated voltages
  - Add power uncorrelated voltages

Similar representation for current sources

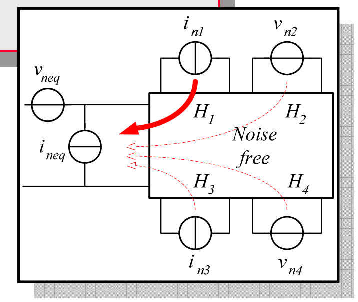
Representation

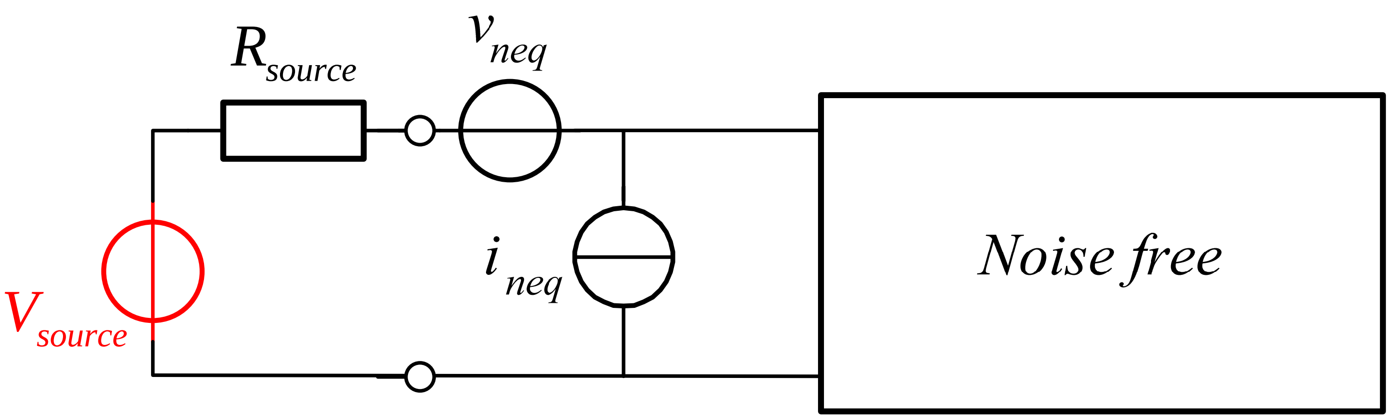


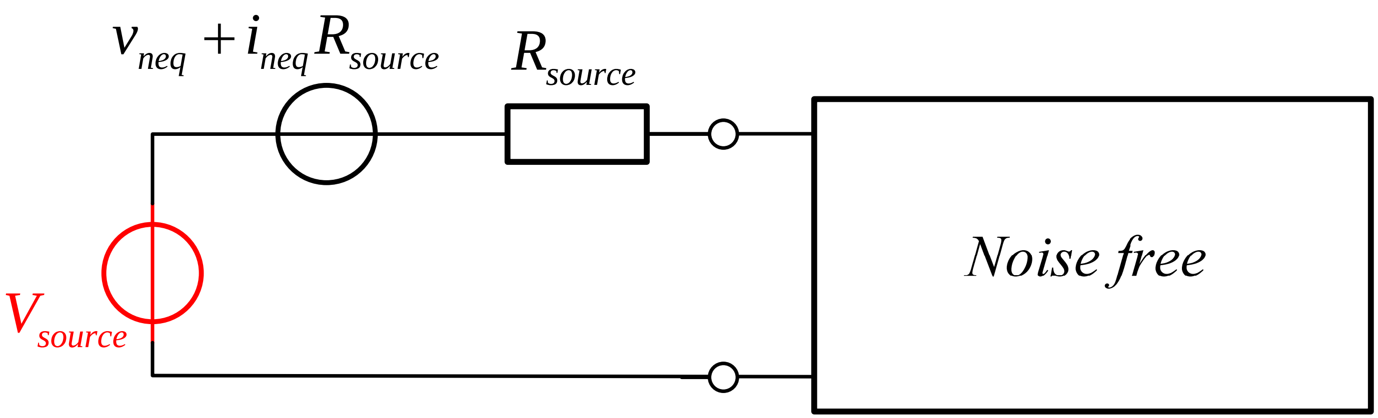
- Current source
  - Use value i_n although only P_n is known
  - Transform them as currents
  - Shift them as currents

- Calculate the equivalent power
  - Add correlated currents
  - Add power uncorrelated currents

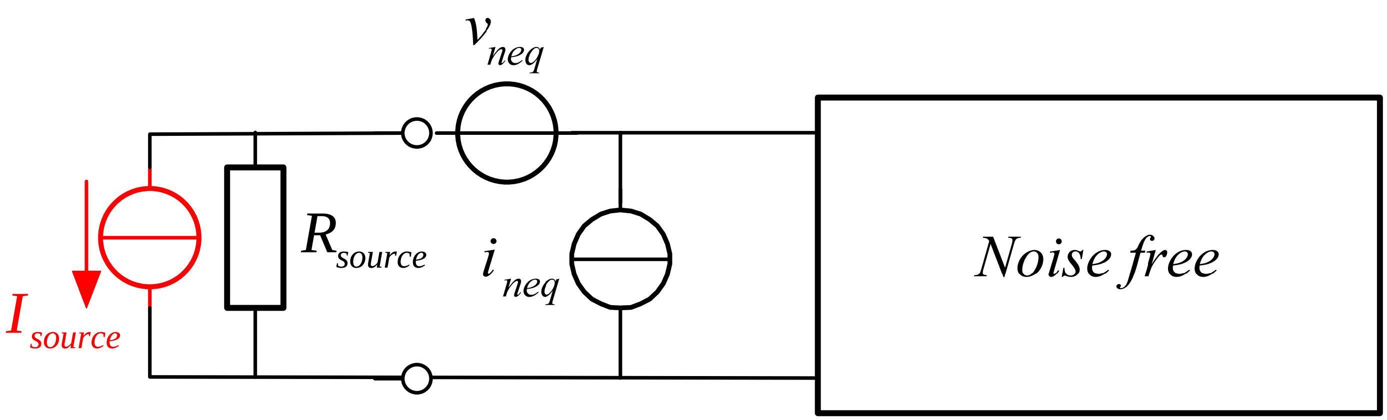
The equivalent noise source

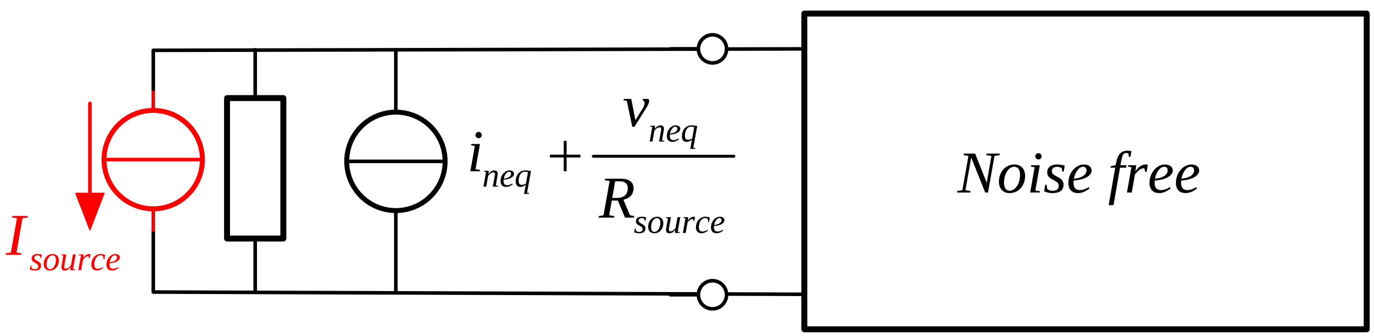






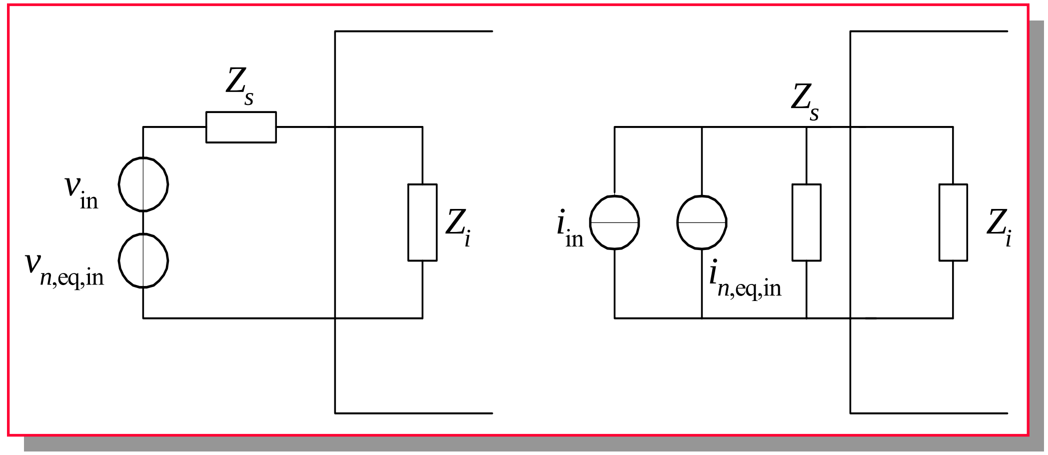
The equivalent noise source

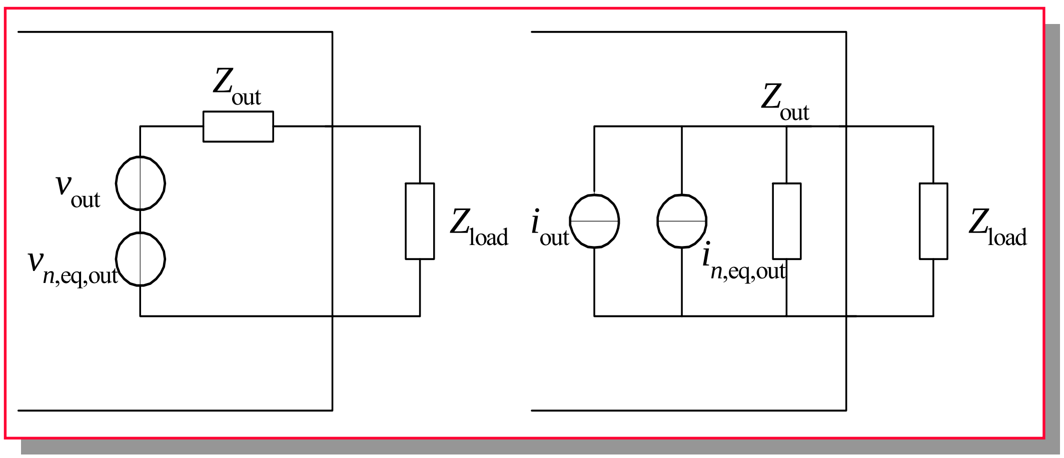




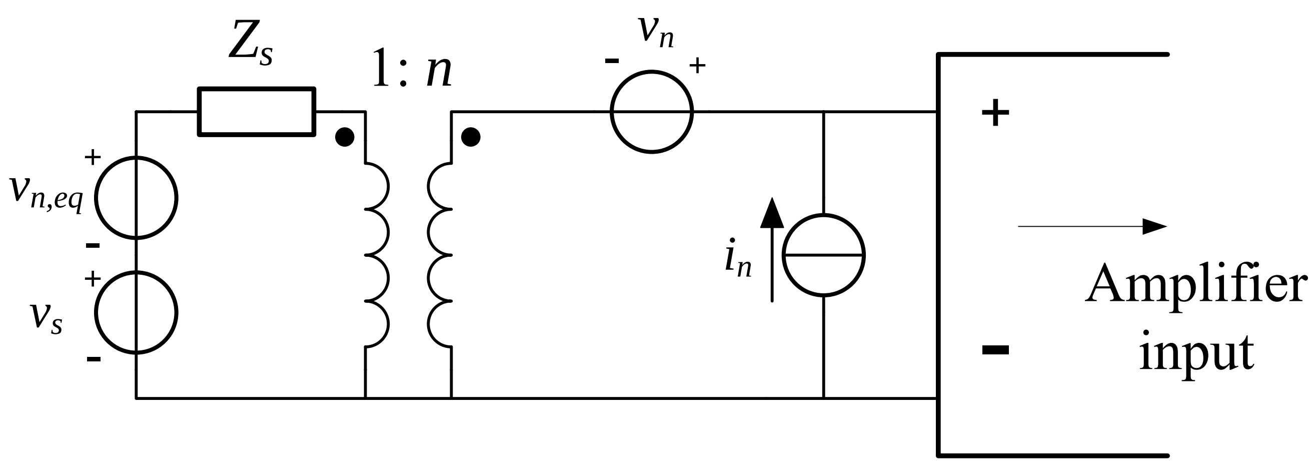
Signal to noise ratio

$$C = B\,{}^{2}\log \frac{S+N}{N}$$





Optimization via transformer



Choose ratio n to minimize equivalent noise source

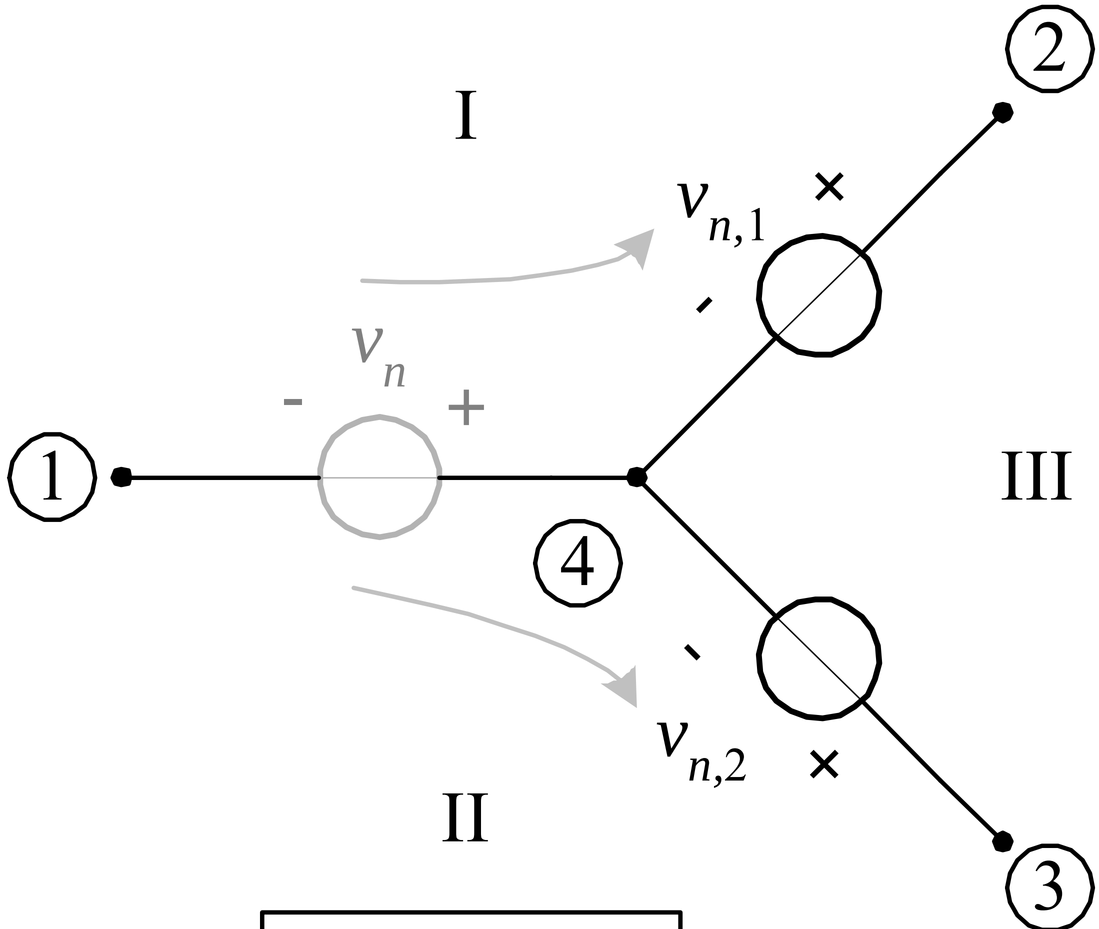
$$v_{neq} = \frac{v_n}{n} + nZ_s i_n$$

How to find the equivalent source?

Four methods:

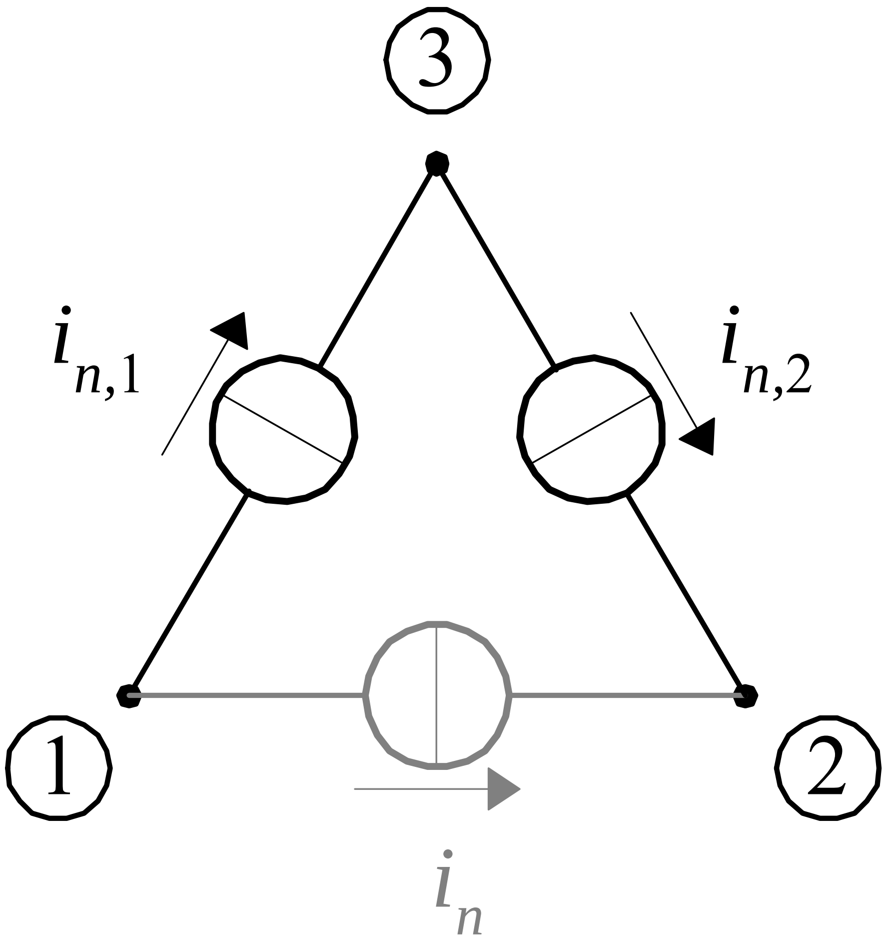
- Voltage source shift
- Current source shift
- Norton-Thevenin transform
- Shift through two-ports

Voltage source shift



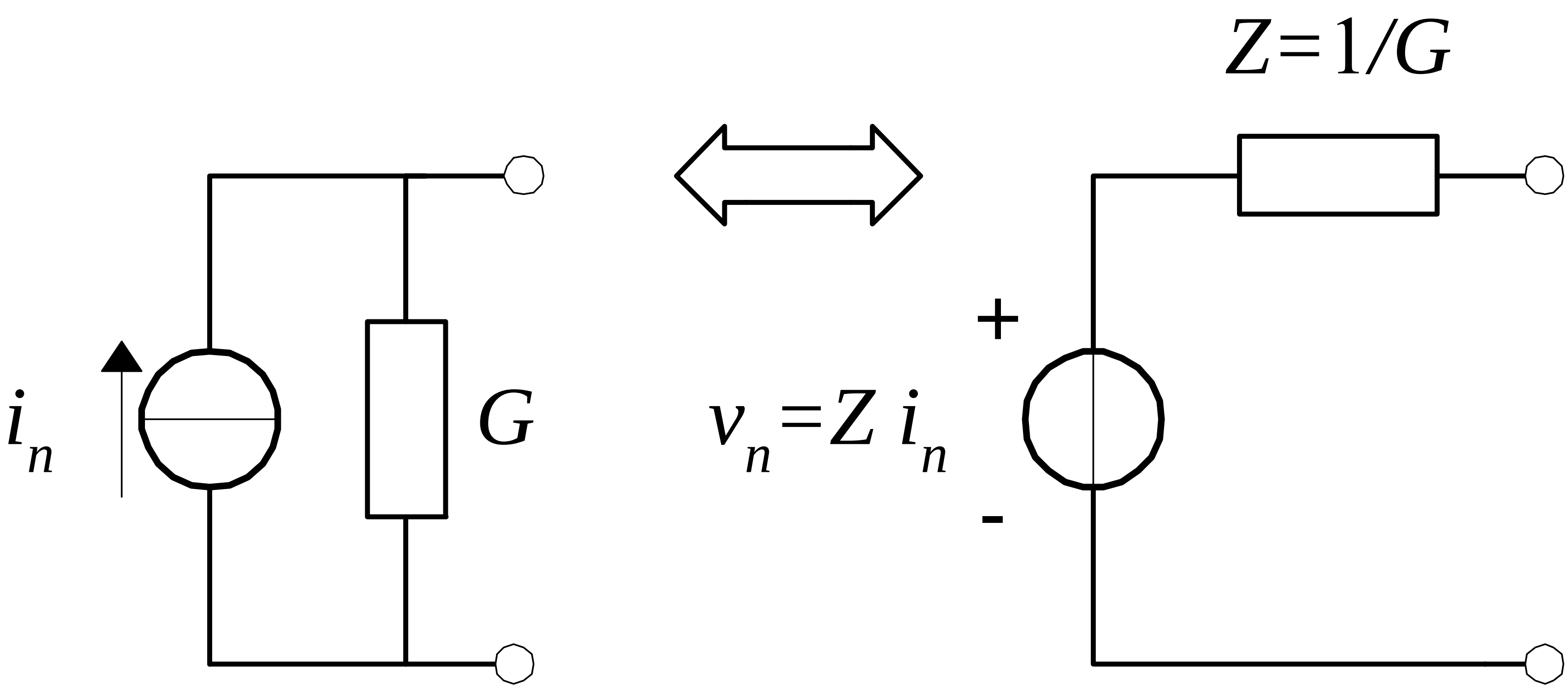
$$v_{n,1} = v_{n,2} = v_n$$

Current source shift

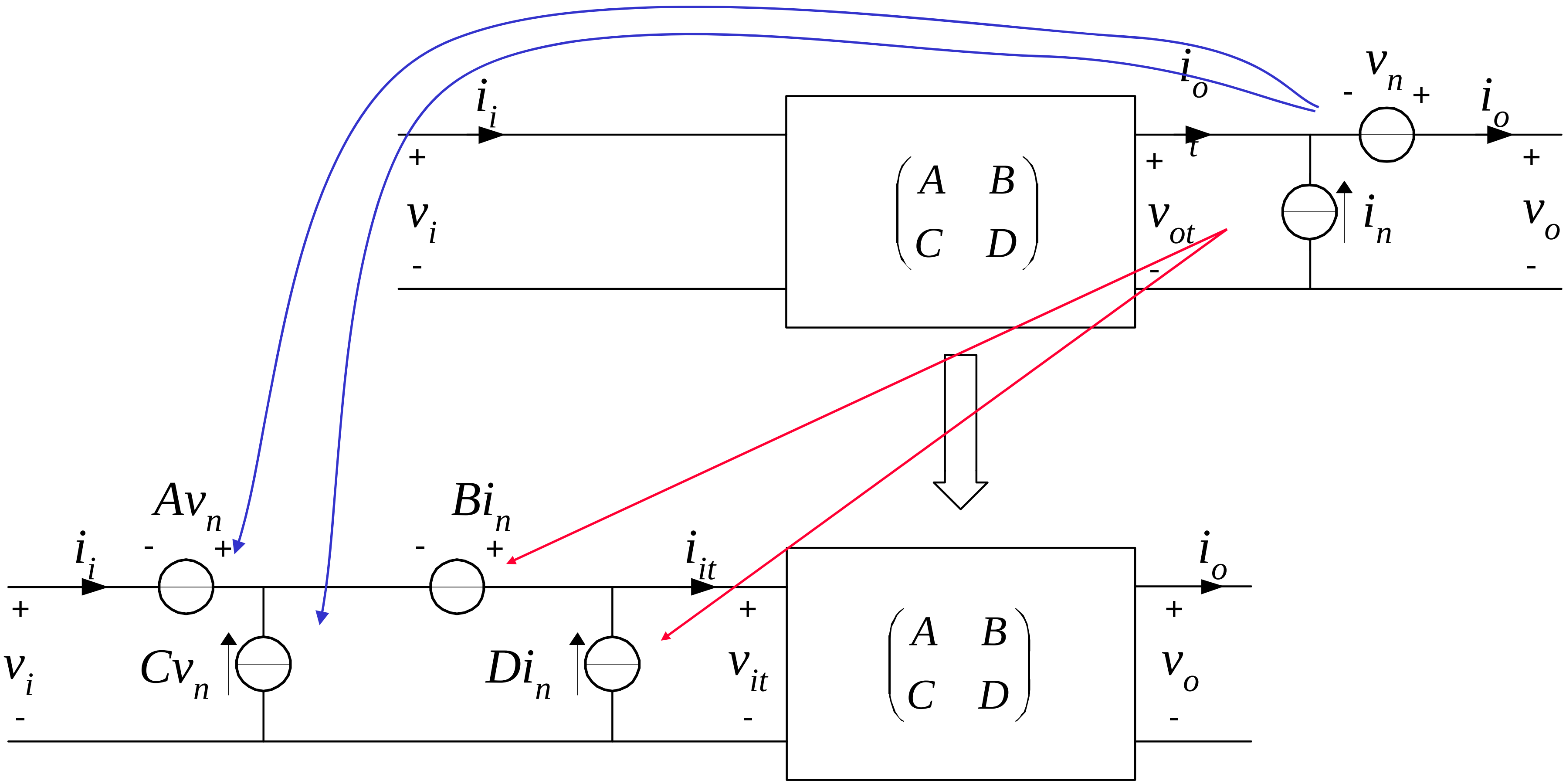


$$i_{n,1} = i_{n,2} = i_n$$

Norton-Thevenin transform



Shift through two-ports



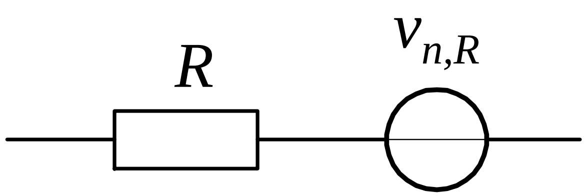
Procedure

1. **Identification** of noise sources : v_n, i_n
2. Determine **equivalent** noise source (input/output) : $v_{n,eq}$ or $i_{n,eq}$
3. Determine **power spectral density** of $v_{n,eq}$ / $i_{n,eq}$: $S_{n,eq}$
4. Determine **power** of $v_{n,eq}$ or $i_{n,eq}$: $P_{n,eq}$
5. **Minimize** noise power : $P_{optimal}$

1. Identification of noise sources

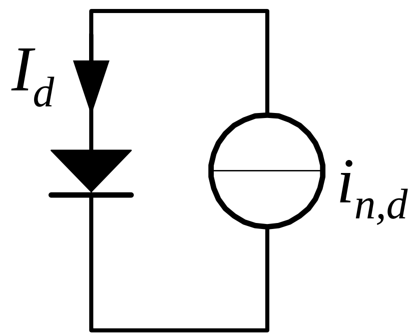
Noise due to quantized character of charge

- Thermal noise: due to collisions of carriers



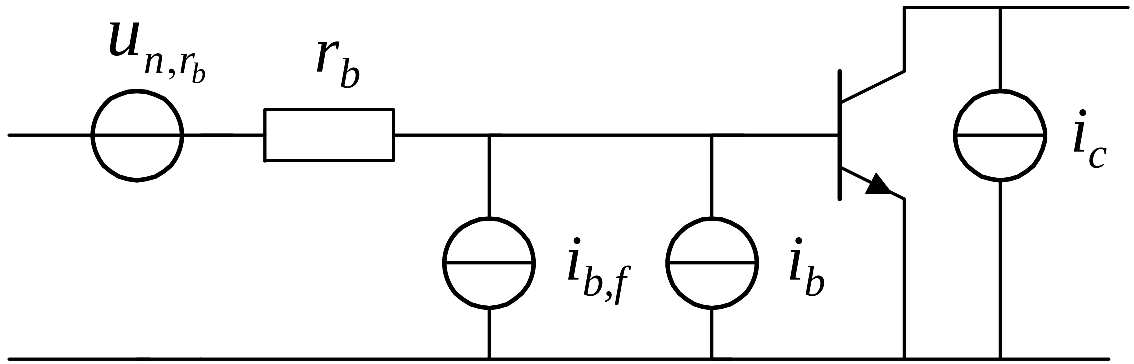
$$S_{v_{n,R}}(f) = 4kTR$$

- Shot noise: due to carriers crossing a junction



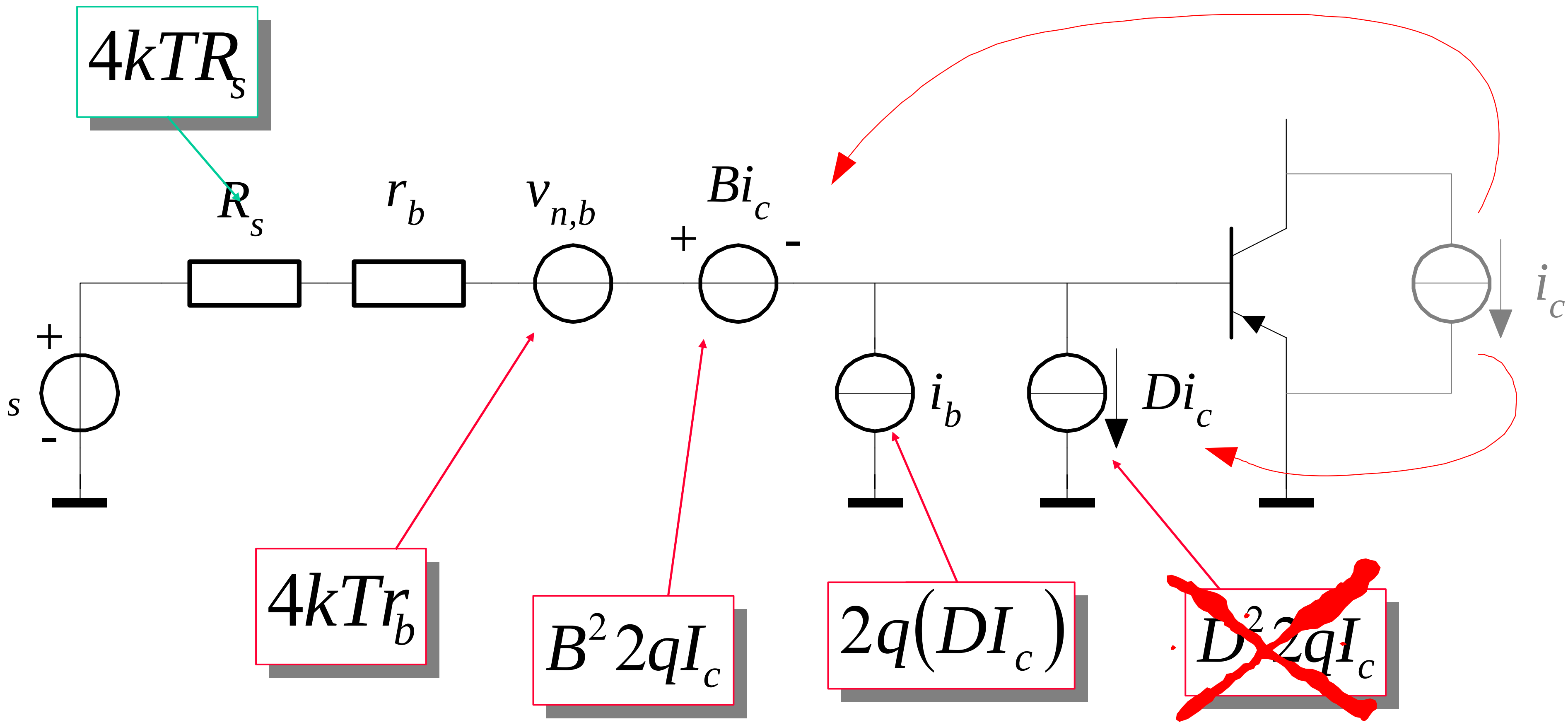
$$S_{i_{n,d}}(f) = 2qI_d$$

Bipolar transistor

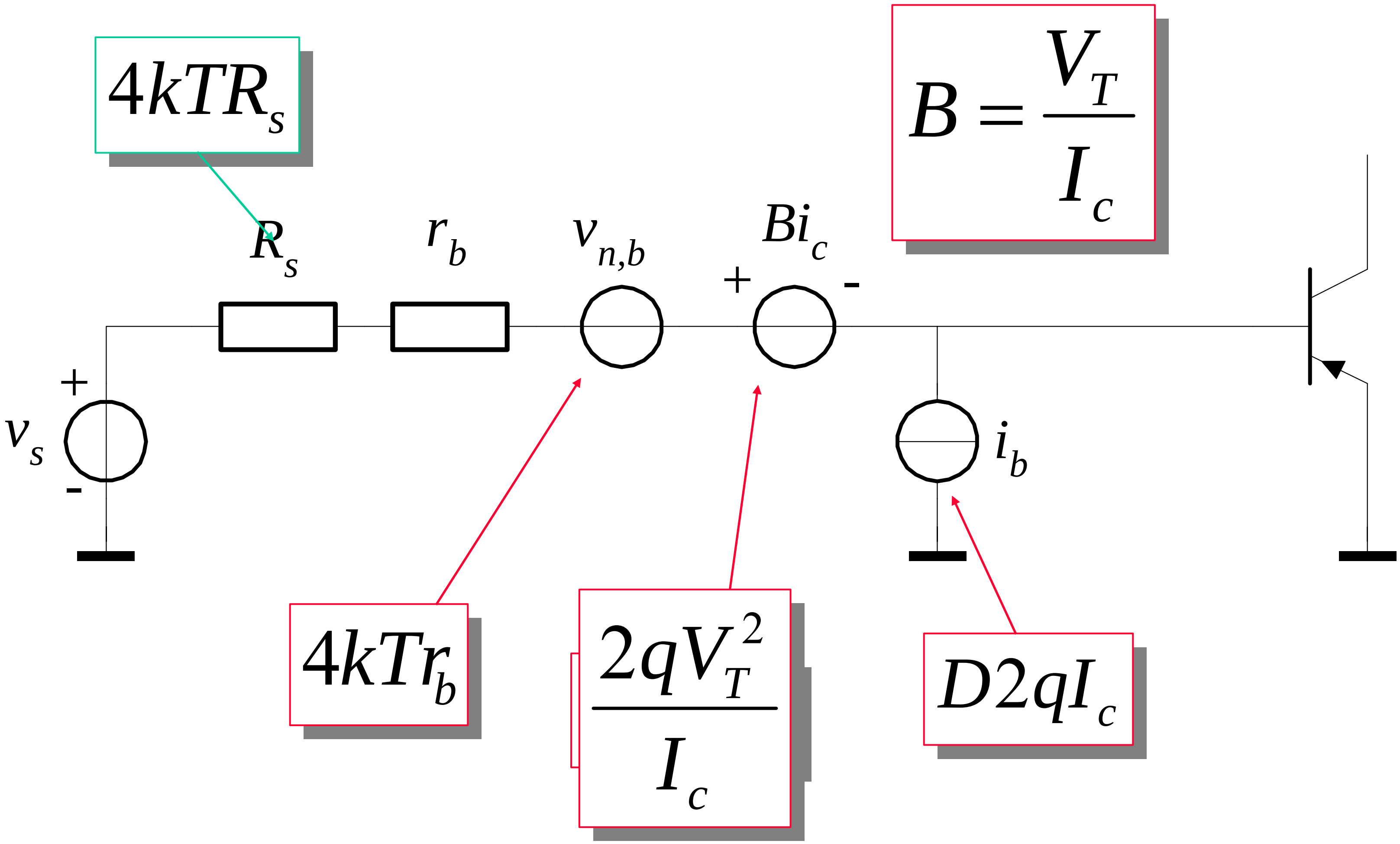


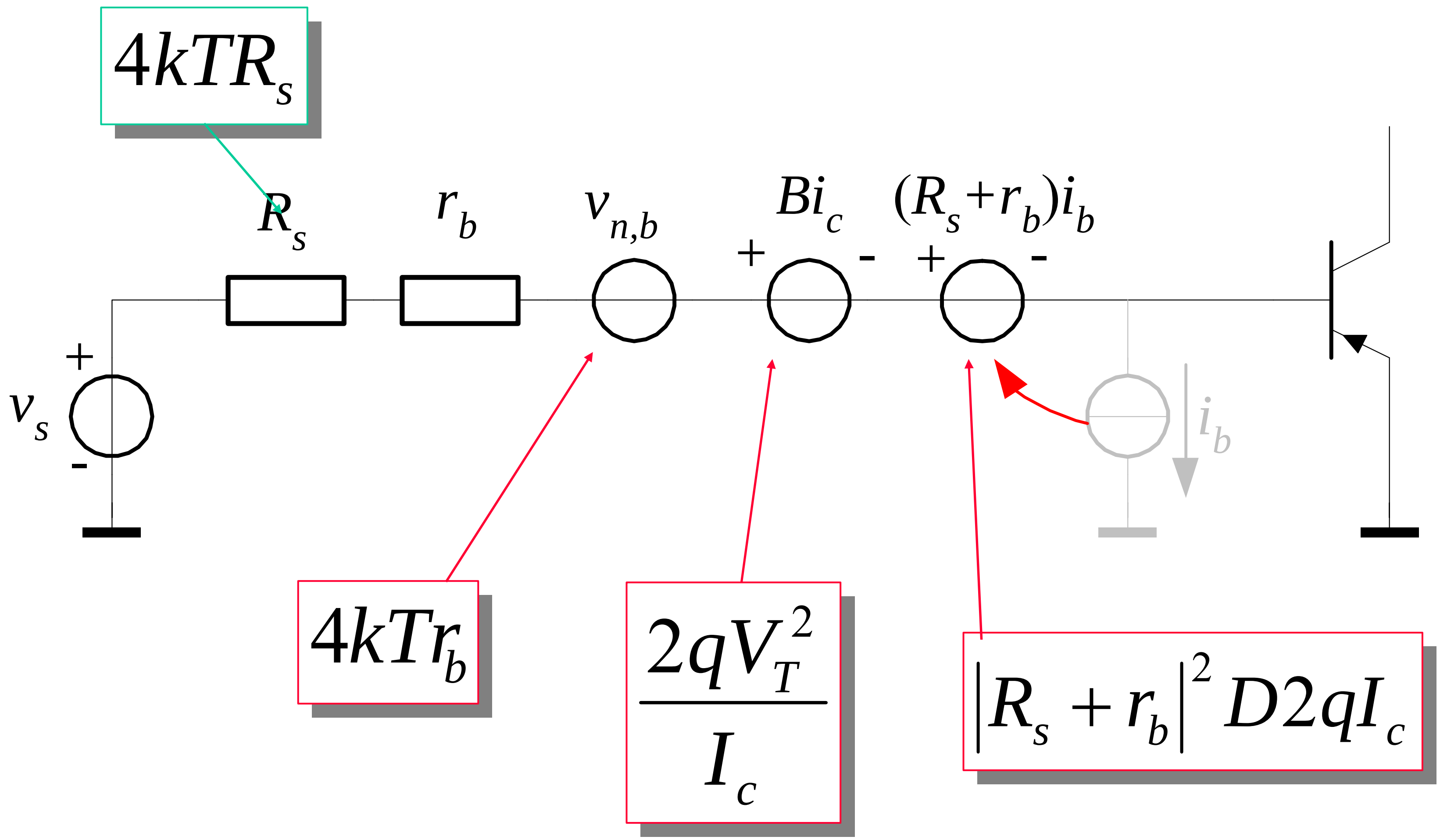
- thermal noise base resistance r_b $$S_{u_{n,r_b}}(f) = 4kTr_b$$
- shot noise collector-basis junction $$S_{i_c}(f) = 2qI_c$$
- shot noise base-emitter junction $$S_{i_b}(f) = 2qI_b$$
- *1/f* - noise base-emitter junction $$S_{i_{b,f}}(f) = 2qI_b \frac{f_l}{f}$$

2. Determination of equivalent source

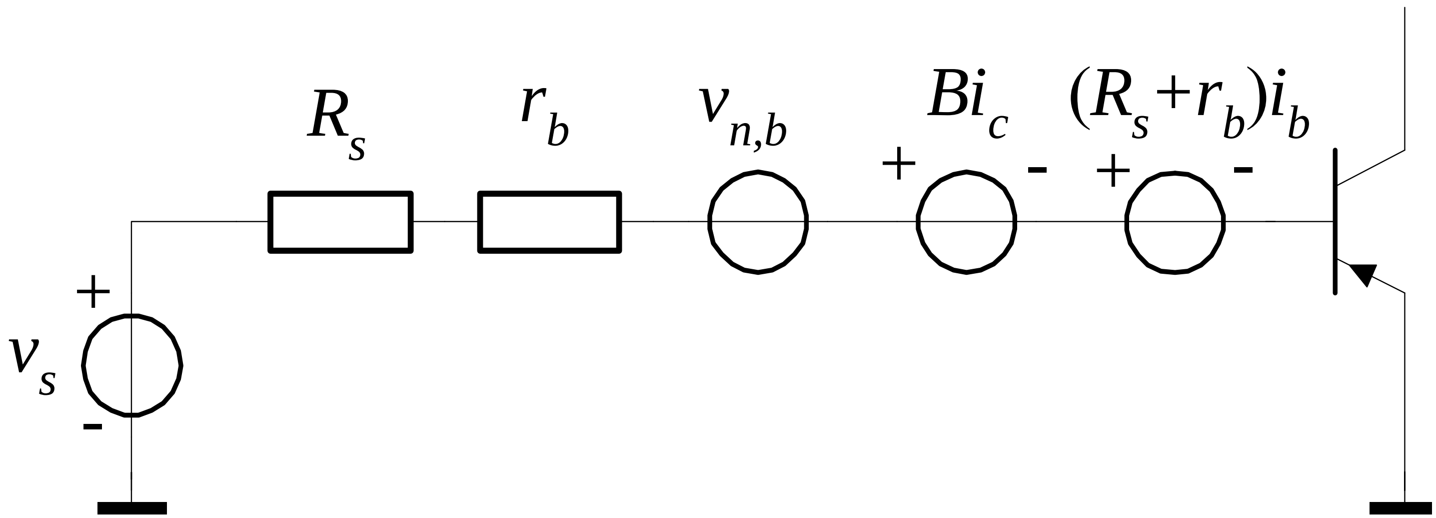


$$V_T = \frac{kT}{q}$$



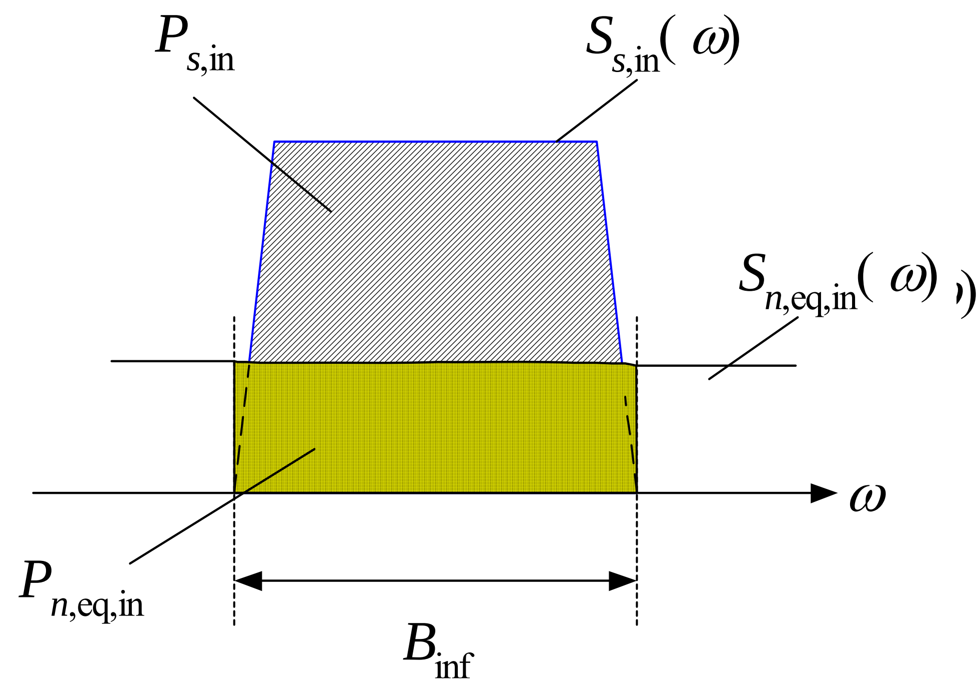


Power spectral densities!



$$4kTR_s + 4kTr_b + \frac{2qV_T^2}{I_c} + \left|R_s + r_b\right|^2 D2qI_c$$

Determine power of equivalent source



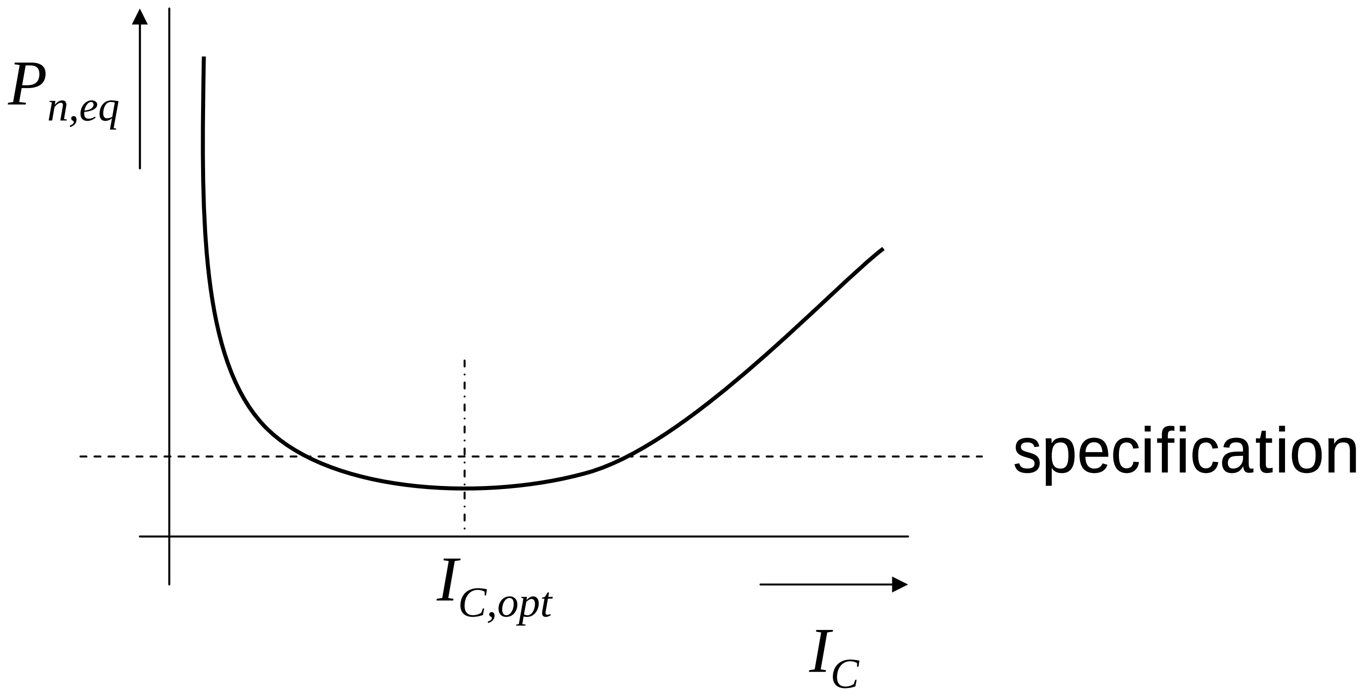
$$B_{\mathrm{inf}}\left(4kTR_s + 4kTr_b + \frac{2qV_T^2}{I_c} + \left|R_s + r_b\right|^2 D2qI_c\right)$$

Minimize noise power

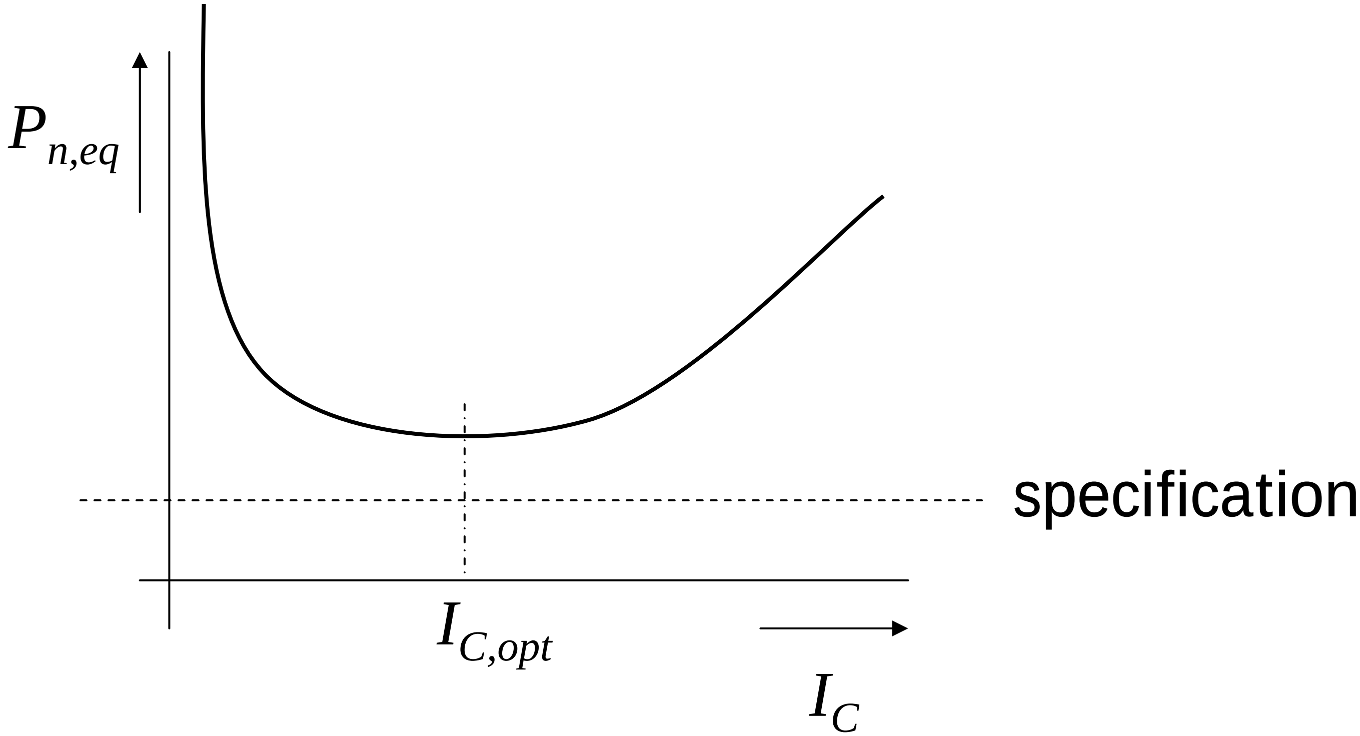
$$\frac{dP_{n,eq}}{dI_C} = 0 \Rightarrow I_{C,opt}$$

$$B_{\inf}\left(4kTR_s + 4kTr_b + \frac{2qV_T^2}{I_c} + \left|R_s + r_b\right|^2 D2qI_c\right)$$

$$I_{c,opt} = \frac{V_T}{\left(R_S + r_b\right)\sqrt{D}}$$

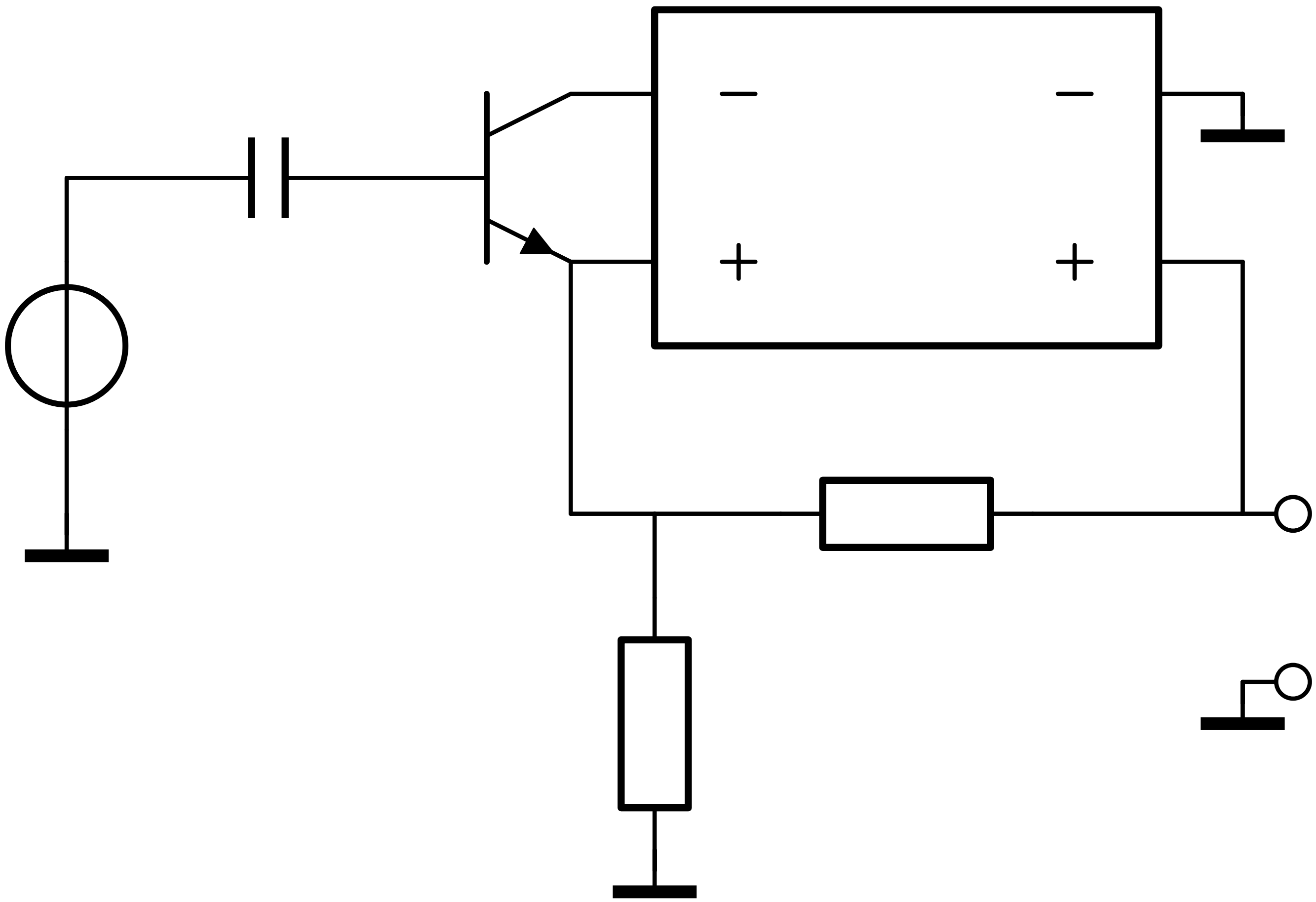


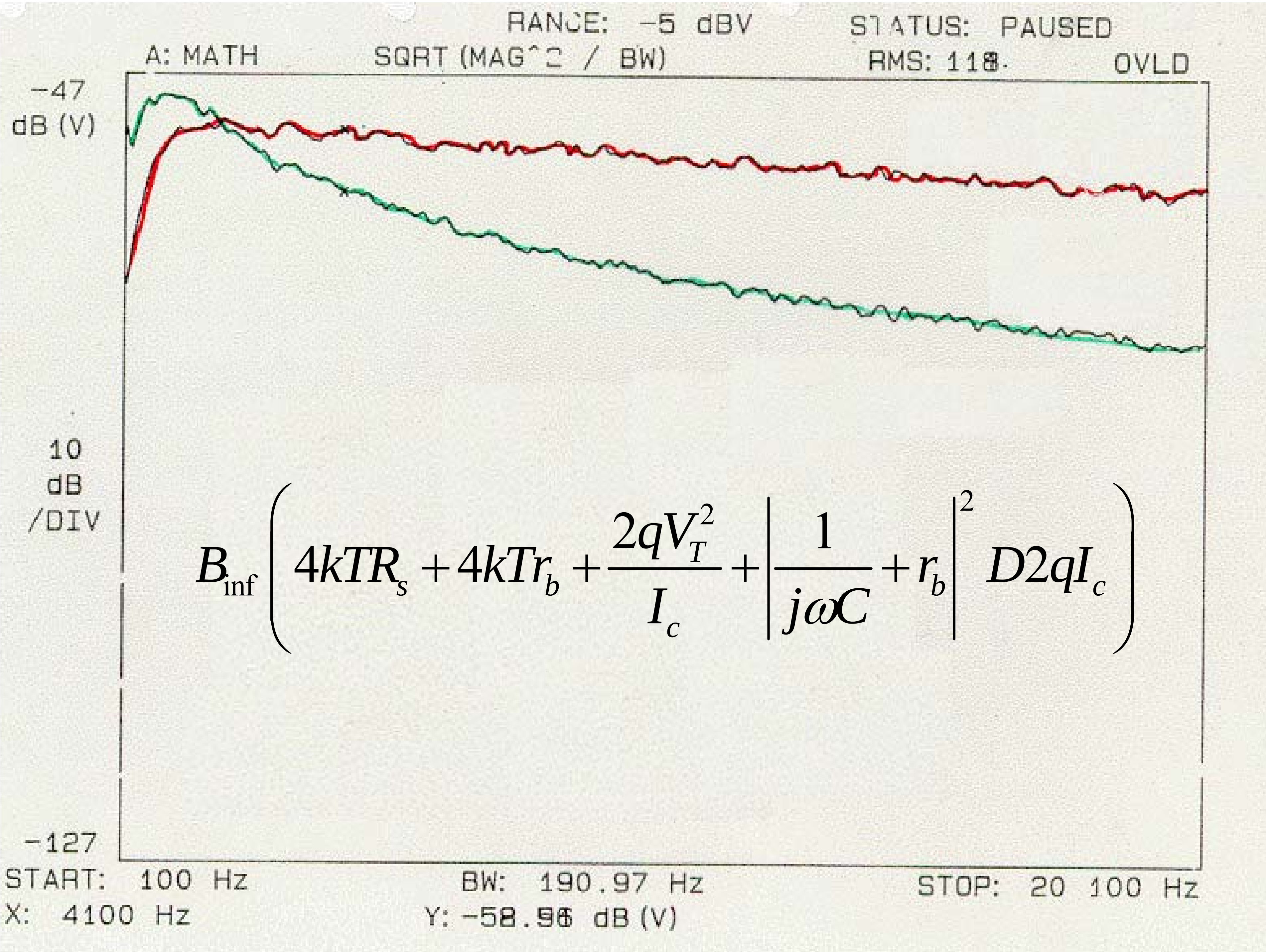
$$B_{\inf}\left(4kTR_s + 4kTr_b + \frac{2qV_T^2}{I_c} + \left|R_s + r_b\right|^2 D2qI_c\right)$$



$$B_{\inf}\left(4kTR_s + 4kTr_b + \frac{2qV_T^2}{I_c} + \left|R_s + r_b\right|^2 D2qI_c\right)$$

Demonstration with capacitive source





$$B_{\text{inf}}\left(4kTR_s + 4kTr_b + \frac{2qV_T^2}{I_c} + \left|\frac{1}{j\omega C} + r_b\right|^2 D2qI_c\right)$$

Conclusions

- All stages should have maximal gain (CE CS)
- First stage : noise behavior
- Last stage : clipping
- Most orthogonal order: N, S, B
- Negative feedback gives orthogonality
- Bias current of first stage can be optimized for noise performance without restriction