Structured Electronic Design

Building the nullor: Frequency behavior
Topology

Best nullor implementation

Voltage and current swing

Power consumption

Noise level : First stage (type, bias parameters)

Clipping level : Last stage (type, bias parameters)

Minimal loopgain necessary to suppress weak distortion
Bandwidth

All nullor stages large gain
First stage $\Rightarrow$ noise
Last stage $\Rightarrow$ clipping
Loopgain reduces weak distortion
What do we want?

An amplifier with the desired bandwidth

An amplifier with a “nice” frequency behavior

A simple bandwidth estimation method
An amplifier with the desired bandwidth

\[ C = B_{\text{inf}}^2 \log \frac{S + N}{N} \]
Usually a biasing problem

Bandwidth optimization

$B_{\text{inf}}$
“Nice” frequency behavior

All-pole Butterworth characteristic

\[ |H(f)|, \quad |H(0)| \]

\[ B_{inf}, \quad f, \quad f_n \]

\[ Re, \quad Im \]
Butterworth poles

$$H(s) = \frac{H(0)}{s^2 - s(p_a + p_b) + p_a p_b}$$

$$CP = s^2 - s(p_a + p_b) + f_n^2$$

Characteristic Polynomial

$$f_n^2 = p_a p_b$$
Bandwidth estimation

What will be the bandwidth in this case?
How many stages are needed?
Can the poles be in Butterworth position?
Which poles?
Frequency dependent loop gain

\[ A_t = A_{t\infty} \frac{-L(s)}{1 - L(s)} \]

\[ \text{CP} = 1 - L(s) \]
Amplifier with a "nice" frequency behavior

\[ A_t(s) = A_{t\infty} \frac{-L(s)}{1 - L(s)} \]
\[ A_t(s) = A_{t \infty} \frac{-L(s)}{1 - L(s)} \]

\[ L(s) = \frac{L(0)}{\left(1 - \frac{s}{p_1}\right)\left(1 - \frac{s}{p_2}\right)} - L(0) \]

\[ A_t(s) = A_{t \infty} \frac{-L(0)}{\left(1 - \frac{s}{p_1}\right)\left(1 - \frac{s}{p_2}\right) - L(0)} \]

\[ A_t(s) = A_{t \infty} \frac{-L(0)}{s^2 - s\left(\frac{1}{p_1} + \frac{1}{p_2}\right) + 1 - L(0)} \]

\[ CP(s) = s^2 - s(p_1 + p_2) + \left[1 - L(0)\right]p_1p_2 \]

\[ CP(s) = s^2 - s(p_a + p_b) + f_n^2 \]
LP -product: Bandwidth prediction

\[ CP(s) = s^2 - s(p_a + p_b) + f_n^2 \]

\[ CP(s) = s^2 - s(p_1 + p_2) + \left[ 1 - L(0) \right] p_1 p_2 \]

- If Butterworth position
- Then \([1-L(0)] p_1 p_2\) predicts the bandwidth

\[ f_n = \sqrt[n]{\left[ 1 - L(0) \right] \prod_1^n p_n} = \sqrt[n]{LP} \]
Synthesis rule

Maximum attainable bandwidth: \( B_{\text{max}} = \sqrt[n]{LP} \)

- \( B_{\text{max}} < B_{\text{spec}} \): Specification never reached

- \( B_{\text{max}} > B_{\text{spec}} \): Chance on success,

if the poles can be brought into Butterworth position

Enough LP-product is necessary but not sufficient
Determining the $LP$ -product

$\left[ 1 - L(0) \right] p_1 p_2$

Influence of feed back network?
Influence of source impedance?
Influence of load impedance?
Influence of the active part?
Modeling

A correct model gives a correct prediction

Never confuse models with “the truth”
A frequency dependent transistor model
Good enough?
The influence of the load impedance
Looks good...
The difference is in the zero
What if short circuit not good enough?
"Miller effect"

\[ v_{C_{\mu}} = v_{be} (1 + g_m R_{next}) \]

\[ i_{C_{\mu,\text{eff}}} = i_{C_{\mu,\text{normal}}} (1 + g_m R_{next}) \]

\[ C_{\mu_{\text{eff}}} = C_{\mu} (1 + g_m R_{next}) \]

\[ v_{out} = -v_{be} g_m R_{next} \]
Check with an ideal short circuit

\[ V_{be} \quad r_{\pi} = C_{\pi} \quad g_m v_{be} \quad r_o \]

\[ i_{in} \quad i_{out} \quad C_{\mu} \quad R_{next} \]

**IF** an ideal current follower solves the problem,

Insert a CB-stage (cascode).
Ideal current follower does not help

The zero is the cause

- Increase $V_{bc}$
- Replace transistor
- Elaborate compensation
Conclusions

• Use simple model, with assumption
  1. Current driven
  2. Output short circuited

Make this true (later)!

• 2 potential problems
  1. RHP zero
  2. Influence of $C_\mu$ and $r_o$ on the pole positions

Distinguish via ideal current follower
Contribution to the $LP$-product

$$CP(s) = s^2 - s(p_1 + p_2) + \left[1 - L(0)\right] p_1 p_2$$

\[ L: \quad g_m r_{\pi} = \beta_F = \frac{1}{D} \quad \text{and} \quad P: \quad \frac{1}{2\pi r_{\pi} C_{\pi}} \]

$$LP \approx \frac{g_m}{2\pi C_{\pi}} = f_T$$
Contribution to $LP$-product: $f_{T1}f_{T2}$
\[ f_n = \sqrt{\left[1 - L(0)\right]} p_1 p_2 \]

\[ LP = \frac{C_{\pi_1}}{C_s + C_{\pi_1}} f_{T_1} f_{T_2} \frac{R_L}{R_s + R_L} \]
First step: Realize sufficient $LP$-product

Realize: $B_{\text{max}} = n\sqrt{LP} > B_{\text{specified}}$

1. By adding stages
2. By changing the bias of an existing stage
Additional stages

\[ I_{bias} = I_{opt,fT} \]

- A CE/CS stage contributes \( f_T \) to the \( LP \) product
- Maximum \( f_T \) for minimum current

\[ LP \approx \frac{g_m}{2\pi C_\pi} = f_T \]
Maximum $f_T$ for minimum current,
AND....

$I_{bias} = I_{opt,fT}$

$I_{bias} > I_2(f_{max})$
Changing the bias of an existing stage

\[
B_{\text{inf}} \left(4kT R_s + 4kT r_b + \frac{2q V_T^2}{I_c} + \left| R_s + r_b \right|^2 D2qI_c \right)
\]

\[\text{Collector Current}\]

[Graph showing \(f_r\) vs. Collector Current]

[Graph showing \(P_{n,eq}\) vs. Collector Current]
Making a good prediction

• Must every pole be taken into account?
  – Dominant poles
• What is $L(\theta)$ exactly?
  – “DC” loop gain

Our definition:
A dominant pole is a pole that can be brought into Butterworth position.
Dominant poles

- If Butterworth position

- Then \([1-L(0)] p_1 p_2\) predicts the bandwidth

\[
CP(s) = s^2 - s(p_a + p_b) + f_n^2
\]

OK

Will *never* work

Butterworth is possible

(via frequency compensation)
Dominant poles

\[ \sum_{i=1}^{n} p_{i,\text{loop}} \geq \sum_{i=1}^{n} p_{i,\text{system}} \]

**Procedure:**
- Determine LP-product
- Sum of loop poles
- Sum of system poles
- Compare
- Reduce order?
"DC" loop gain

\[ L(0) = 0 \]

Charge amplifier

\[ |L| \]

\[ z_1 \quad p_1 \quad p_2 \quad p_3 \quad f \]
“DC” loop gain

\[ R = \frac{C_\pi r_\pi}{C_f} \]
Conclusions

• LP product predicts maximum attainable bandwidth
• Use dominant poles (and simple models)
• Pole and zero positions are still undefined

• When the LP product is too low, the design will never reach the required bandwidth

• A transistor contributes $f_T$ to the LP product
• General LP product: $LP = \beta_i \beta_o \beta_T f_{T1} f_{T2} f_{T3}$
Frequency compensation

\[ v_{be} \uparrow r_{\pi} = C_{\pi} \downarrow g_m v_{be} \]

- First use the **simple** model
  - No \( r_o \), \( C_\mu \), and \( r_o \)

- Refine models after successful compensation

- \( LP \) product gives maximum bandwidth

\[ CP = s^n + a_{n-1}s^{n-1} + a_{n-2}s^{n-2} + \ldots + LP \]
Frequency compensation methods

Resistive broad-banding
  Change loop pole position

Pole-zero cancellation
  Change loop pole position

Pole splitting
  Change loop pole position

Phantom zero
  Change root locus
Phantom zero

\[ A_t = A_{t\infty} \frac{-L(S)}{1 - L(S)} \]

\[ A_{t\infty}(s) = \frac{1}{\beta \left( \frac{s}{n_{ph}} + 1 \right)} \]

Make a zero \( n_{ph} \) in the feedback network

\[ L(s)_{new} = L(s)_{old} \left( \frac{s}{n_{ph}} + 1 \right) \]

\[ A_t = A_{t\infty} \frac{-L(S)_{old}}{1 - L(S)_{old} \left( \frac{s}{n_{ph}} + 1 \right)} \]

Zero appears in the loop
Zero does not appear in the transfer
Pole not dominant (should not be)
Phantom zero

- In feedback network
- \textit{Increases} the loop gain for high frequencies
- Extra pole not dominant

\[ L(s) \uparrow \delta \]

\[ n_{ph} \quad \rho = \delta n \]
Increase loop gain for high frequencies

Extra’s:
- Reduces distortion at high frequencies
- Sometimes possible at input or output

(when source or load impedance have influence 😏)
Demonstration
The other methods

\[ A_t = A_{t\infty} \frac{-L(s)}{1 - L(s)} \]

\[ A_{t\infty} = \frac{1}{\beta} \]

\[ L(s) = A(s) \beta \]

- Pole splitting
- Pole zero cancellation
- Resistive broad-banding

Change frequency behavior of active circuit (with a passive component)
Pole splitting

More *local* loopgain for high frequencies
- Input impedance goes down
  - higher input capacitance (*miller*)
  - input pole goes down
- Output impedance goes down
  - output pole goes up
Pole splitting

Less overall loopgain:
• Lower \( LP \)-product
• More distortion
• Introduces a zero
• Reduced accuracy
Pole-zero cancellation

Loopgain is reduced for high frequencies
- More distortion, etc.
Does not introduce a zero
Resistive broad-band"ing

Overall loopgain is reduced even at low frequencies
• Much more distortion
Does not introduce a zero
After successful frequency compensation
Add $c_\mu$ and $r_\omega$ one by one

- Insert CB-stage (cascode)
- Increase $V_{bc}$
- Replace transistor
- Elaborate compensation
Conclusions

• Start with **simple** model

• Create sufficient $LP$-product with dominant poles

• Do a frequency compensation
  Preferably with a phantom zero

• Insert $r_o$ and $C_\mu$ one by one

• Insert ideal current follower if necessary

• Reduce $C_\mu$ if necessary (deal with zero)

• Replace ideal current followers by CB-stages

Compensation results remains valid
Next time: batteries and real transistors