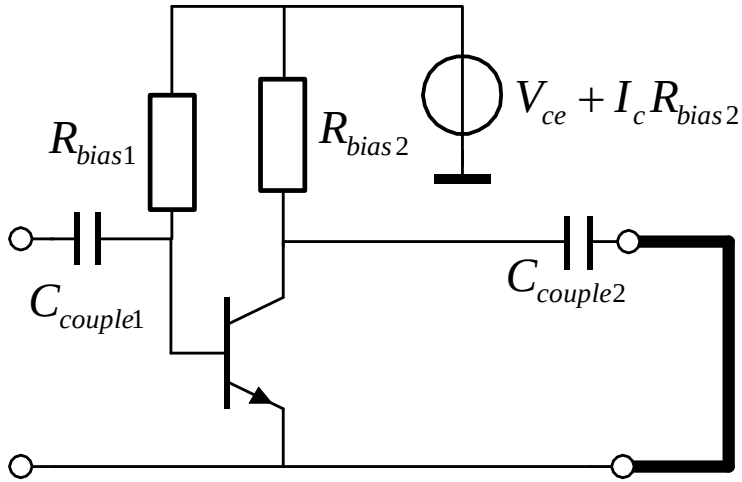
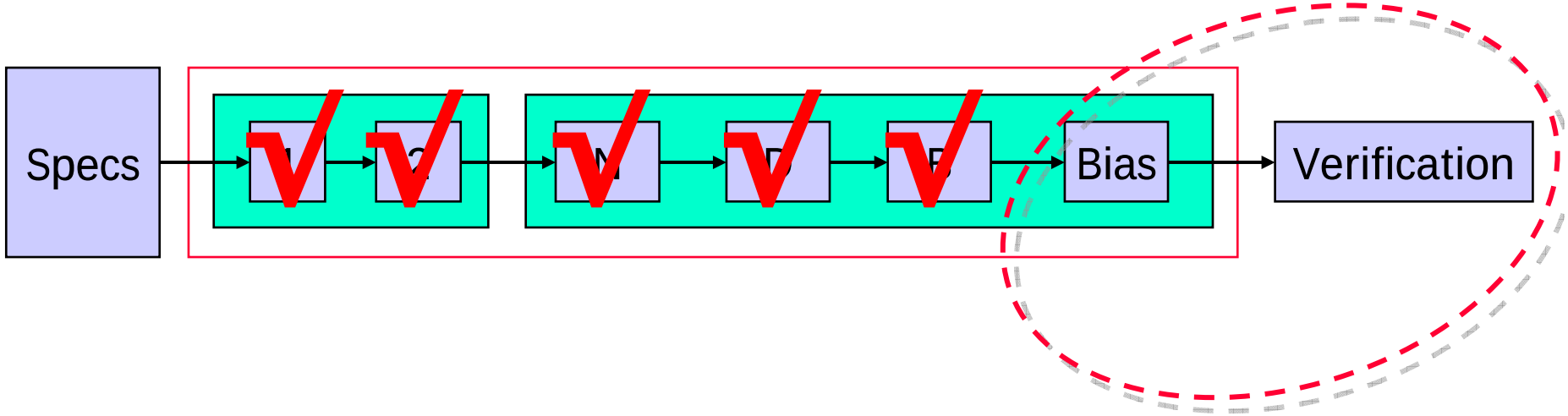
Structured Electronic Design

Building the nullor: **Biasing**

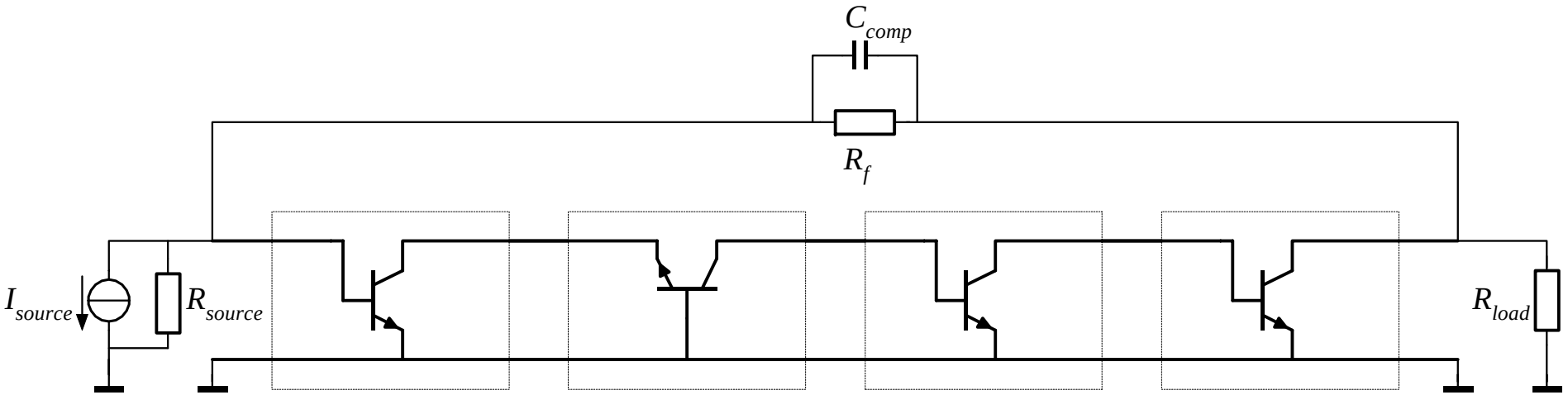


Today



- Biasing
- Verification (simulation)

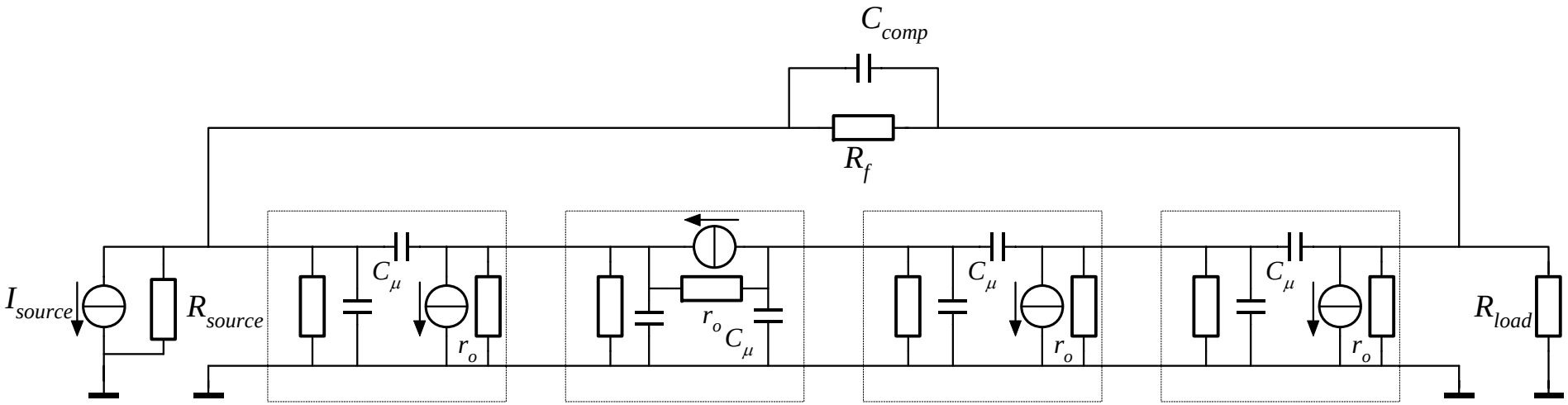
"At the end" of small-signal design



I_c =... V_c=...	I_c =... V_c=...	I_c =... V_c=...	I_c =... V_c=...
noise	model simplification	***LP***-product	clipping

Bias quantities are just **parameters**

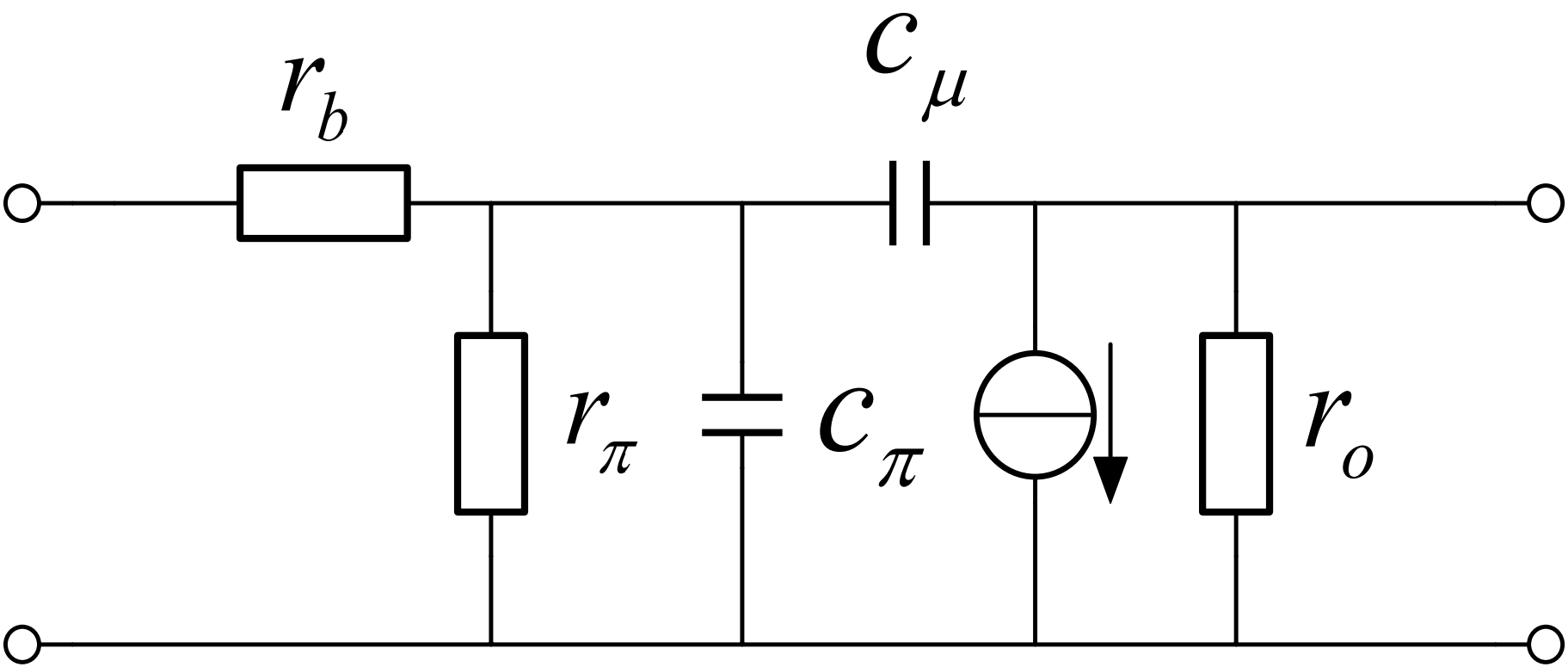
"At the end" of small-signal design



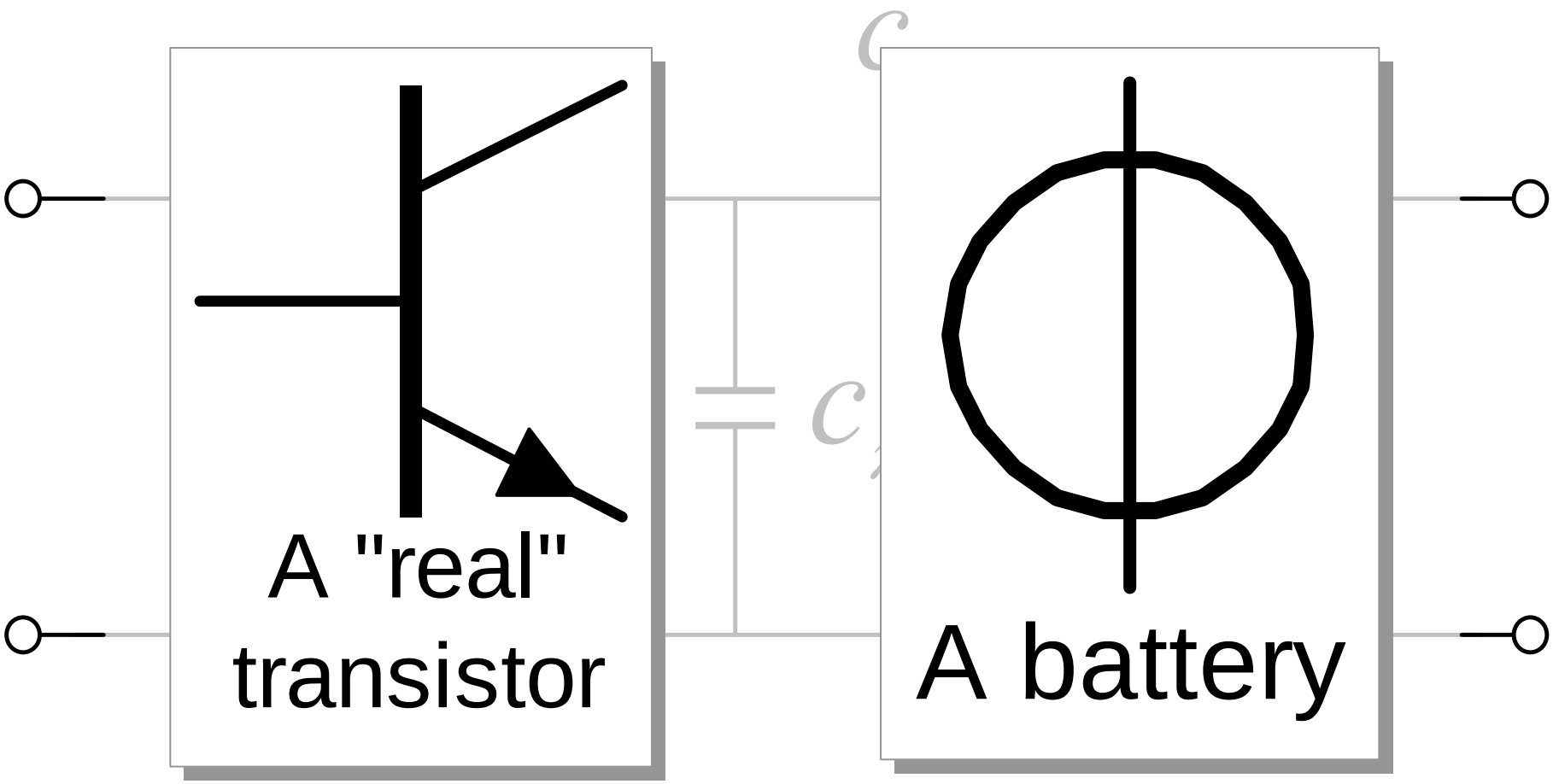
I_c =... V_c=...	I_c =... V_c=...	I_c =... V_c=...	I_c =... V_c=...
noise	model simplification	***LP***-product	clipping

Bias quantities are just **parameters**

The small-signal model

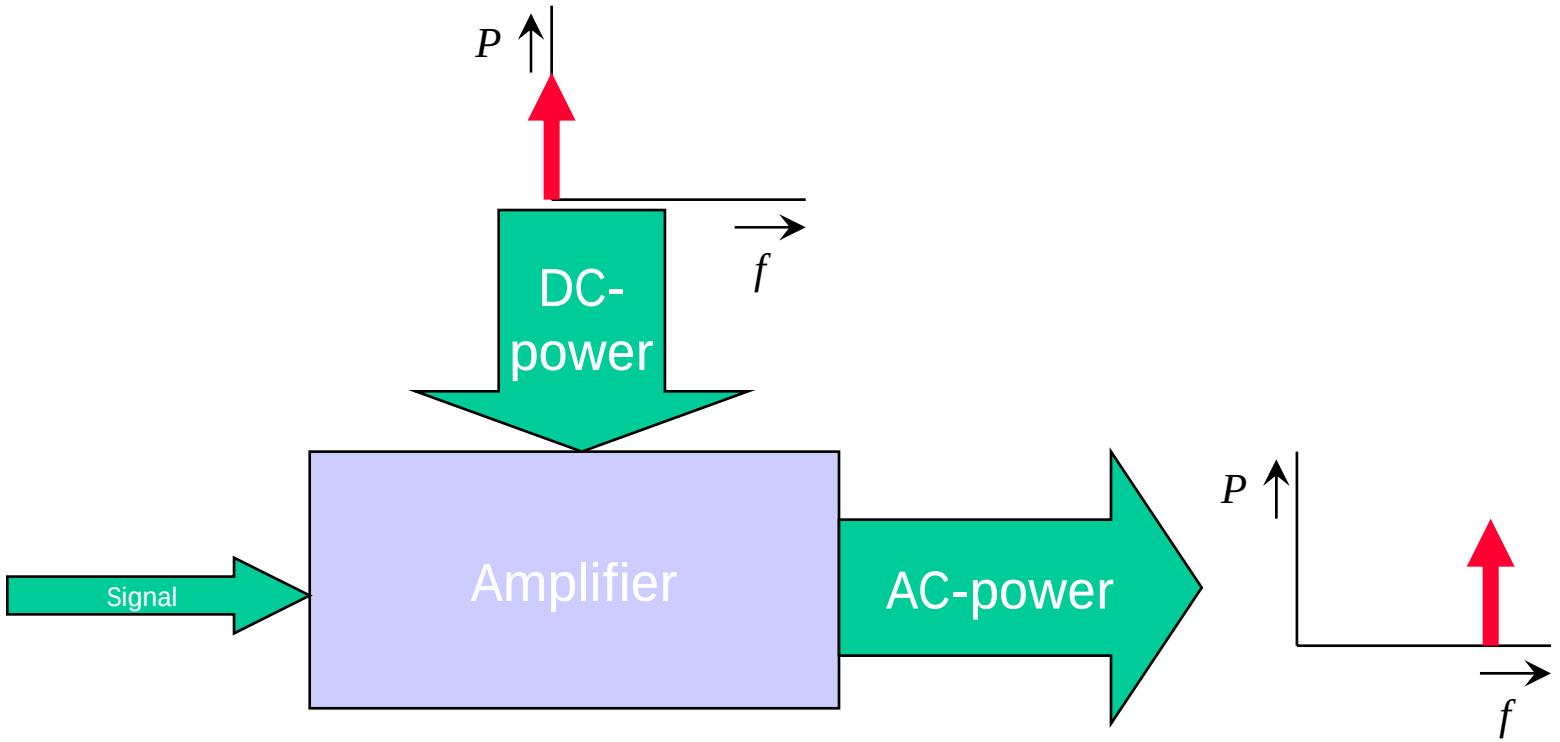


"Inside" de small-signal model

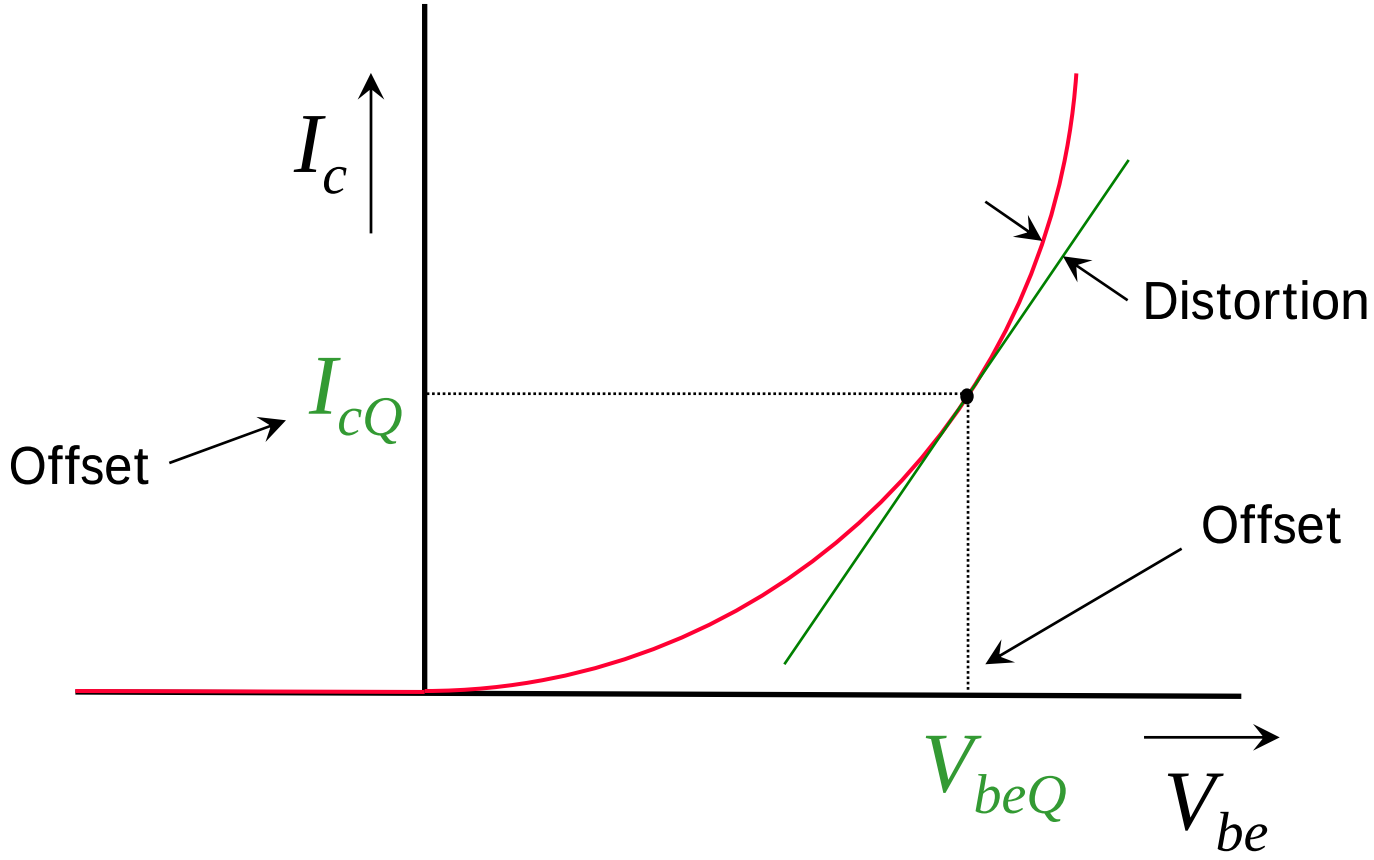


Conclusion

When only DC energy sources exist,
a non-linear element is needed for amplification

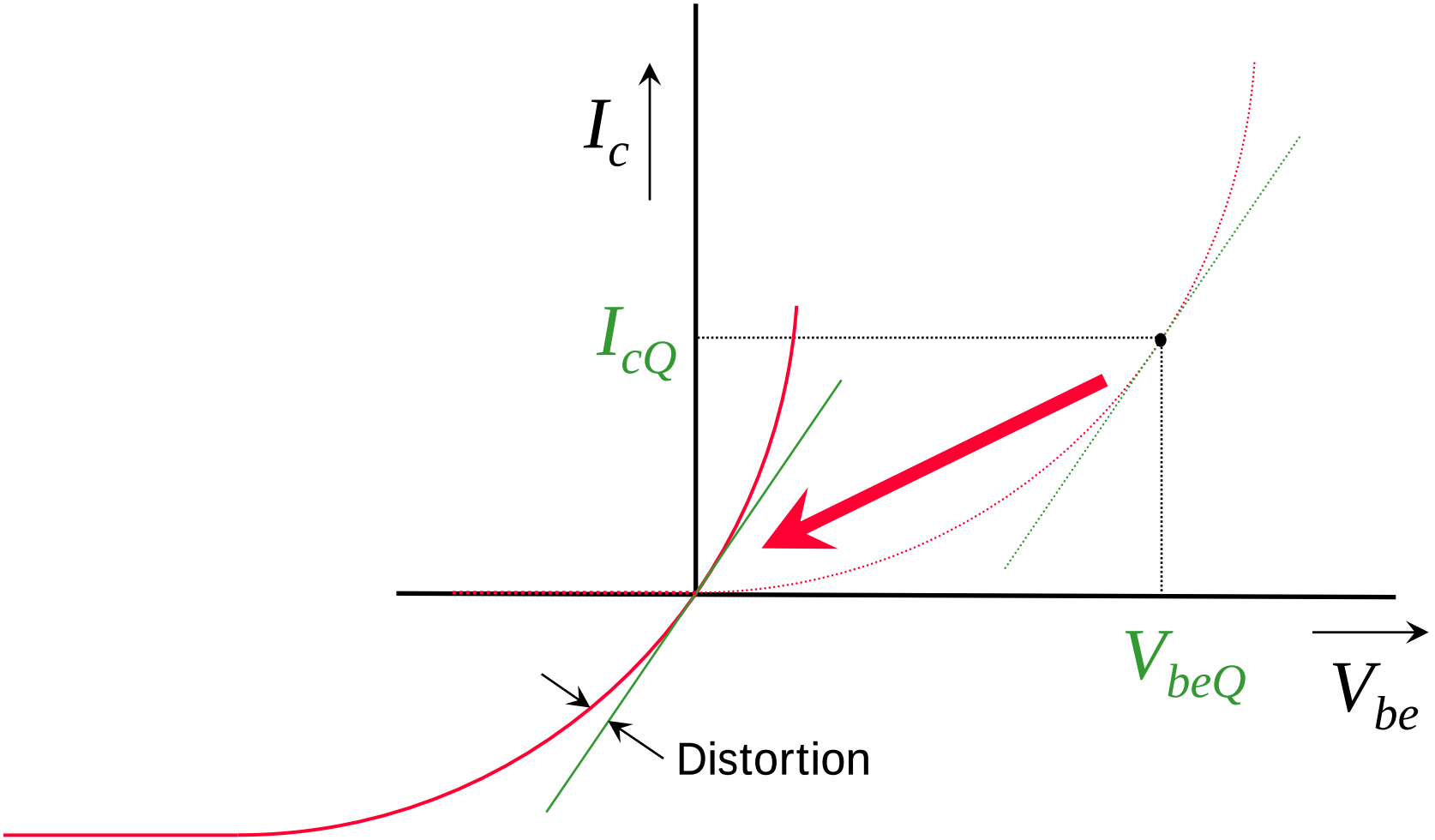


Using the non-linear element

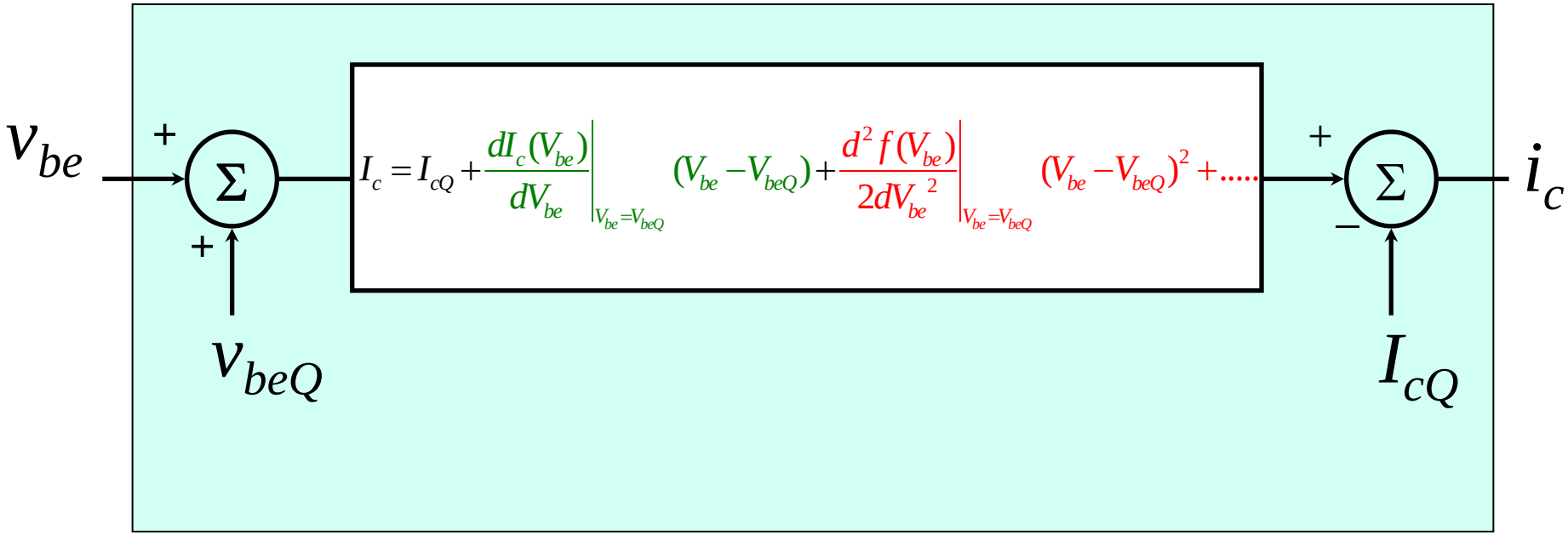


$$I_c = I_{cQ} + \left.\frac{dI_c(V_{be})}{dV_{be}}\right|_{V_{be}=V_{beQ}} (V_{be} - V_{beQ}) + \left.\frac{d^2 f(V_{be})}{2dV_{be}^{\ 2}}\right|_{V_{be}=V_{beQ}} (V_{be} - V_{beQ})^2 + \ldots..$$

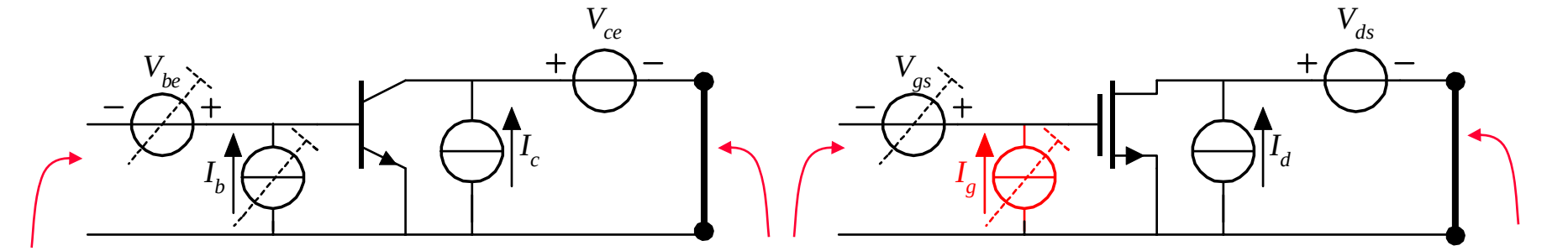
Biasing is translation to the origin



Adding and subtracting offsets



Translation (bias) sources



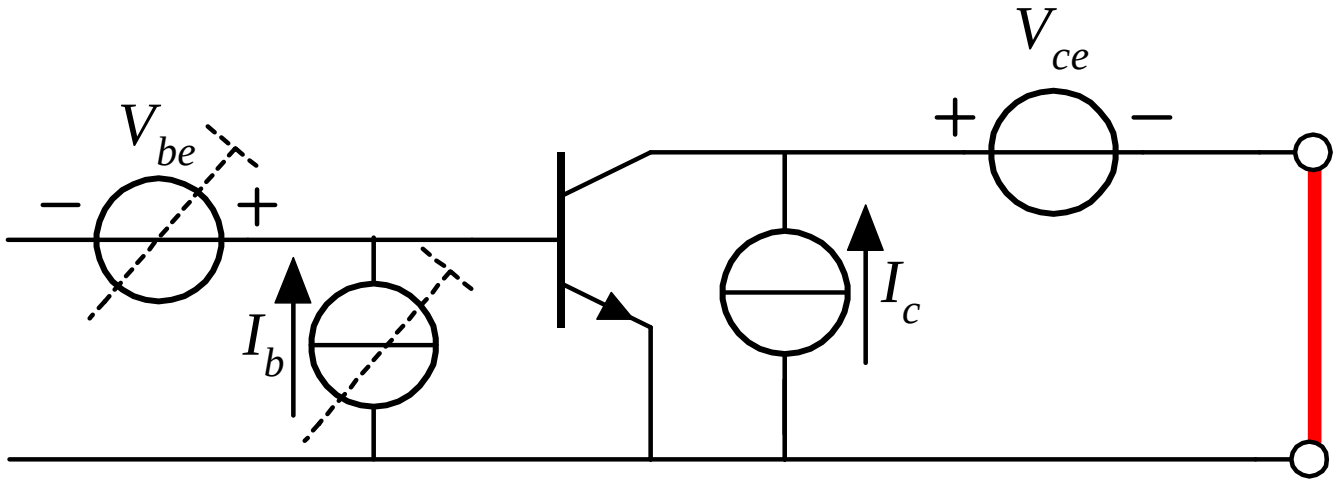
2 independent sources

2 sources need control

$I_{c,d}$ and $V_{ce,ds}$ independent

Boundary conditions

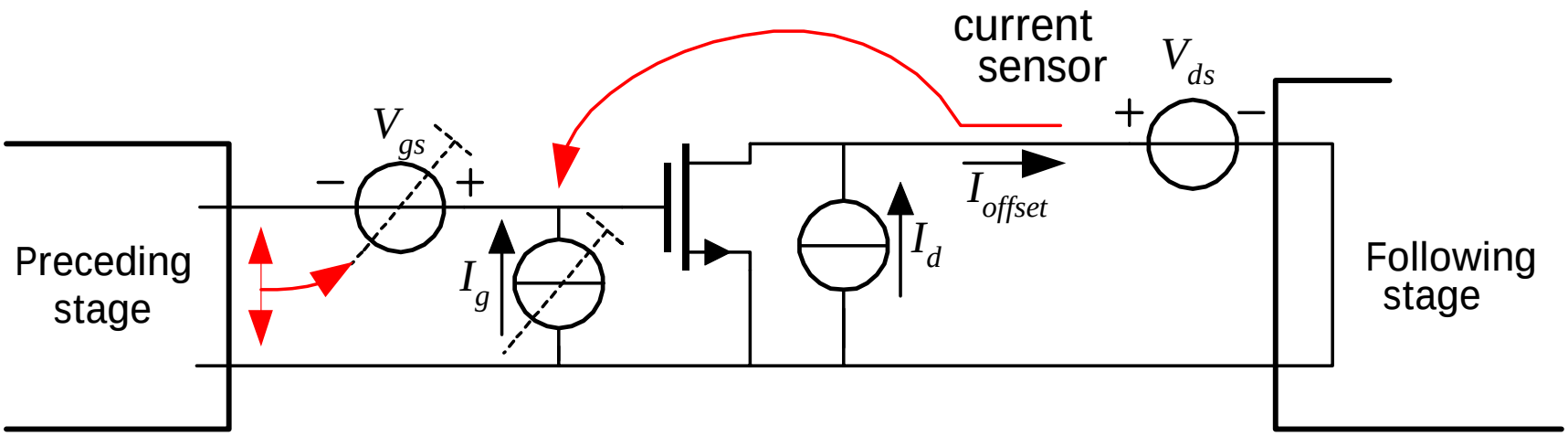
Output voltage **not** enforced internally.
(Device is a current source)



Following stage acts as short-circuit (usually)

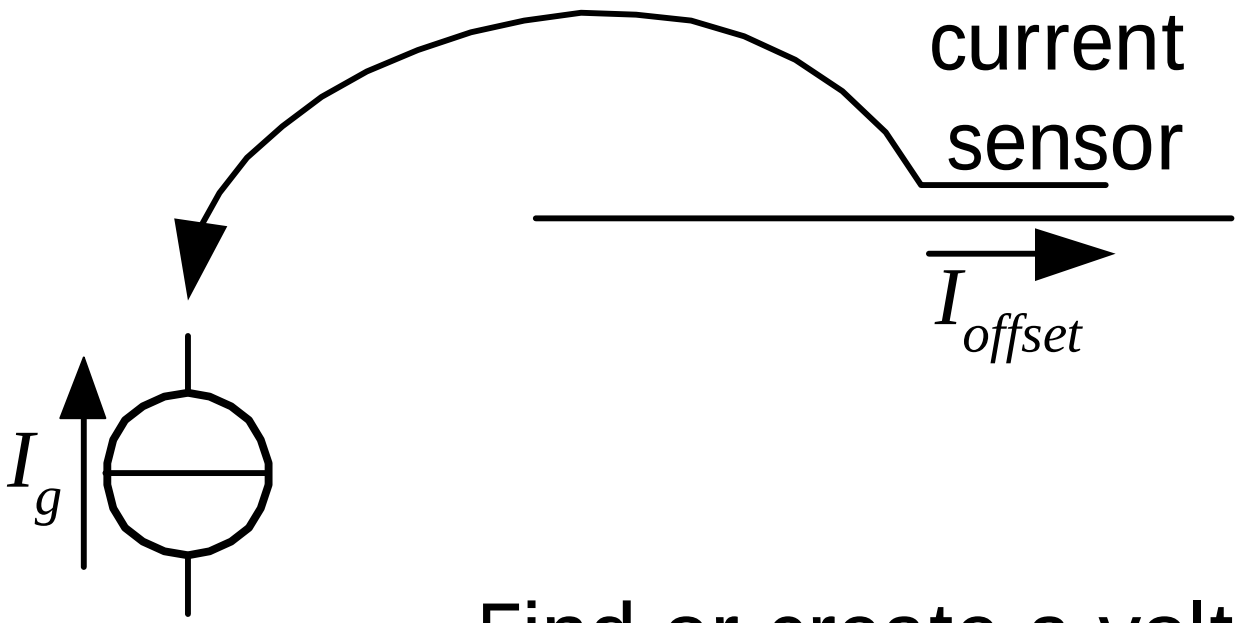
Preceding stage is an open-circuit (usually)

Implementation of the control



The loops need a **loop filter**
but we will deal with that later

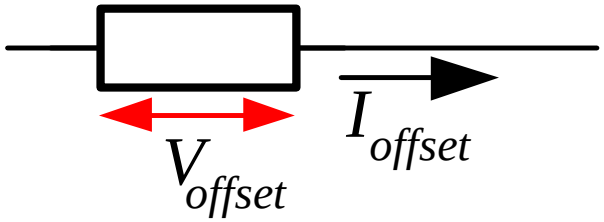
The current sensor

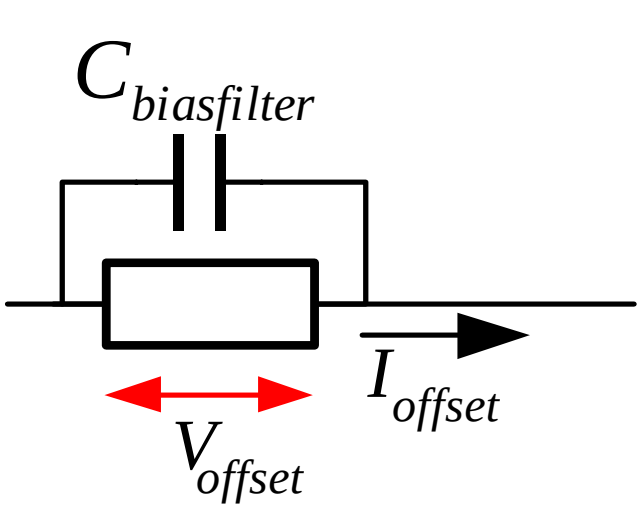


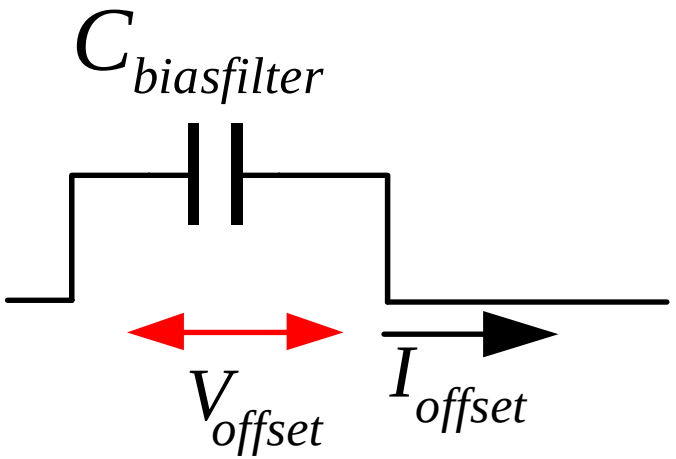
Find or create a voltage

Measure the voltage

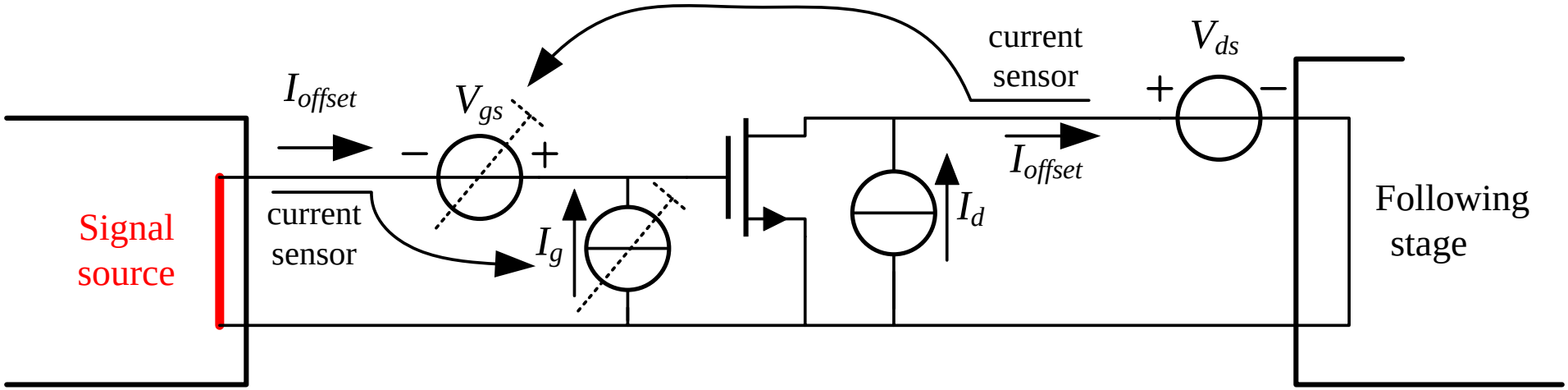
“Poor mans” current sensor



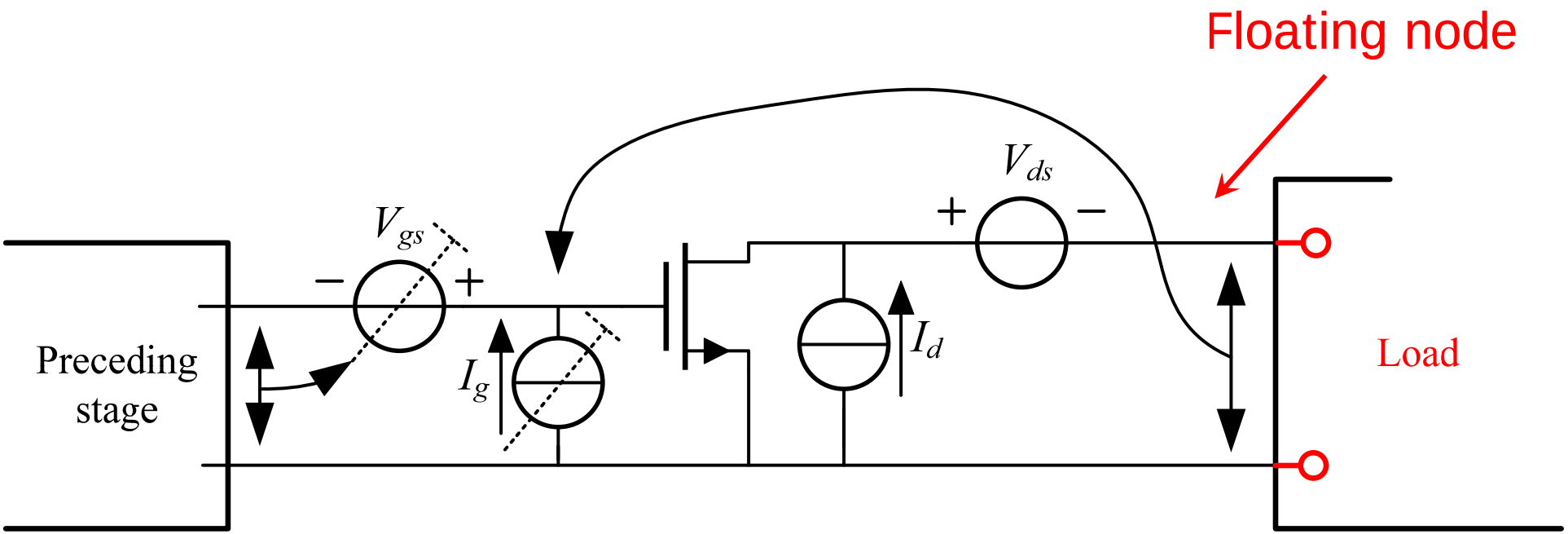




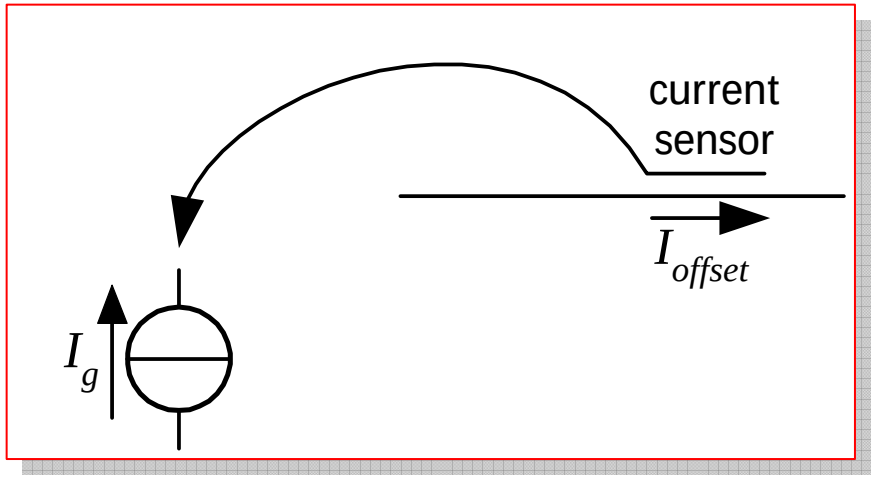
Special case at input

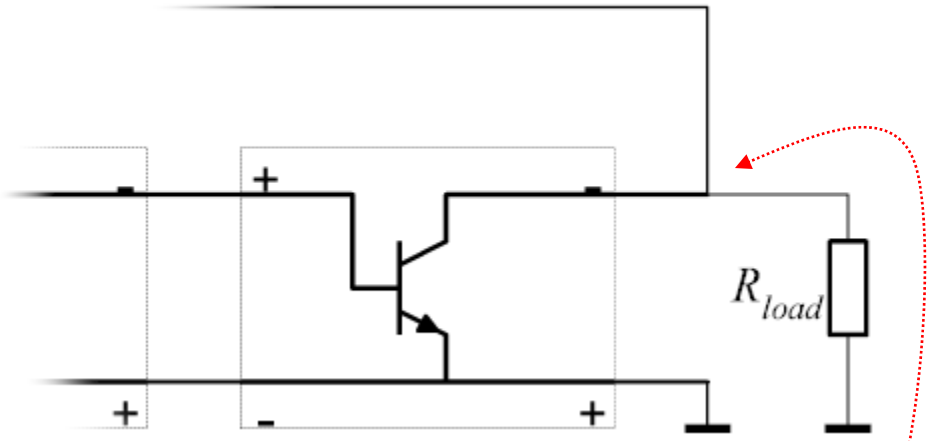


Special case at output



Floating nodes can be very useful

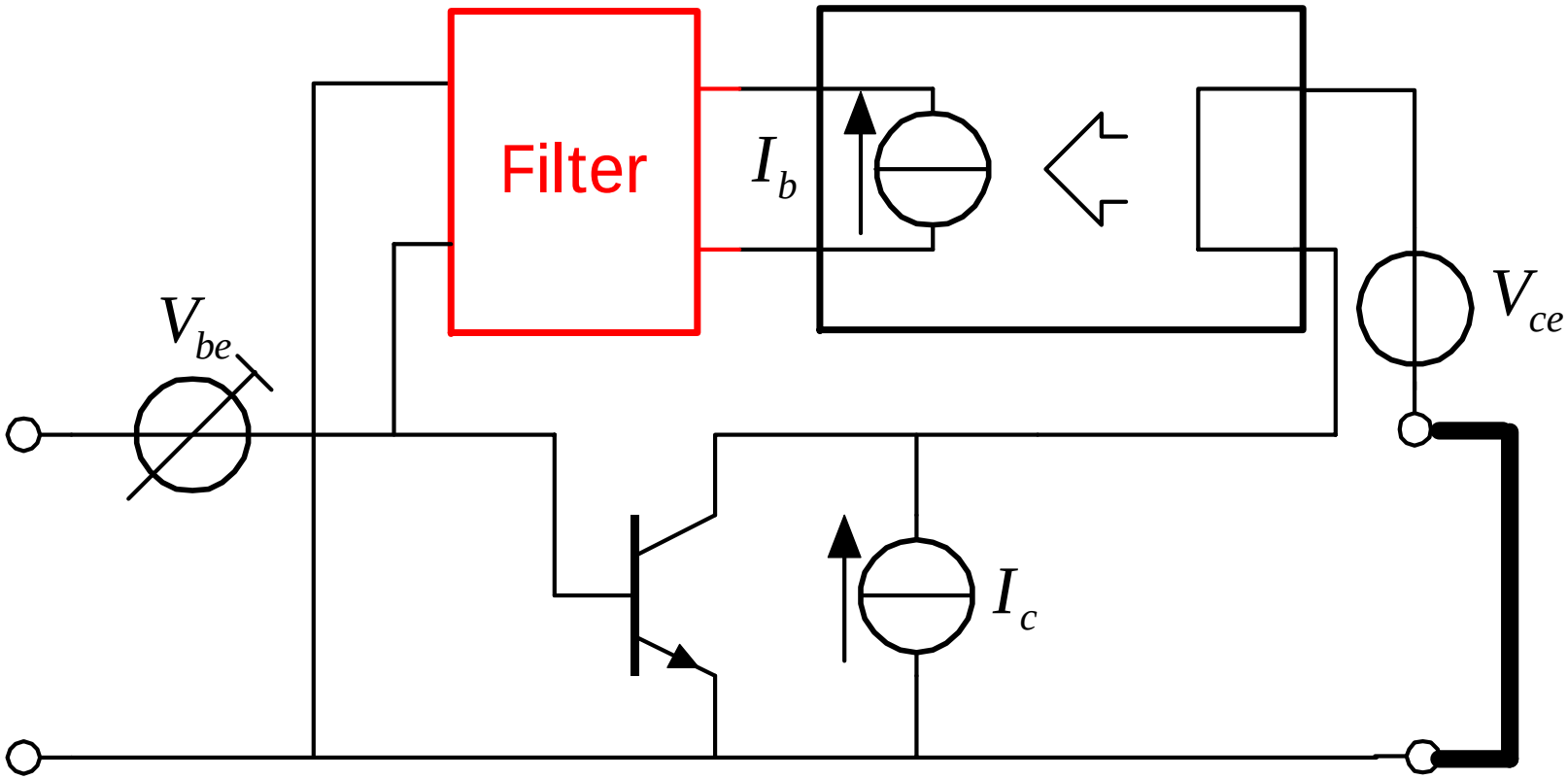




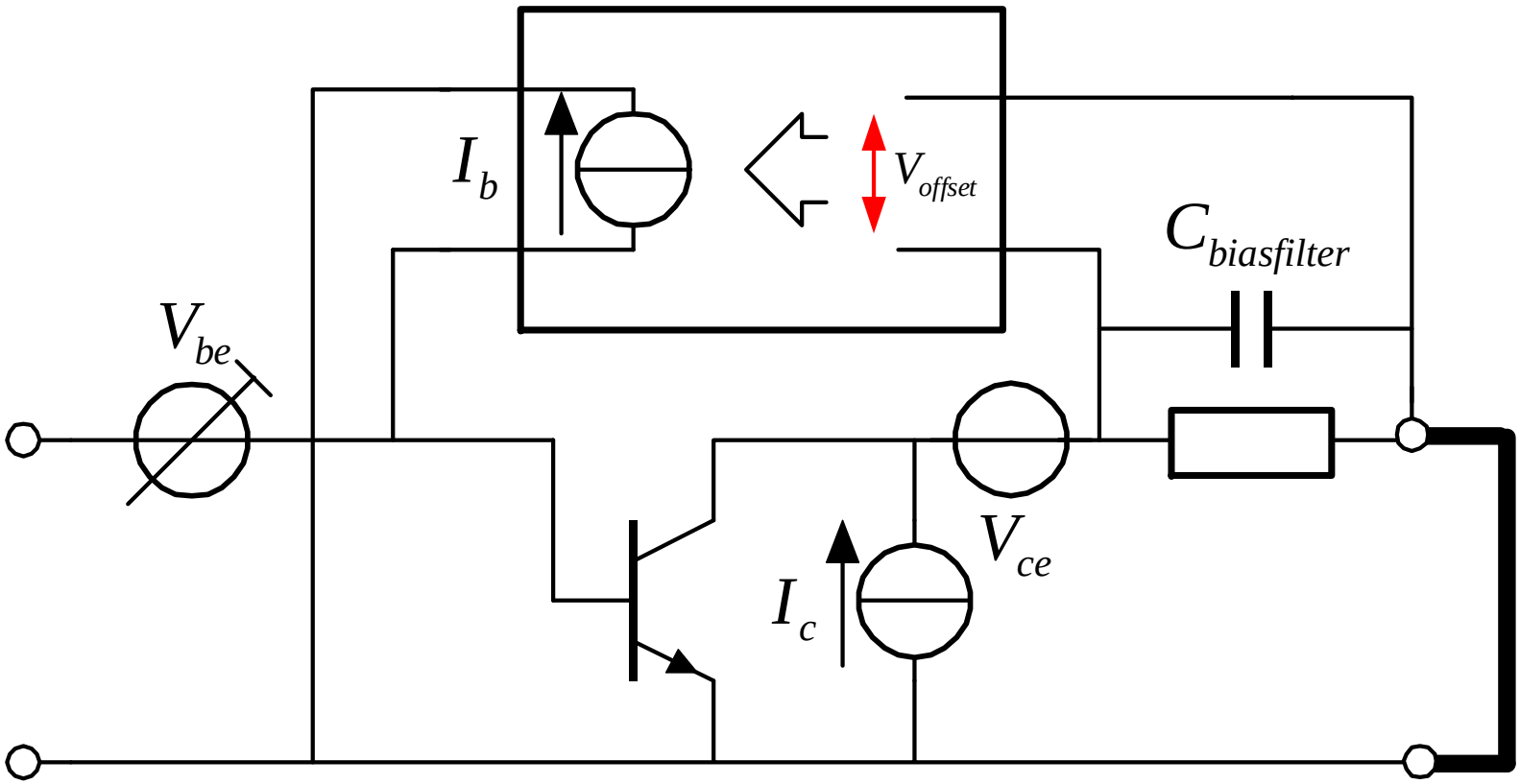
Current sensitive voltage

"Free" implementation of a **current sensor**

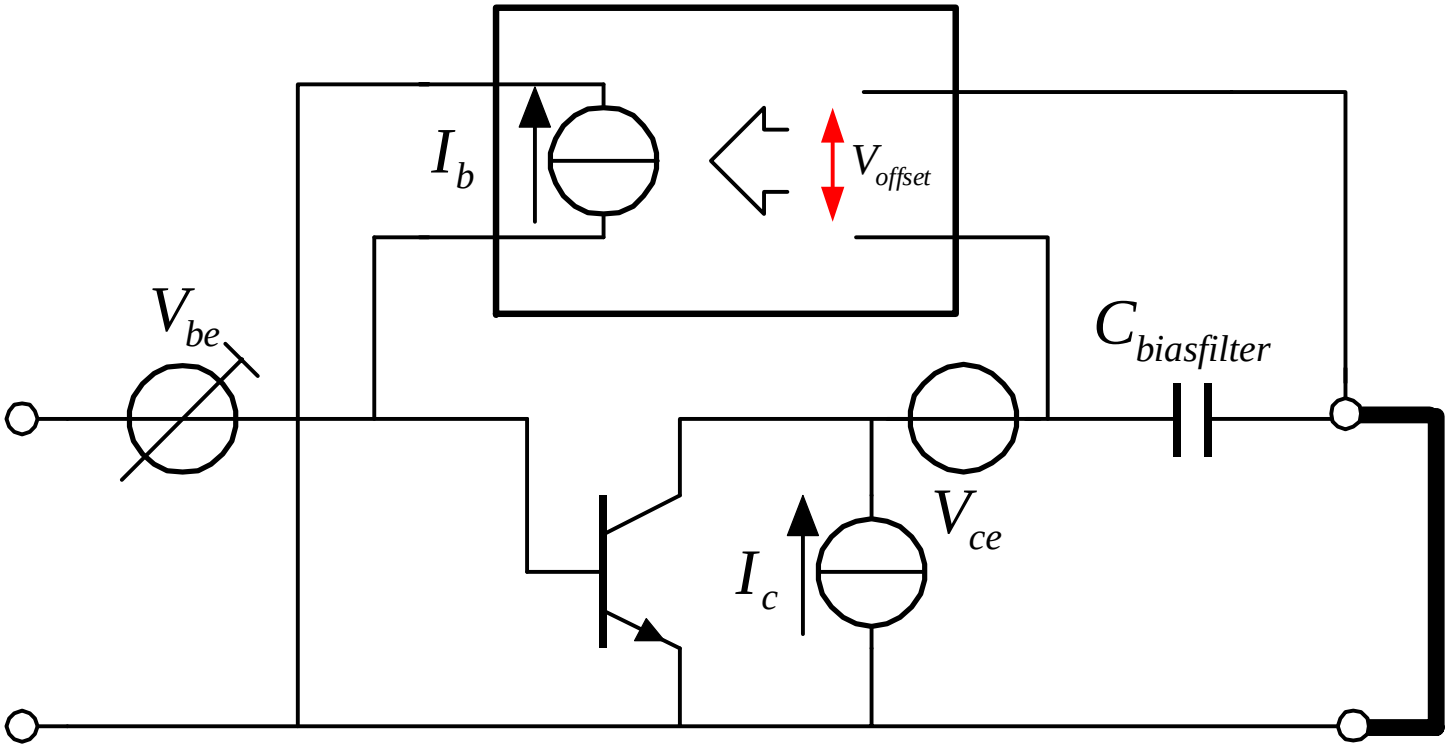
Biasing a single transistor



Biasing a single transistor

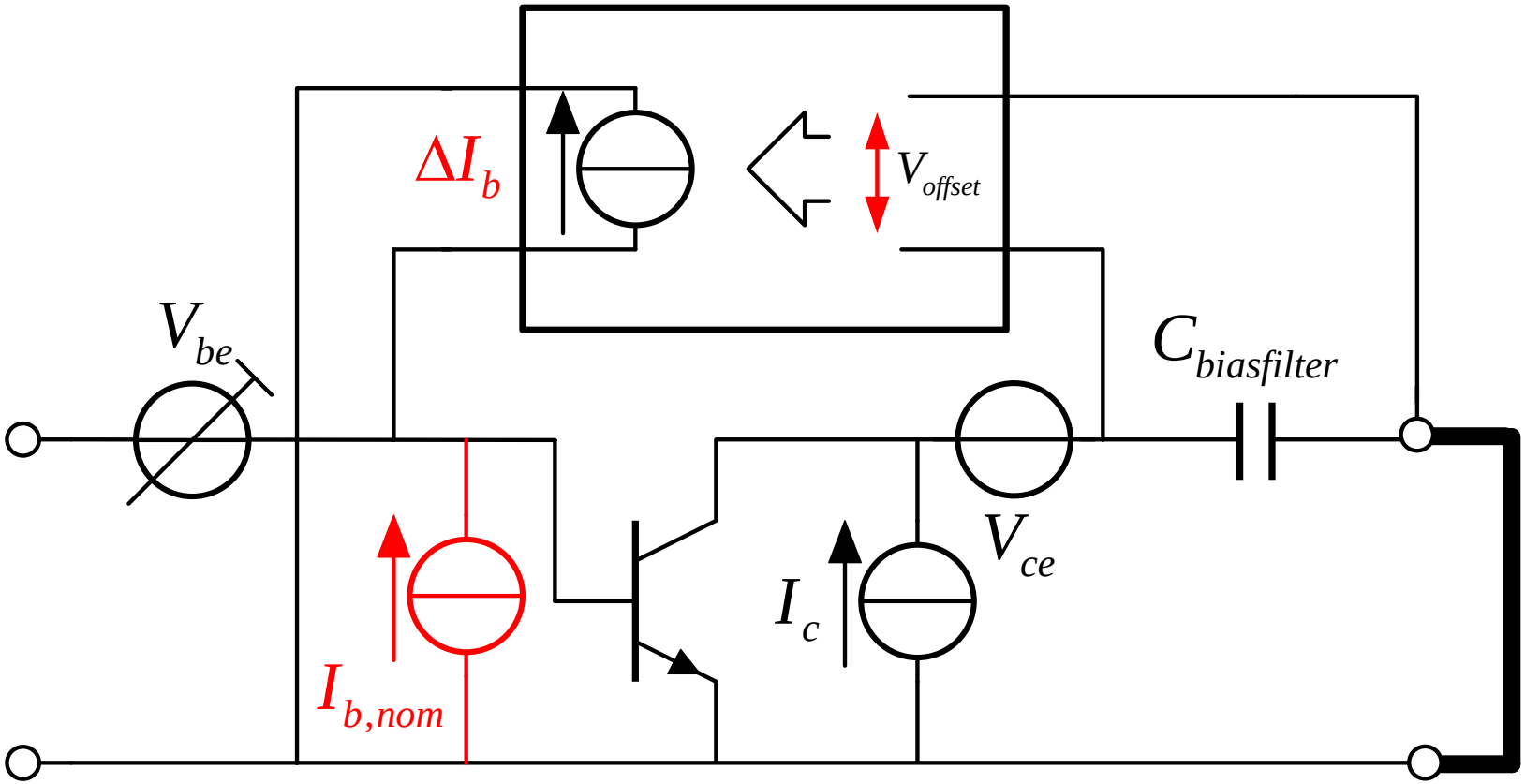


Biasing a single transistor



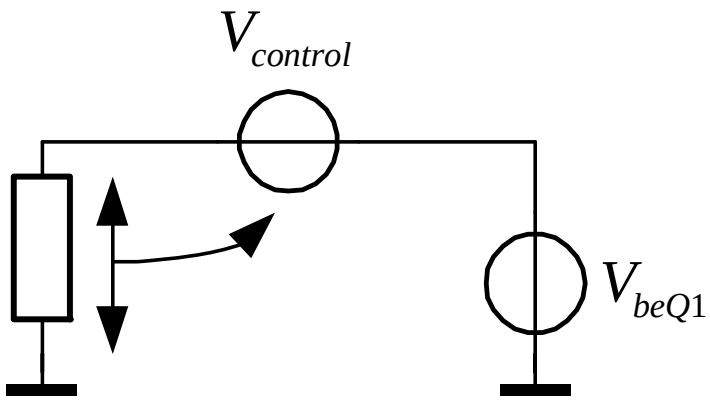
Conflict:
- High gain gives high bandwidth (undesired for bias signals)
- Low gain gives much offset

Biasing a single transistor (2)



Add $I_{b,nom}$ to reduce offset at limited loop gain.

Local voltage control loops

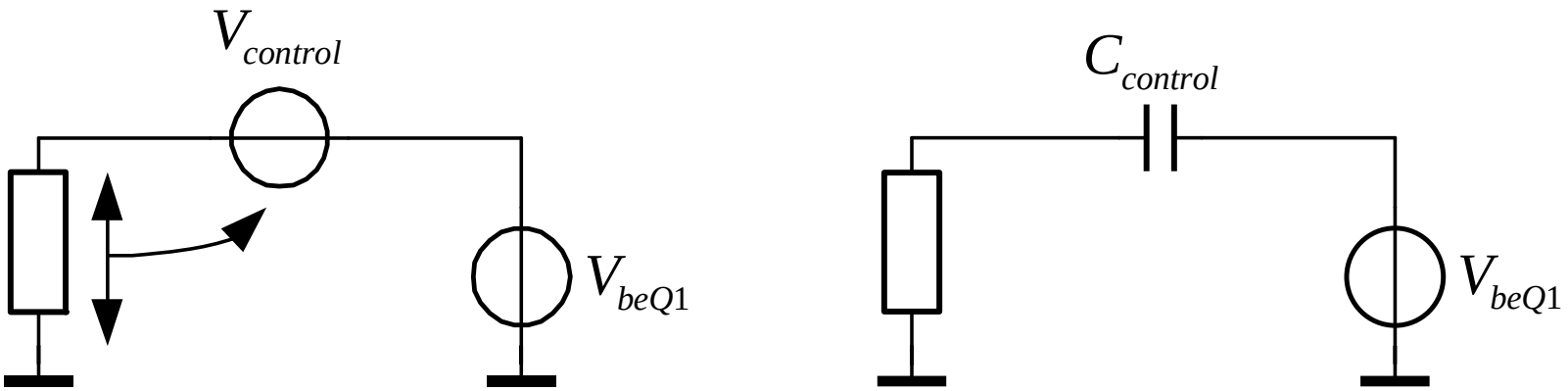


There is no current through $V_{control}$

$V_{control}$ does not produce power

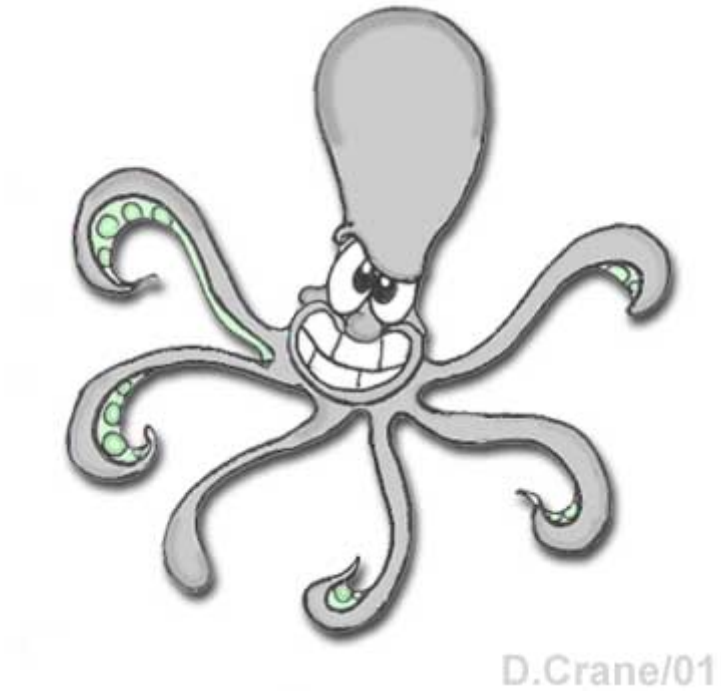
$V_{control}$ can be a passive component

Local voltage control loops

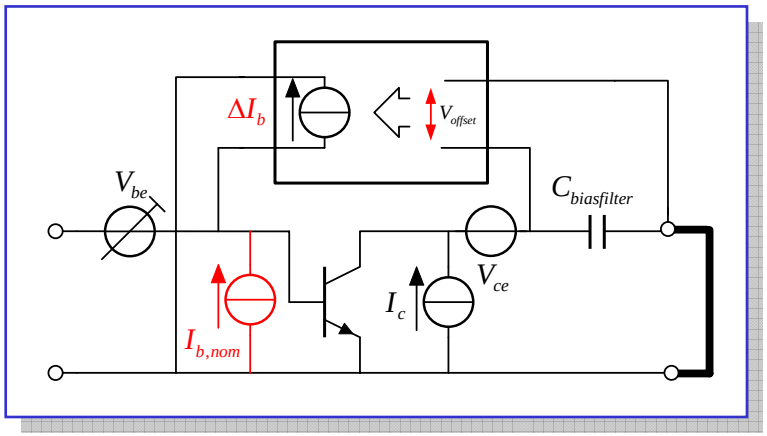


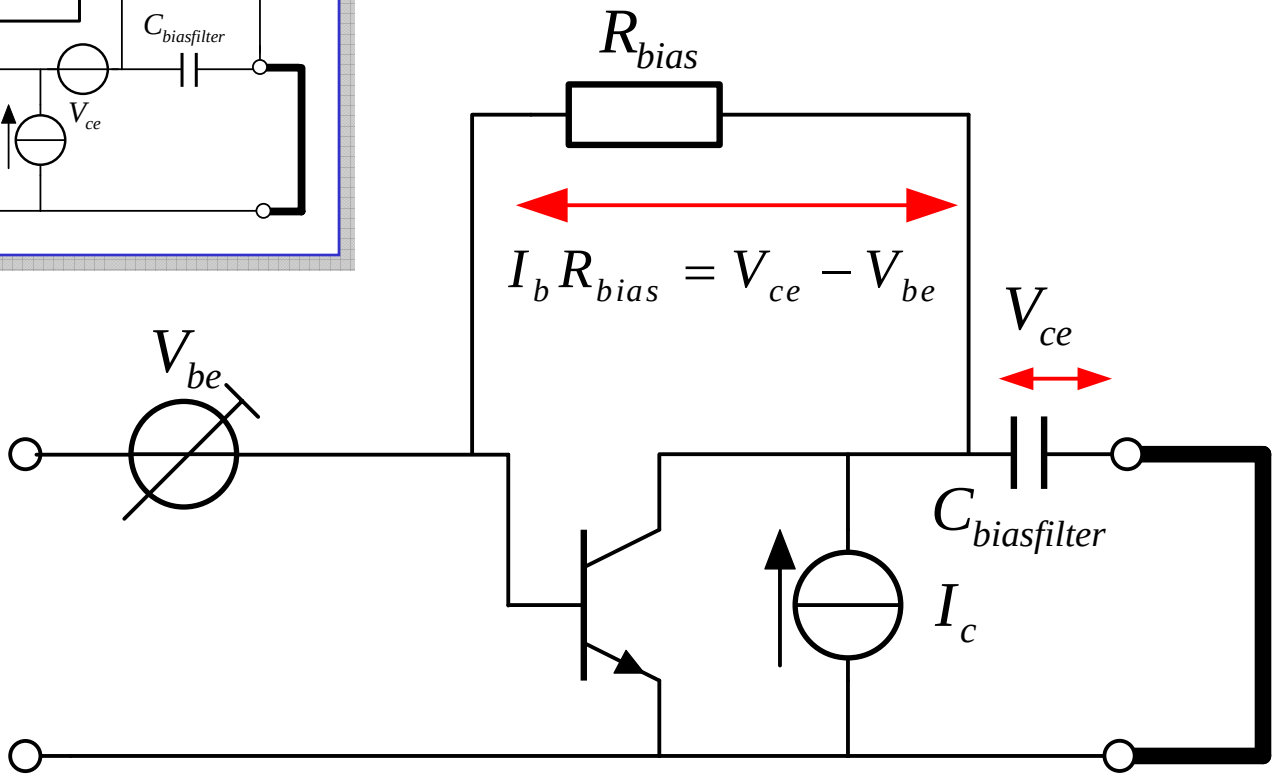
Only possible because this bias **source is not delivering power**

Practical examples



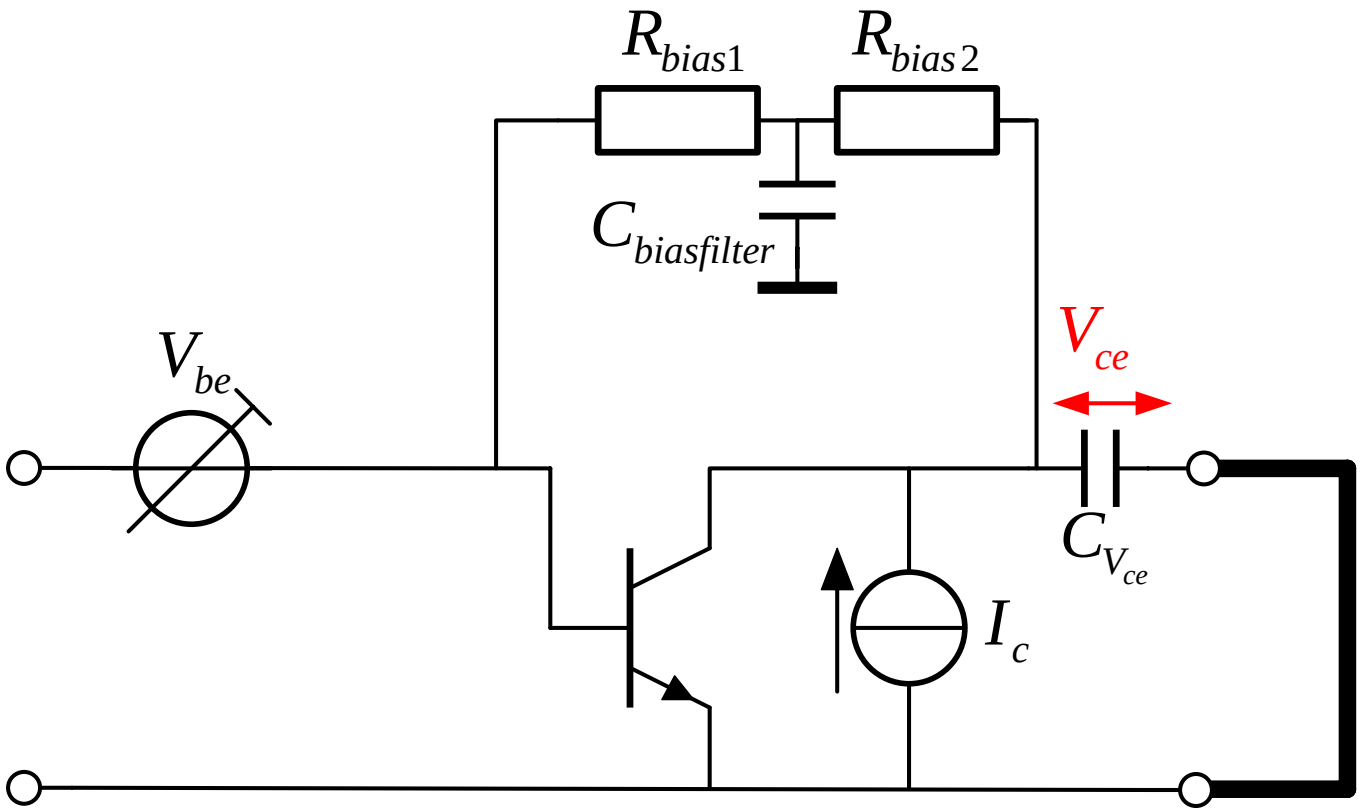
Biasing a single transistor





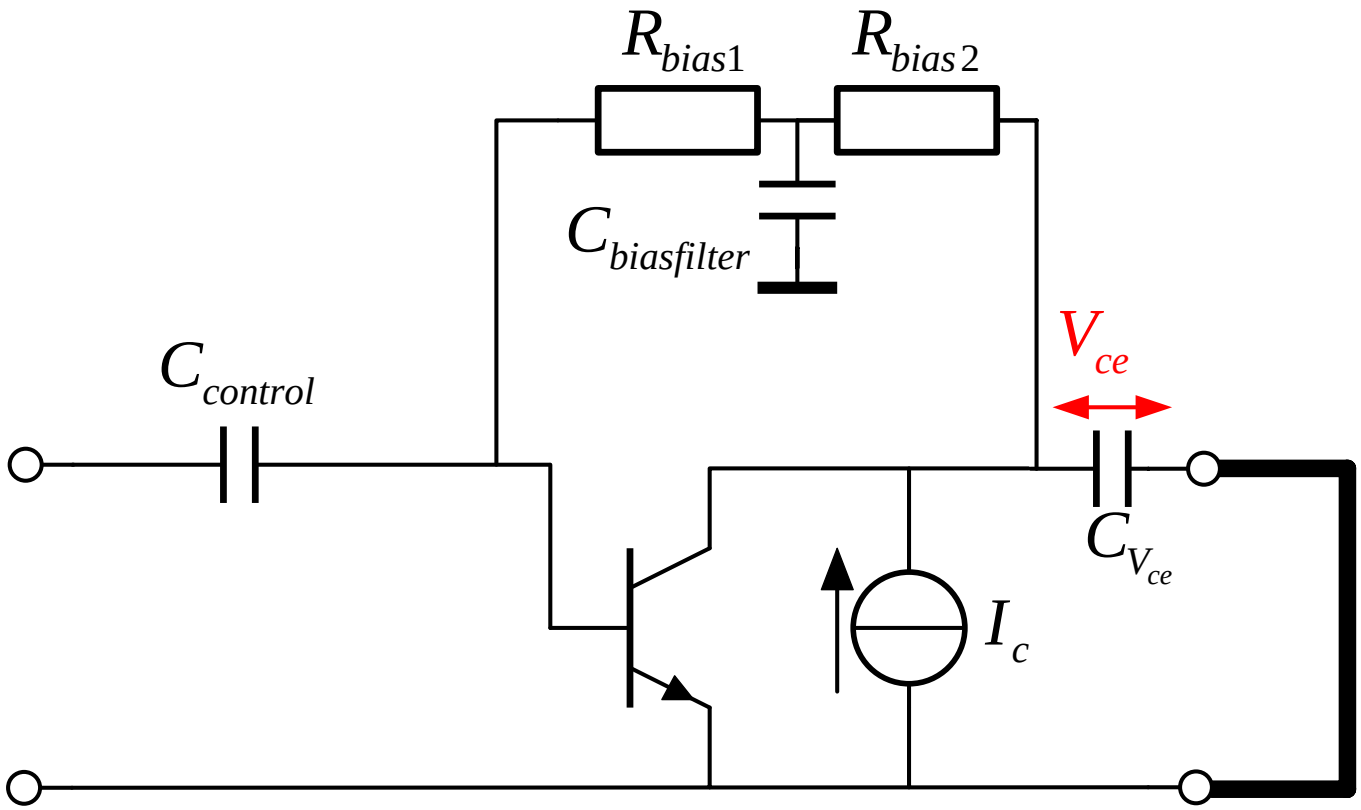
Problem: Filter function is lost!

Biasing a single transistor



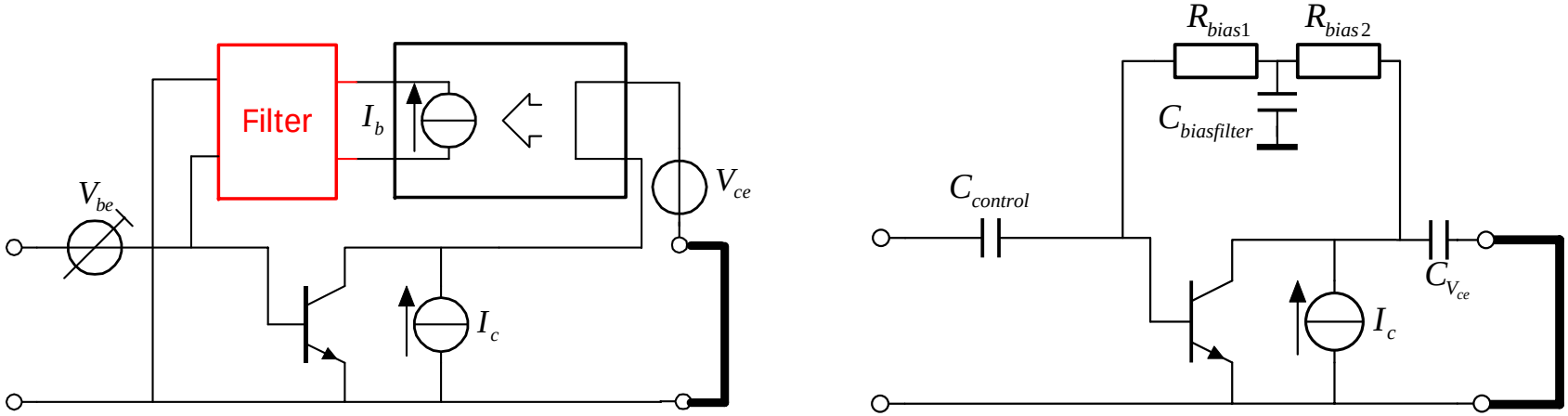
$$I_b \left(R_{bias1} + R_{bias2} \right) = V_{ce} - V_{be}$$

Biasing a single transistor



$$I_b \left(R_{bias1} + R_{bias2} \right) = V_{ce} - V_{be}$$

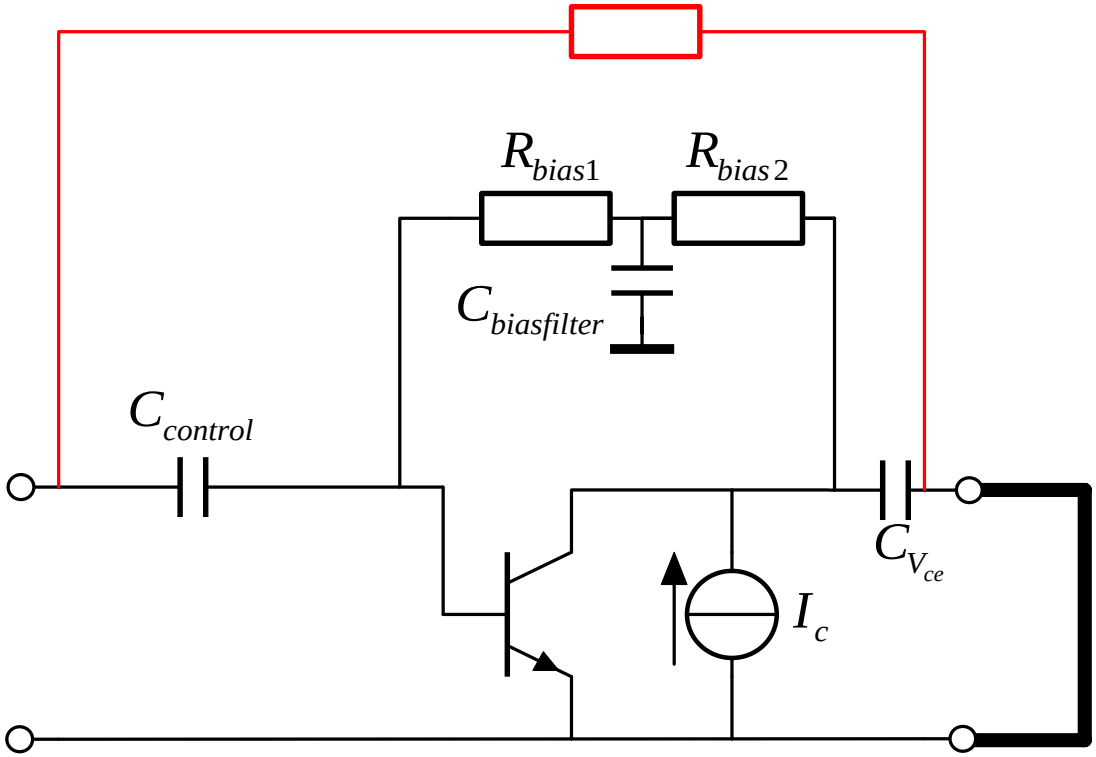
Non-ideal biasing a single transistor



5 non-idealities:

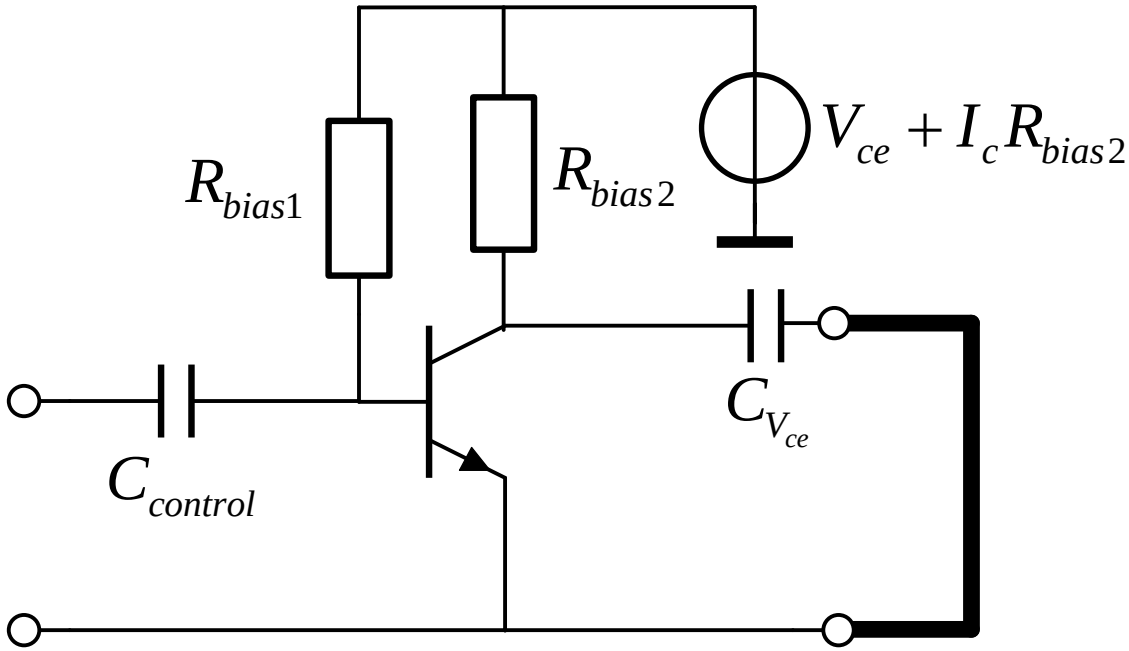
1. R_{bias1} loads input
2. R_{bias2} loads output
3. Collector bias *voltage* depends on I_b
4. $C_{control}$ increases noise contribution of I_b
5. C_{Vce} increases output voltage swing: distortion

C_{Vce} increases output voltage swing: distortion



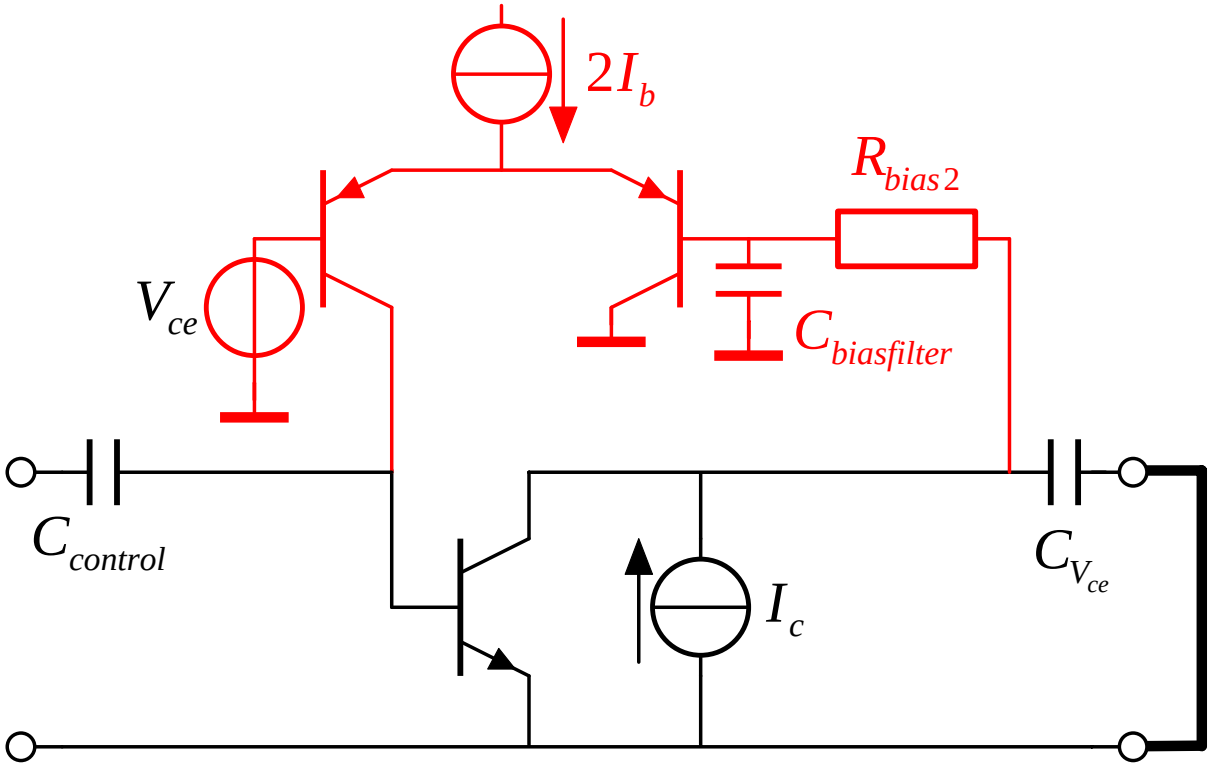
Biasing components are **inside** the loop

How about this?



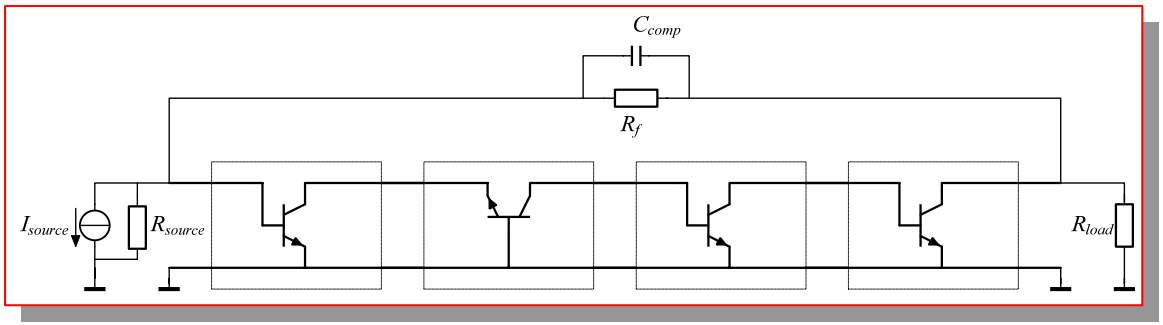
1. R_{bias1} loads input
2. R_{bias2} loads output
3. Collector bias *voltage* depends on I_c
4. $C_{control}$ increases noise contribution of I_b
5. C_{Vce} increases output voltage swing: distortion
6. Collector **current depends on I_b and D** (unreliable)

An active implementation

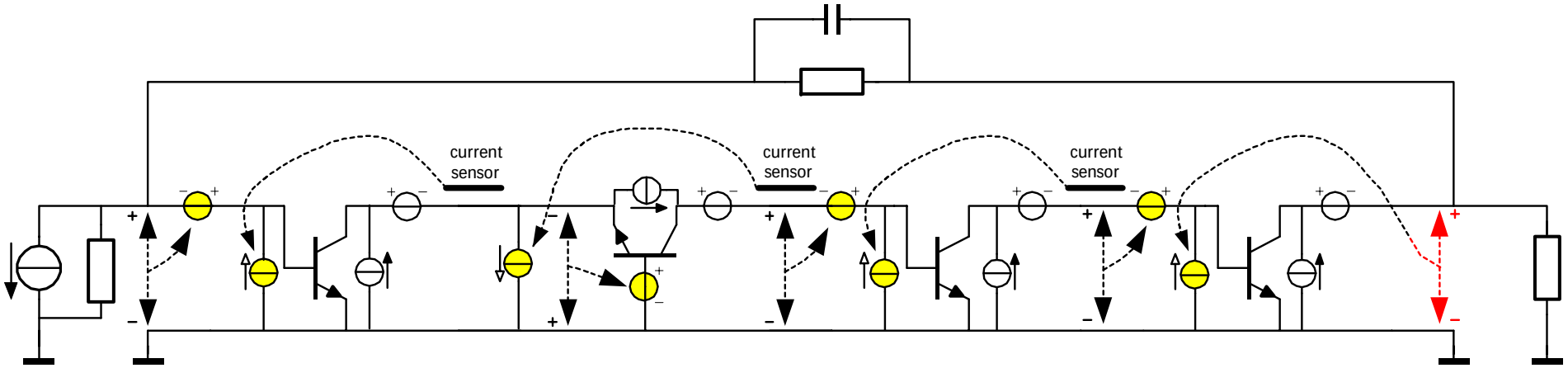


1. R_{bias2} loads output (but it can be large)
2. $C_{control}$ increases noise contribution of I_b
3. C_{Vce} increases output voltage swing: distortion
4. takes a lot of transistors

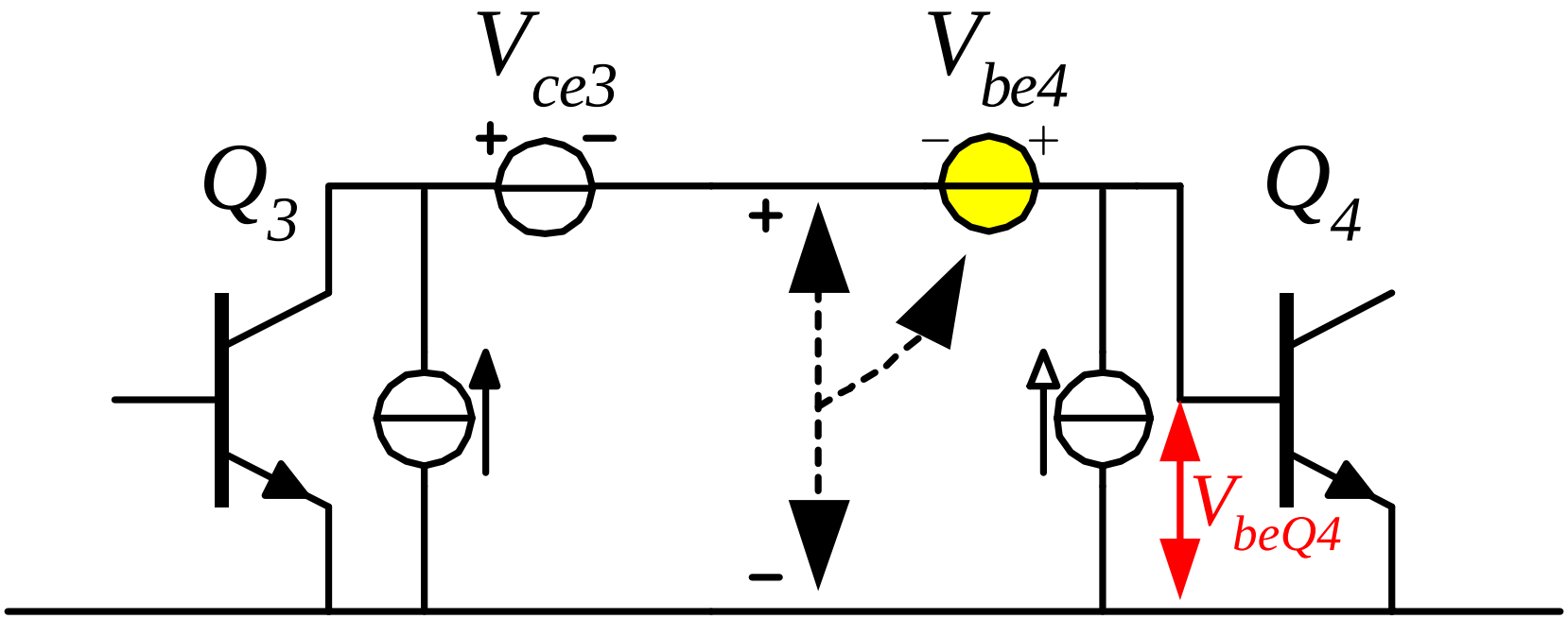
Biasing a circuit



It works, but
- too many sources
- too many controls



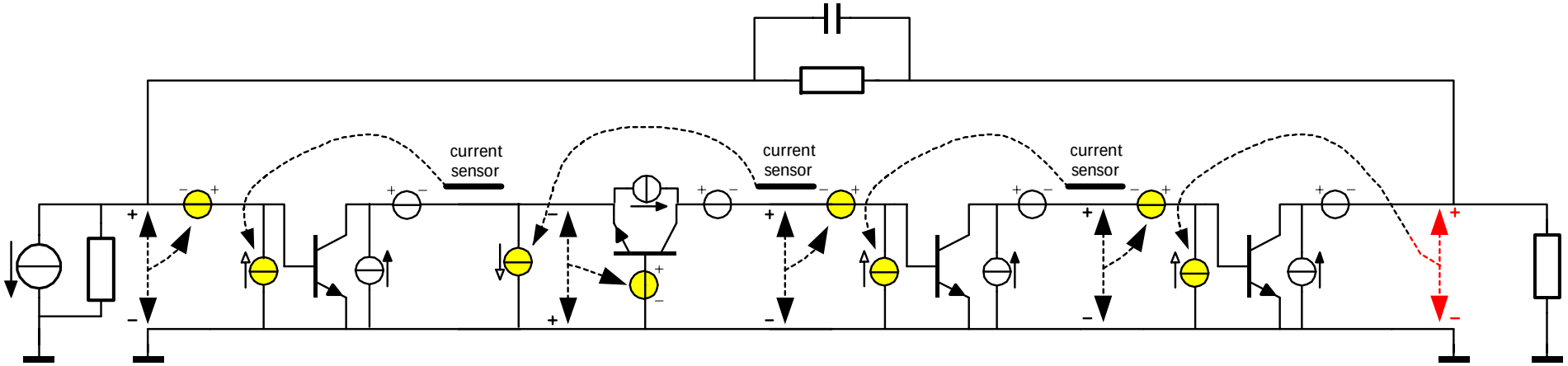
Removing a voltage control loop

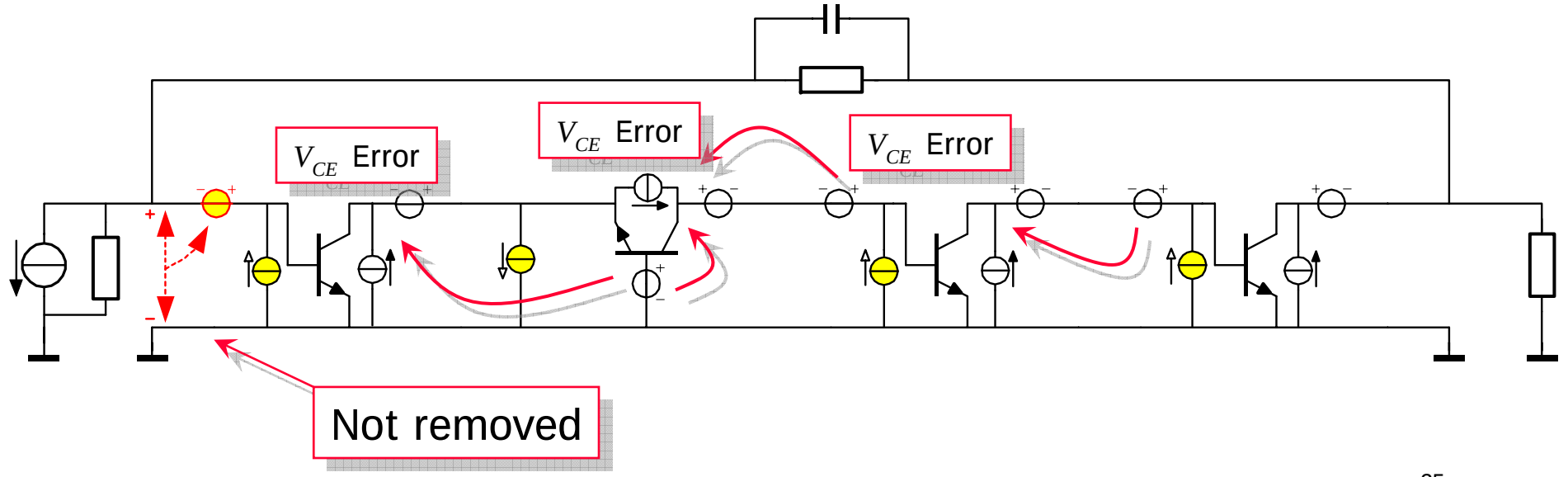


Set source V_{be} at **nominal value**

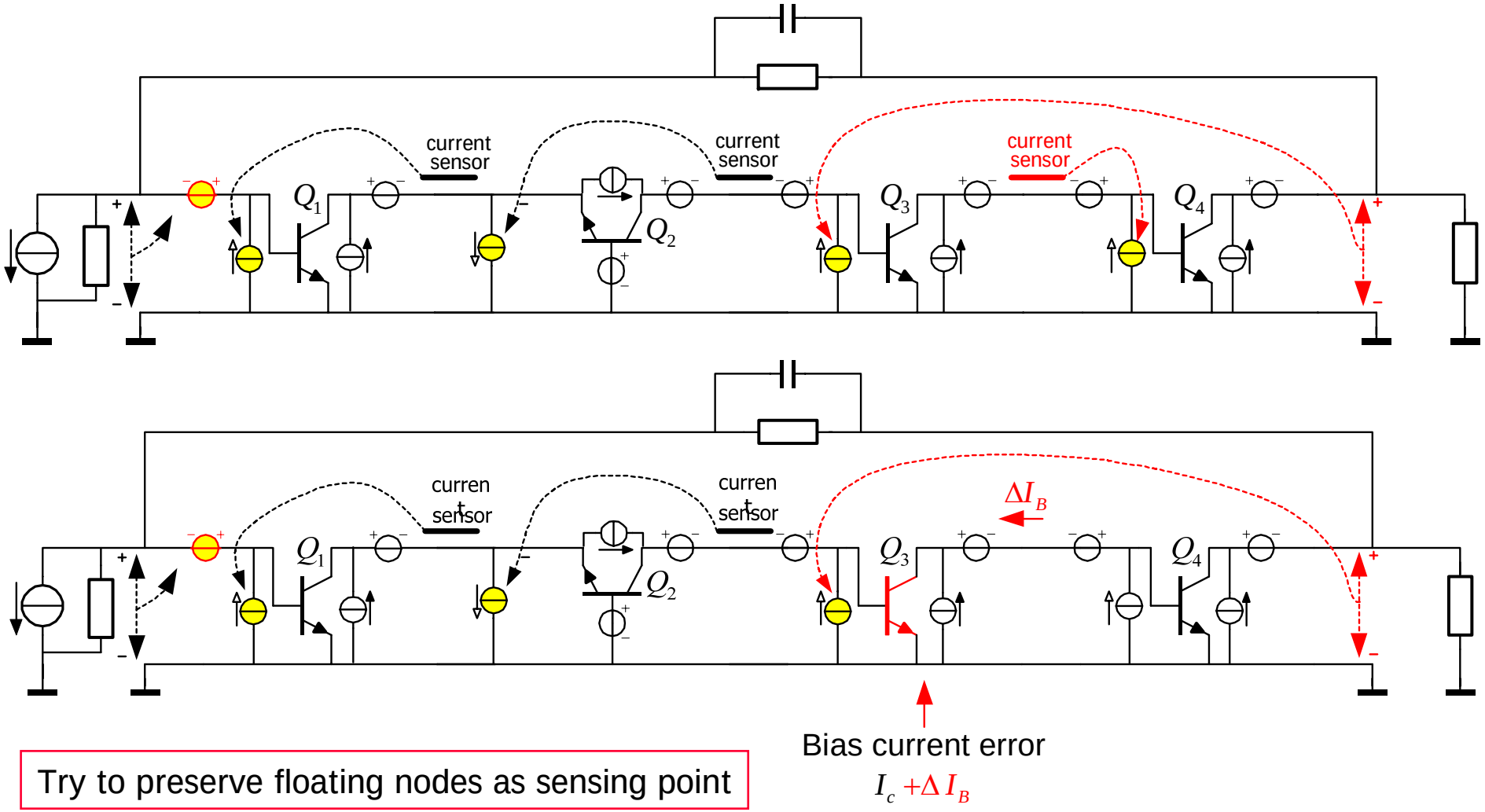
Bias **voltage error** for Q_3 : $\Delta V_{ceQ3} = V_{be} - V_{beQ4}$

Removing voltage controls



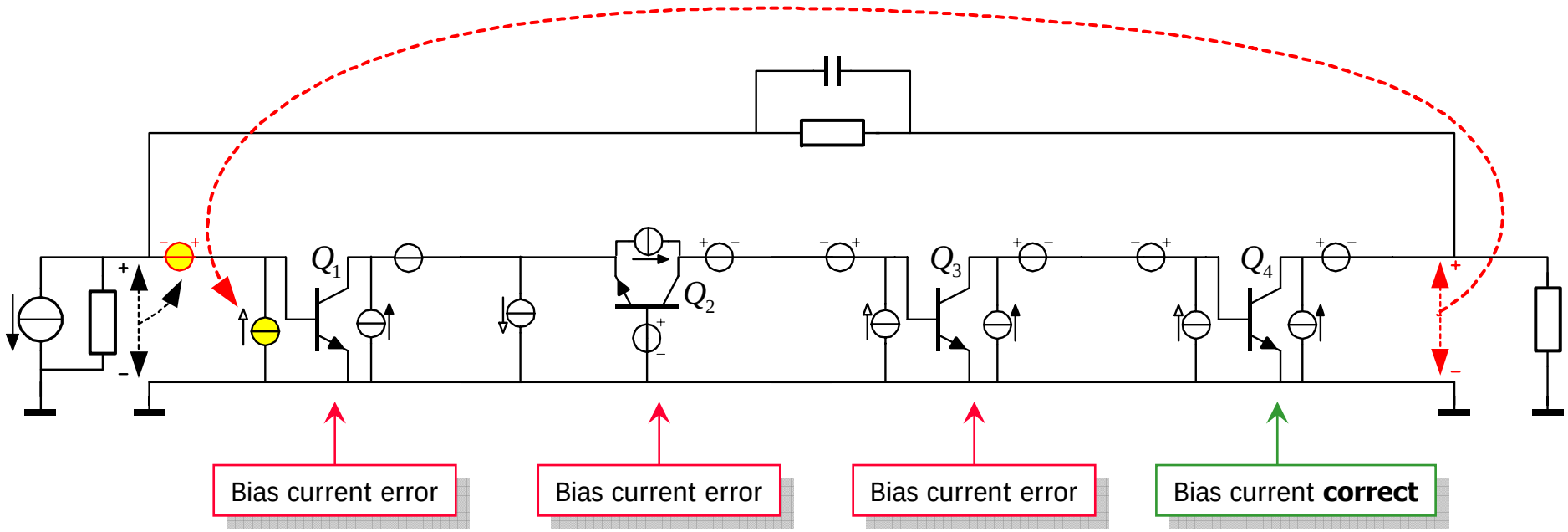


Removing current control loops

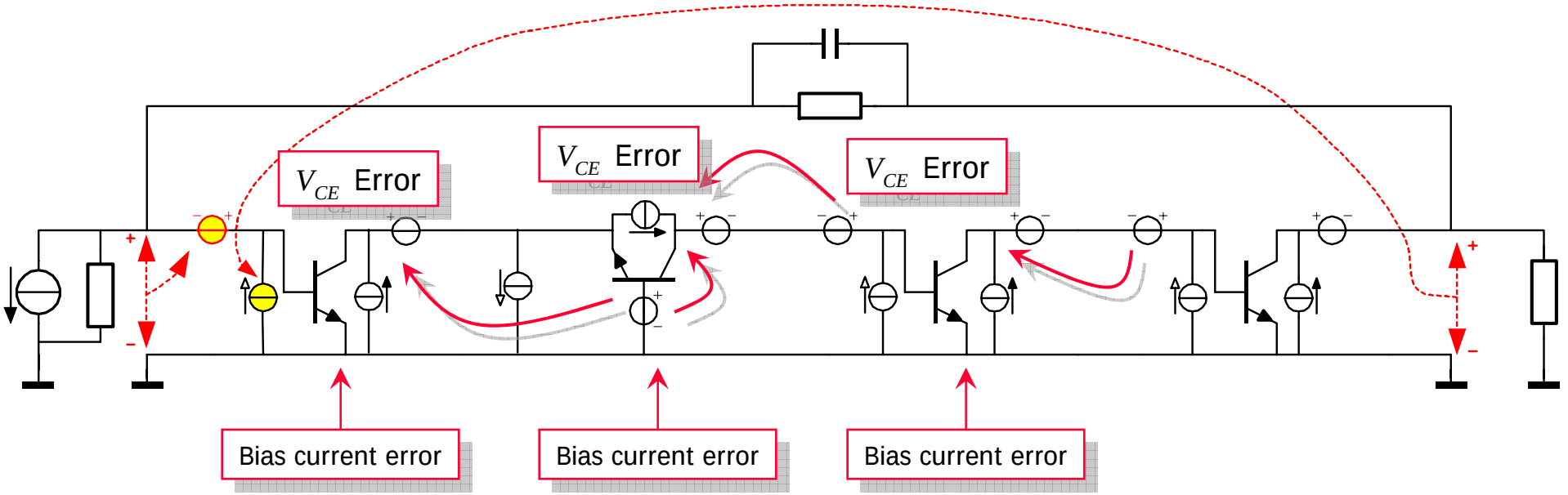


Try to preserve floating nodes as sensing point

One overall current control loop



Circuit with 2 loops and 6 errors



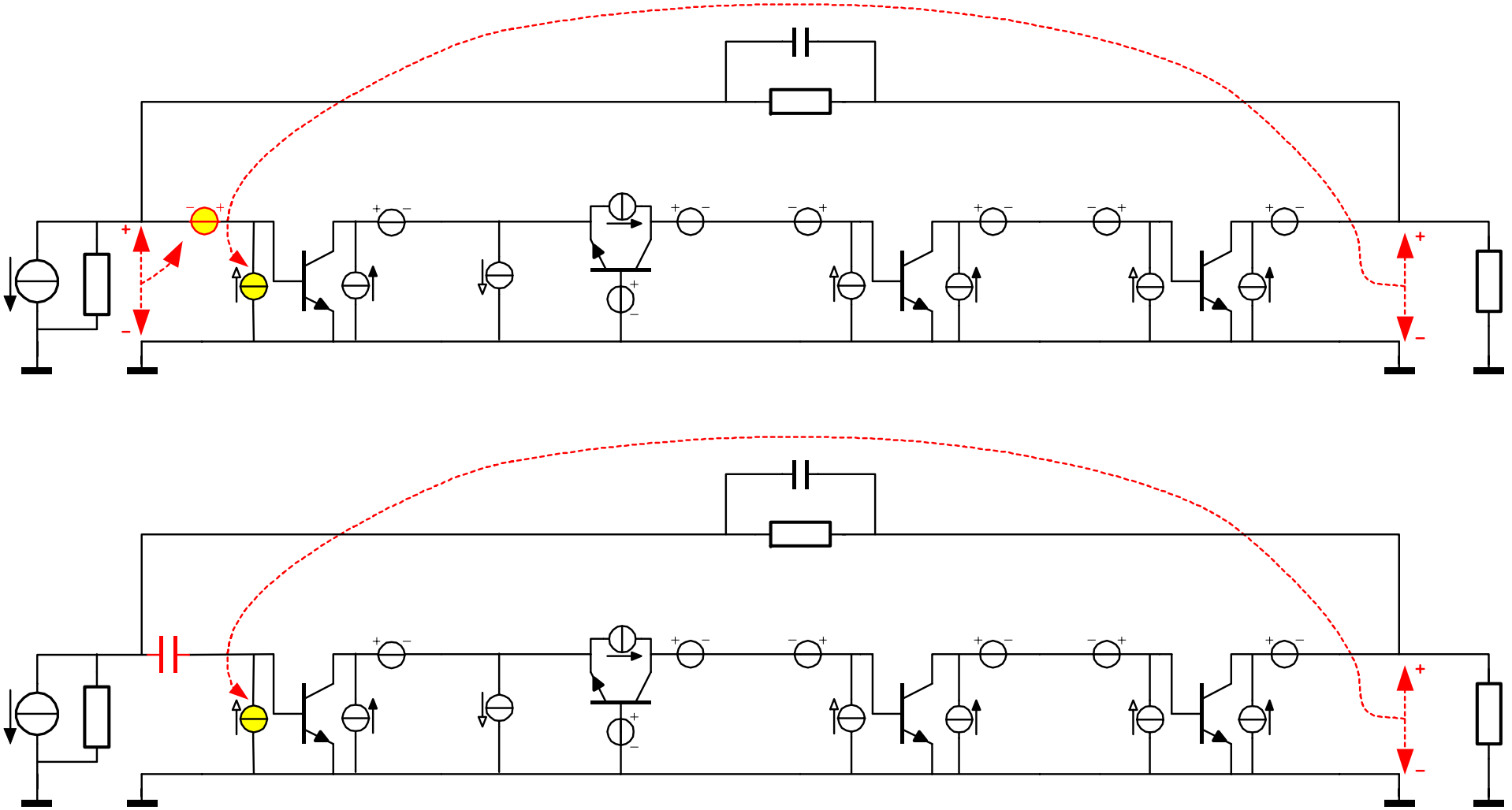
Last transistor has no biasing errors

Other transistors have **acceptable** errors

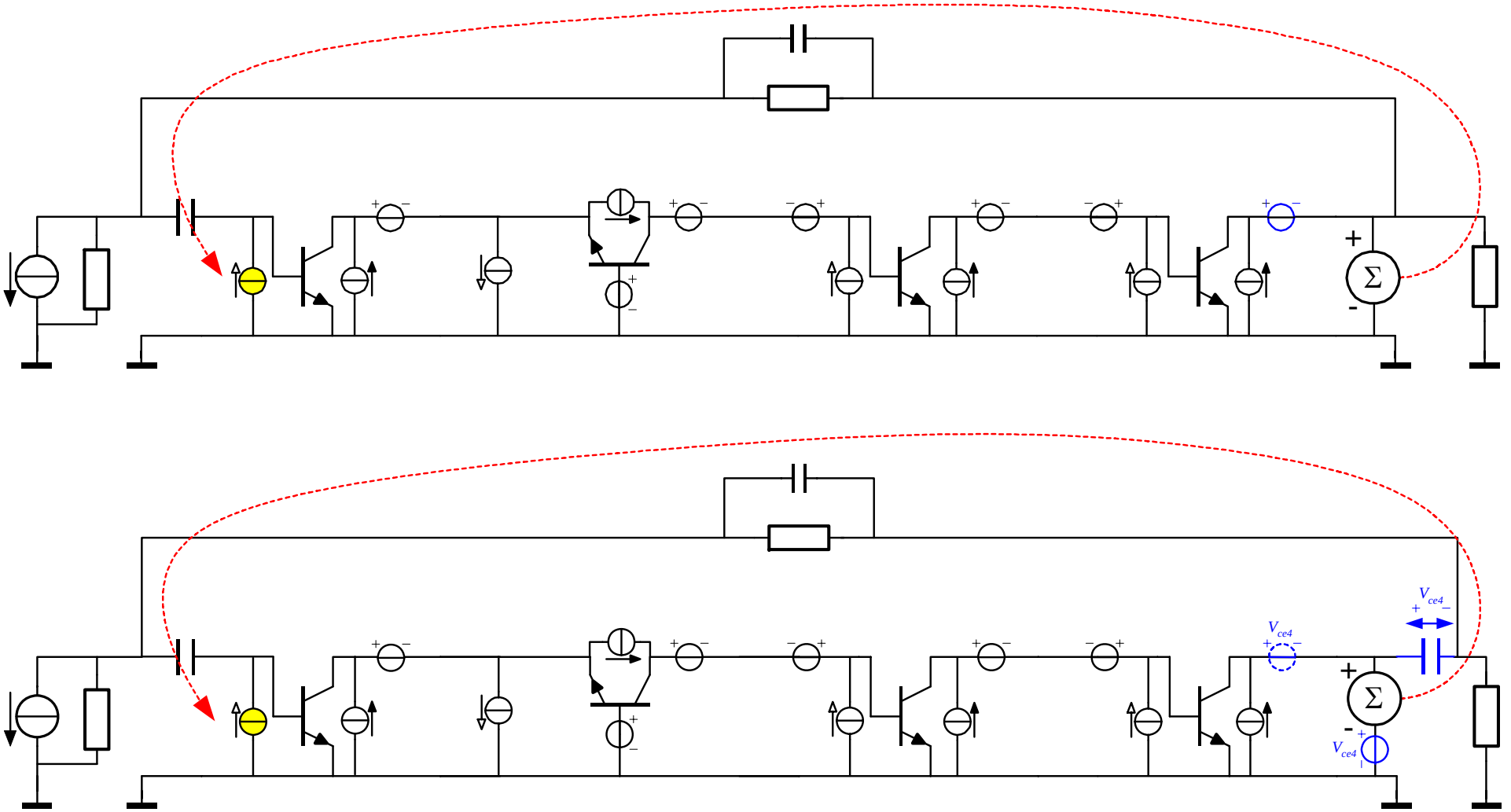
One voltage loop to be implemented

One current loop to be implemented

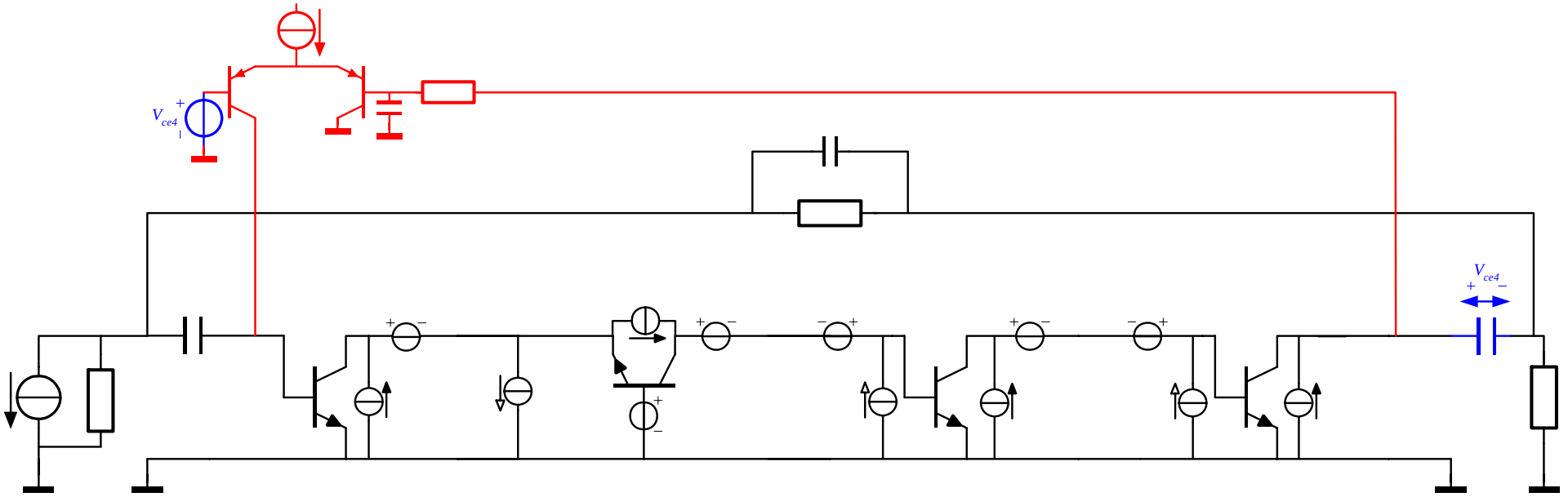
The local voltage loop



The current sensor



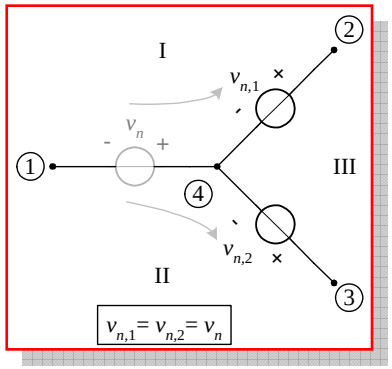
The bias current loop

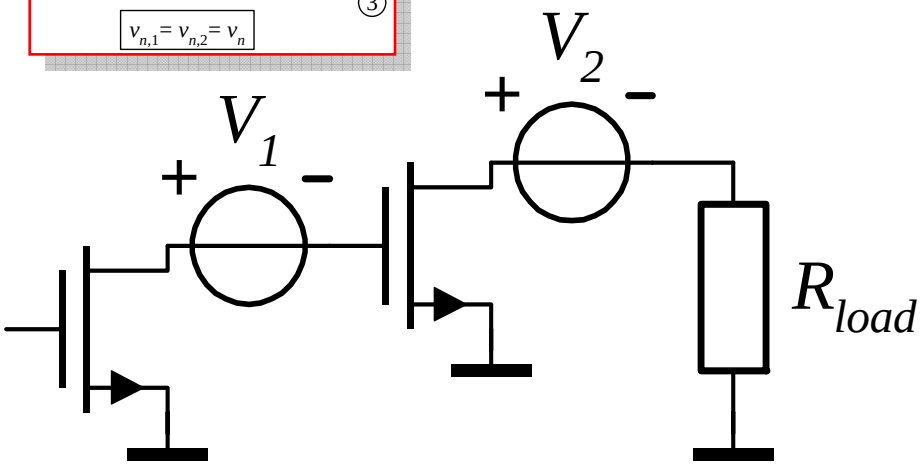


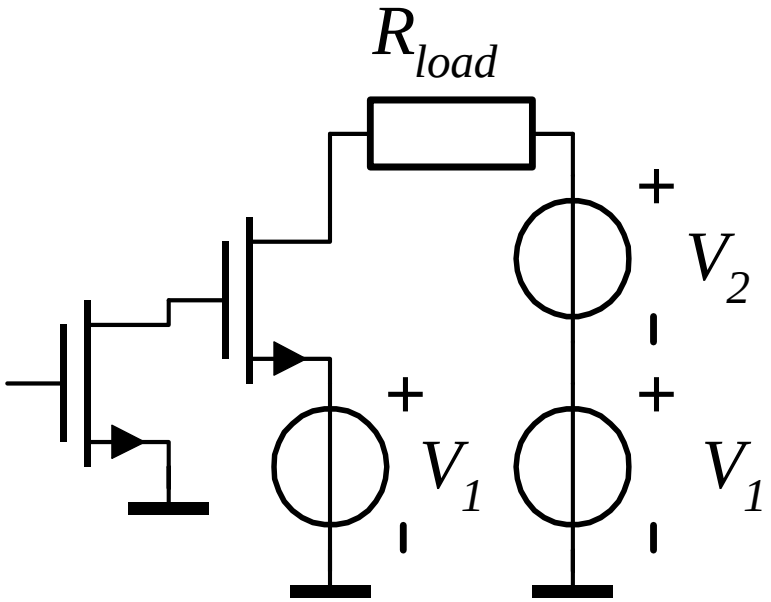
☺ Practical loop

☹ Voltage and current sources at inconvenient places

Shifting of voltage sources



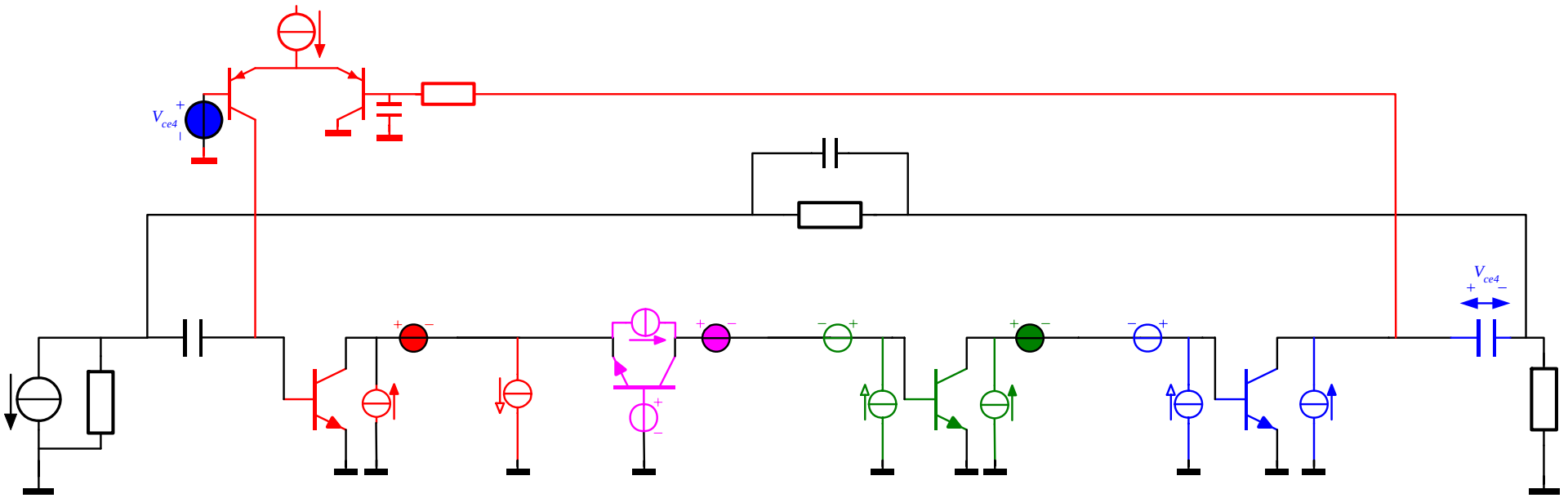




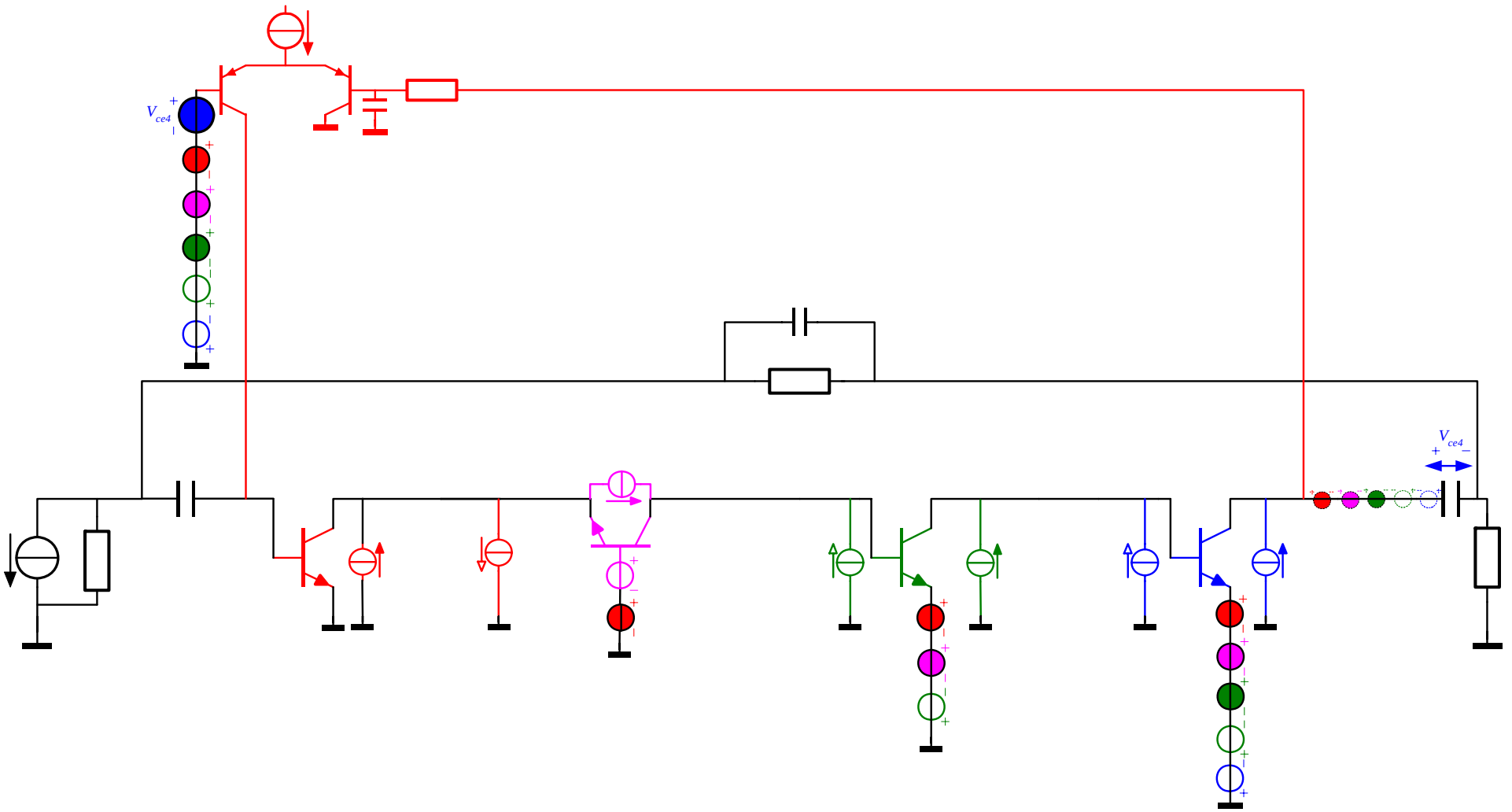
Preference for **grounded branches**

Grounded sources become **supply voltages**

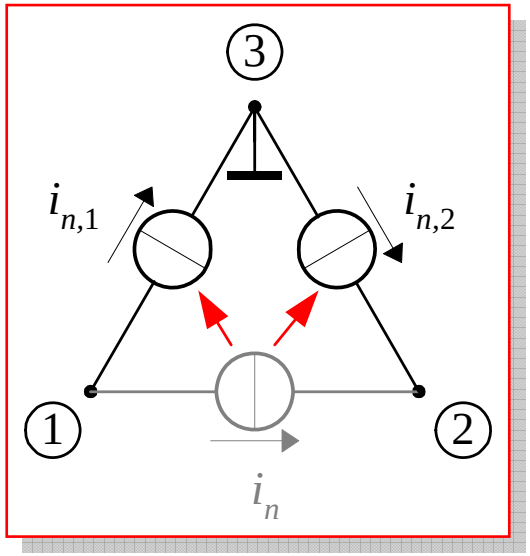
Shifting voltage sources

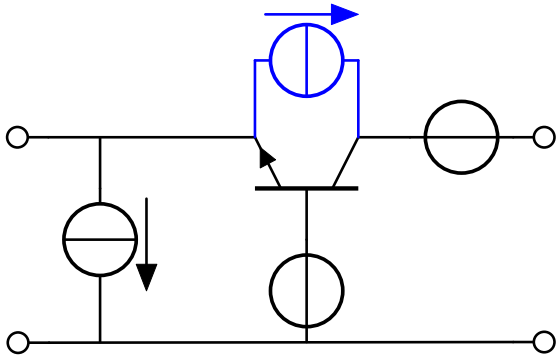


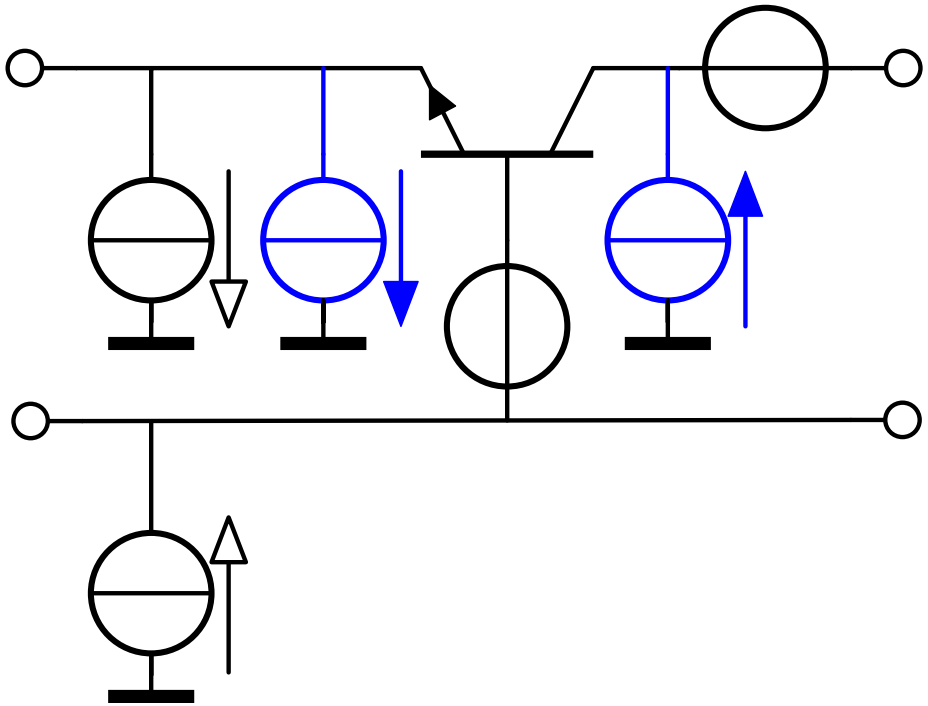
Shifting voltage sources



Merging current sources



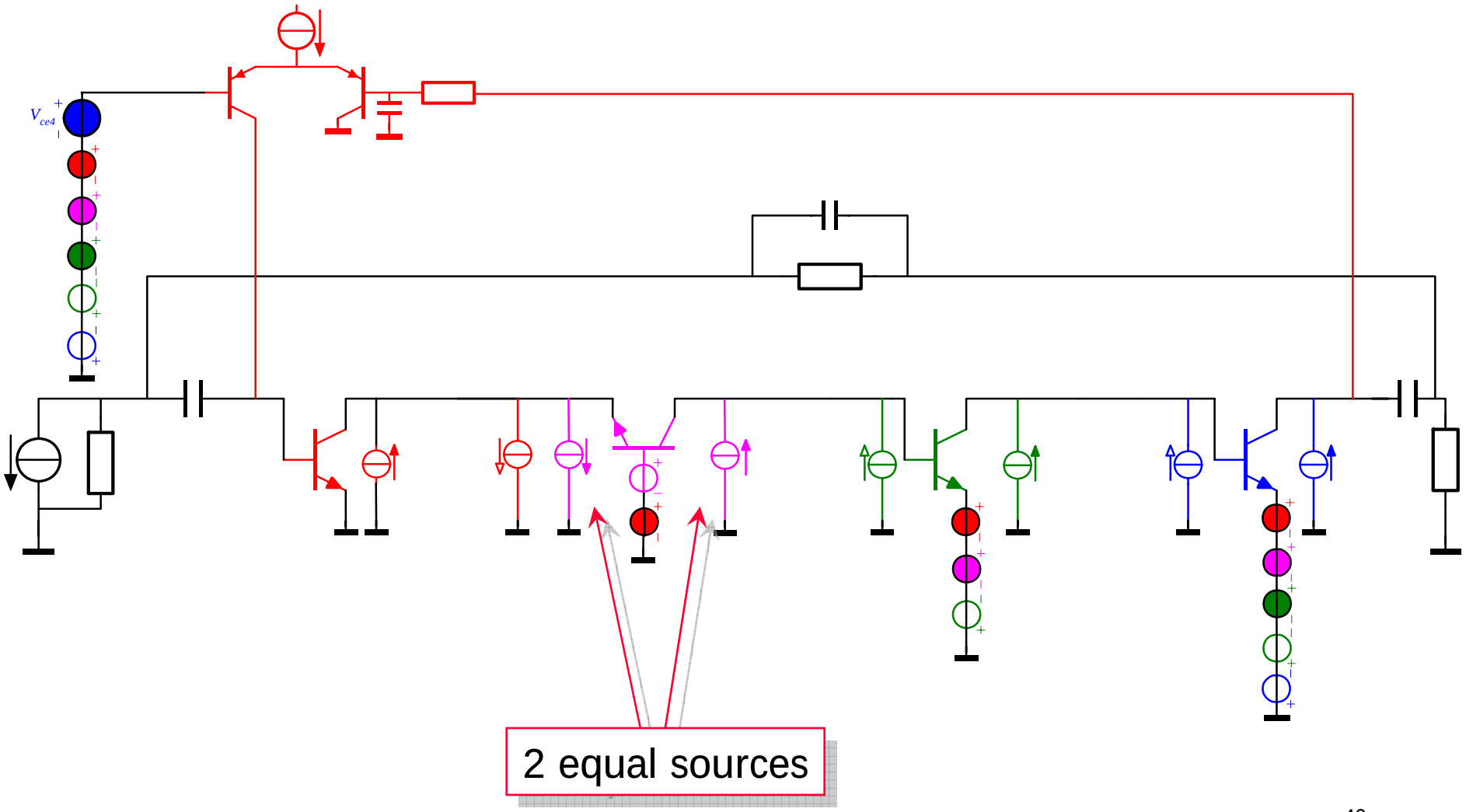




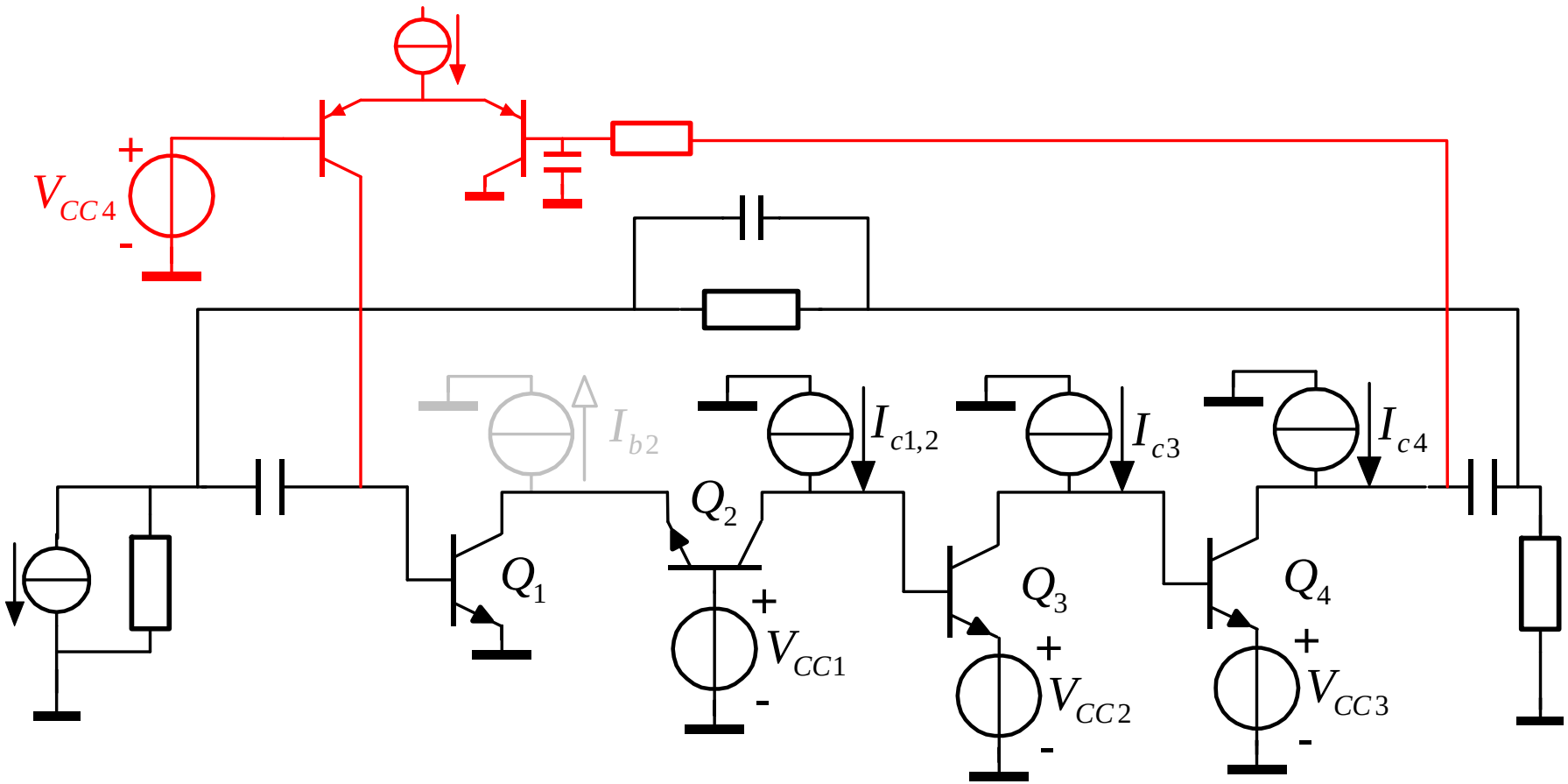
Create grounded current sources

1 source $\Rightarrow$ 2 *equal* sources

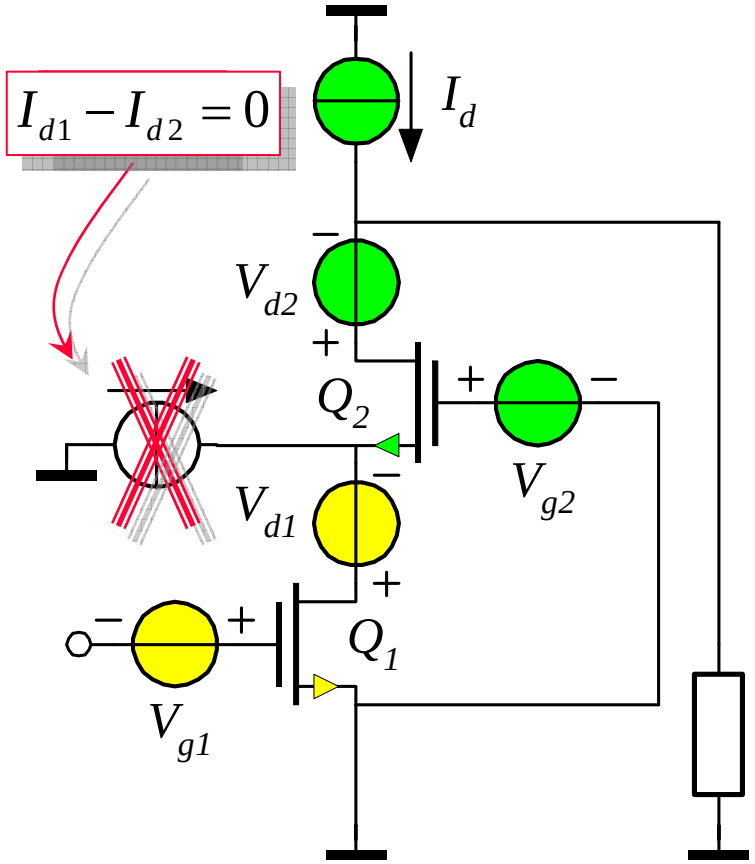
Merging the current sources

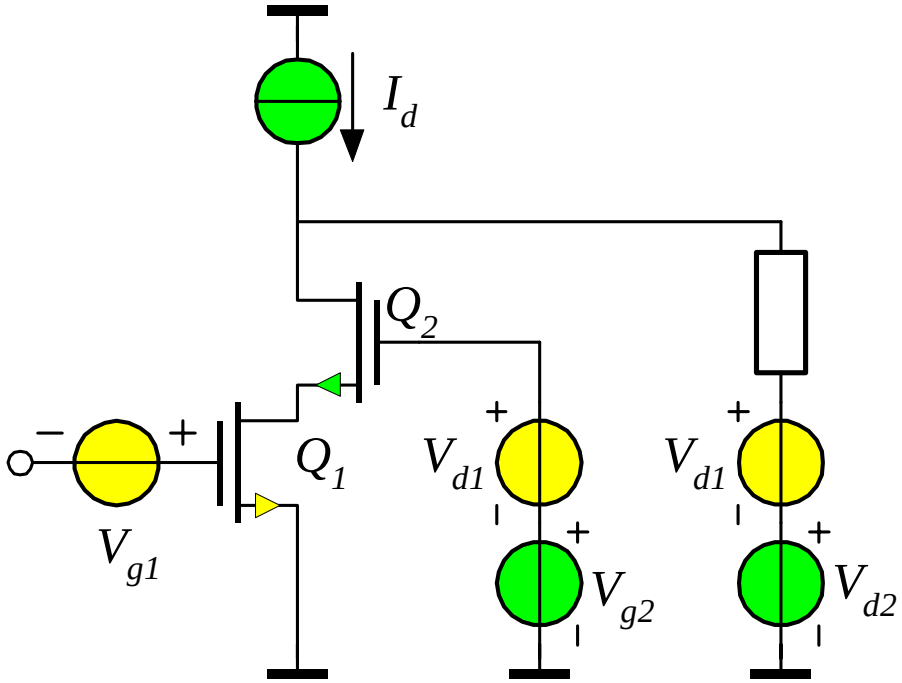


Result



Supply voltage or current minimization

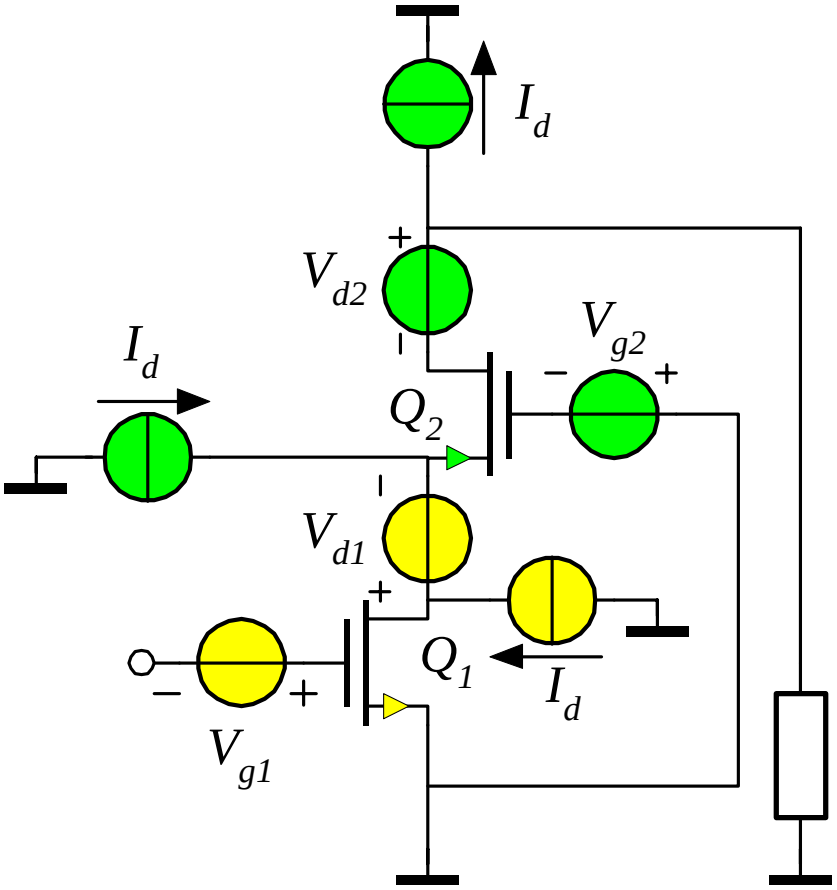


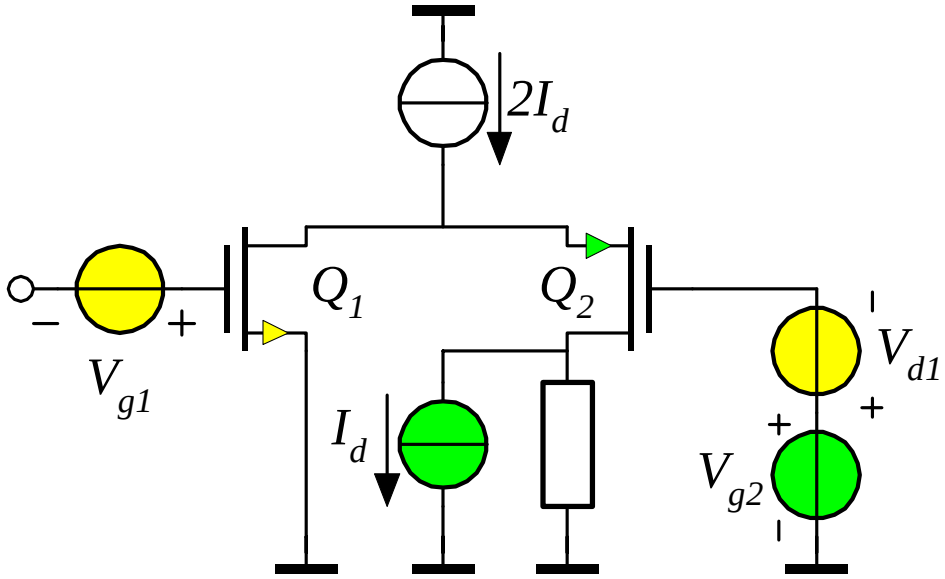


Current minimization

Changing transistor type

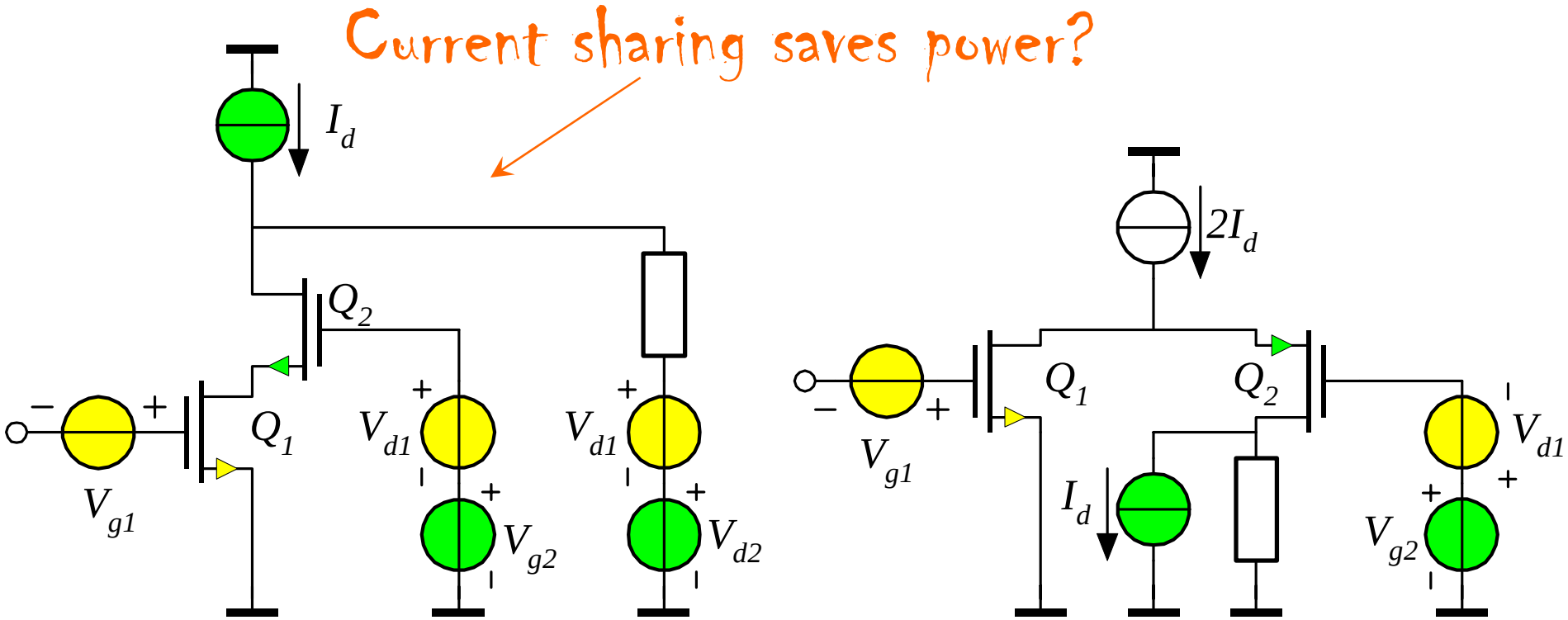
Bias sources change sign





Voltage minimization

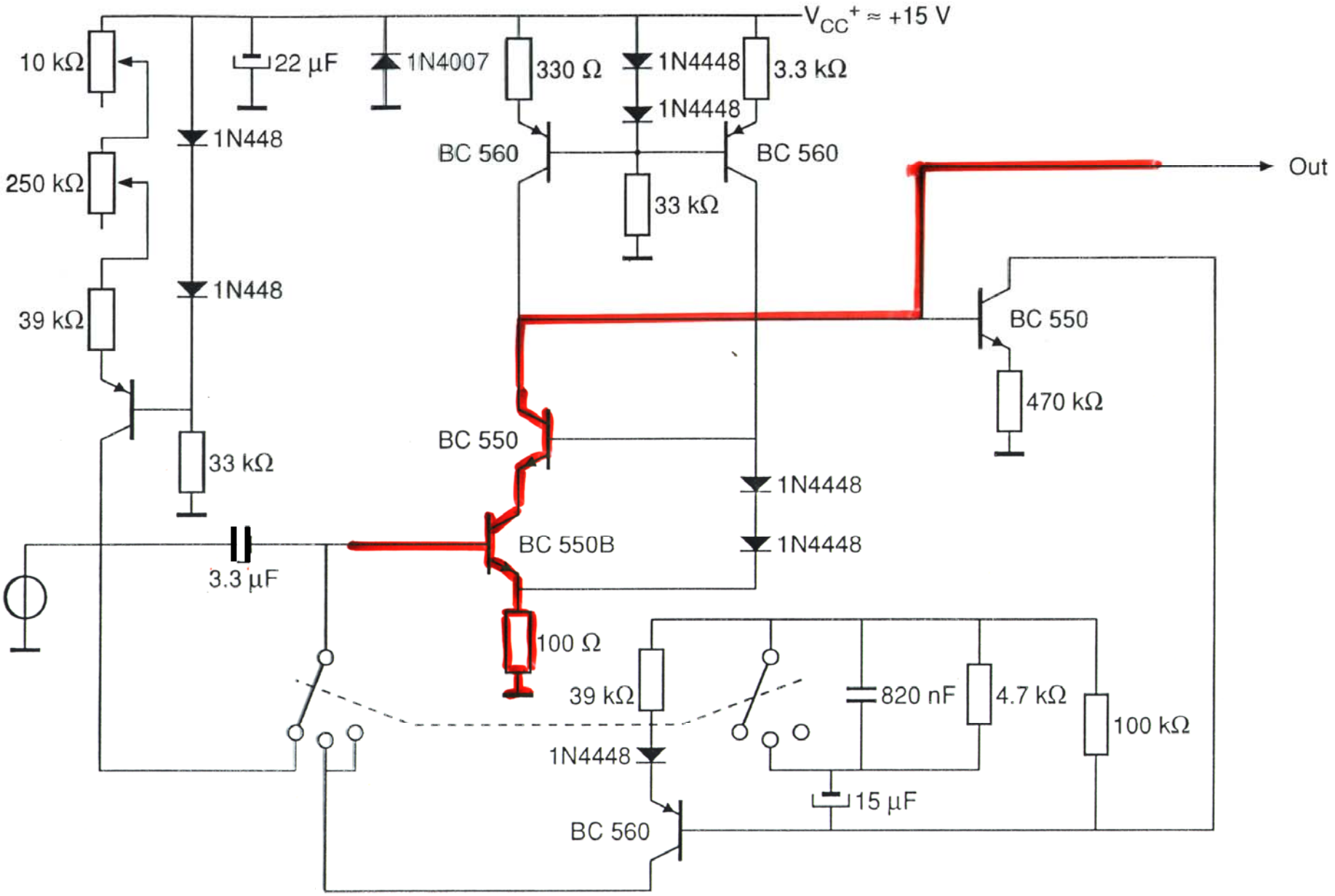
Low voltage or current designs



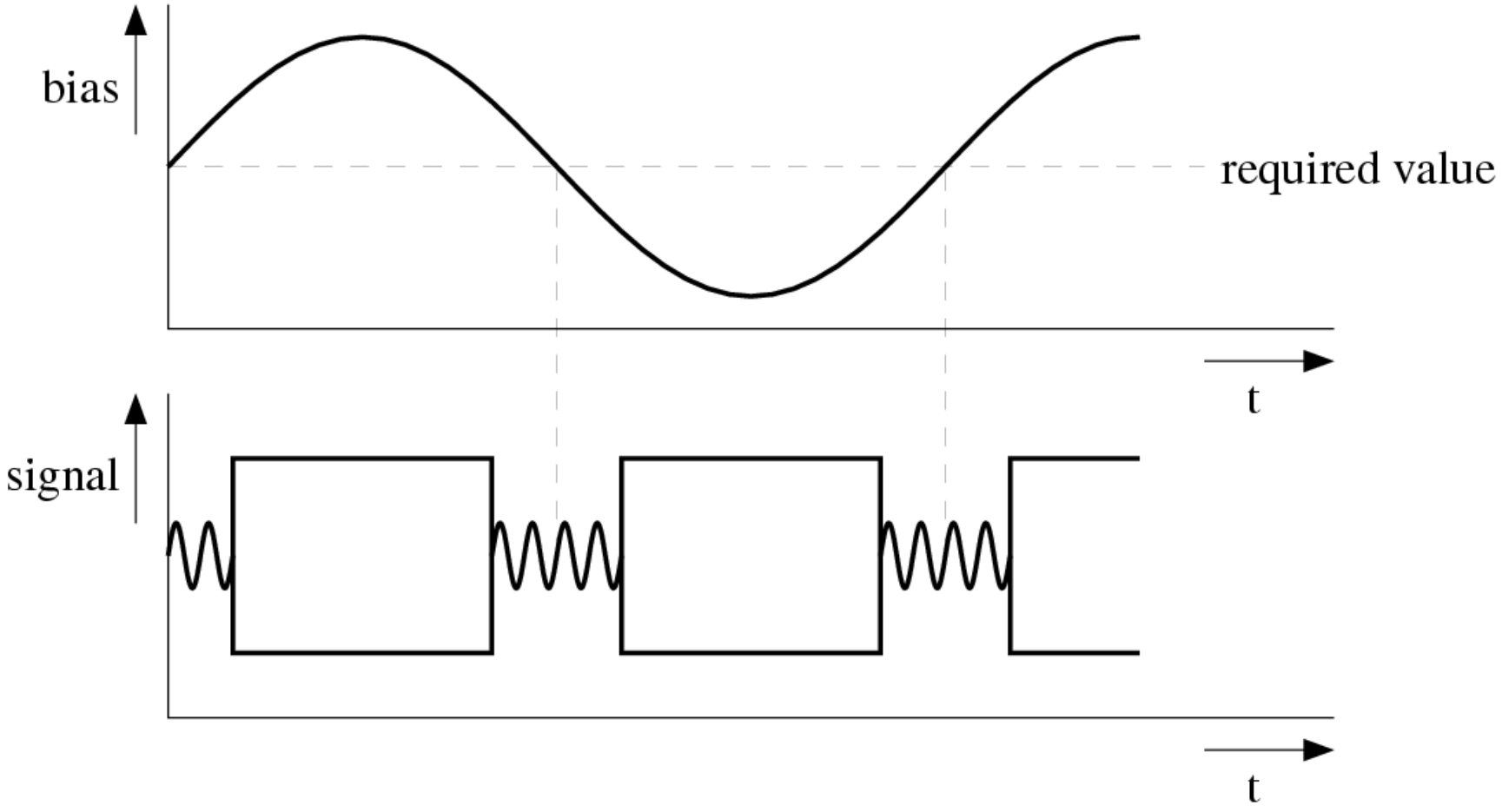
Always 4 sources

Power dissipation does not change

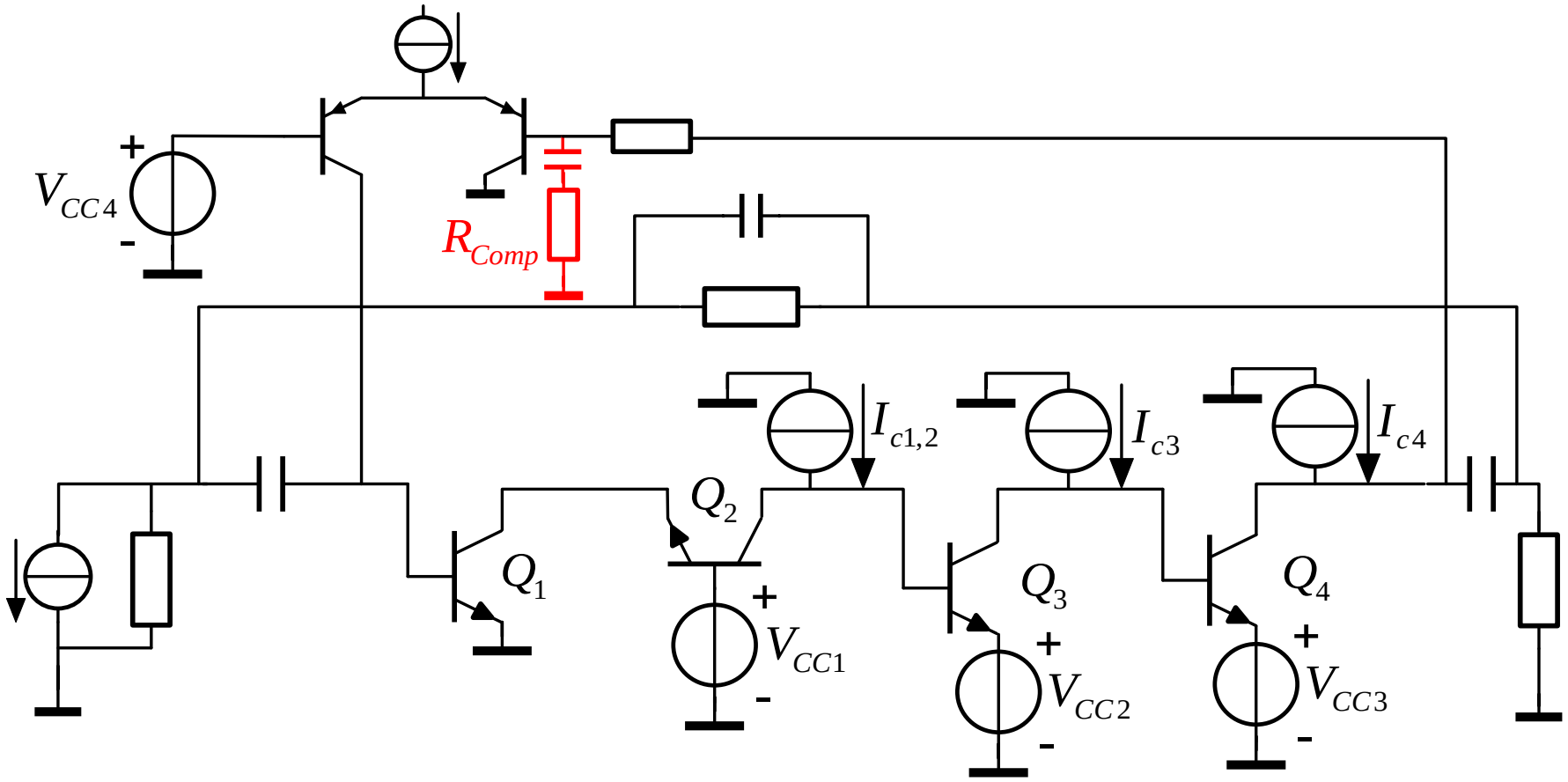
Choice between low voltage or low current


$V_{CC}^{+} \approx +15$ V
10 kΩ
22 µF
1N4007
330 Ω
1N4448
3.3 kΩ
1N4448
1N448
BC 560
BC 560
Out
250 kΩ
33 kΩ
1N448
39 kΩ
BC 550
470 kΩ
BC 550
33 kΩ
1N4448
BC 550B
1N4448
3.3 µF
100 Ω
39 kΩ
820 nF
4.7 kΩ
100 kΩ
1N4448
15 µF
BC 560

Unstable bias loop



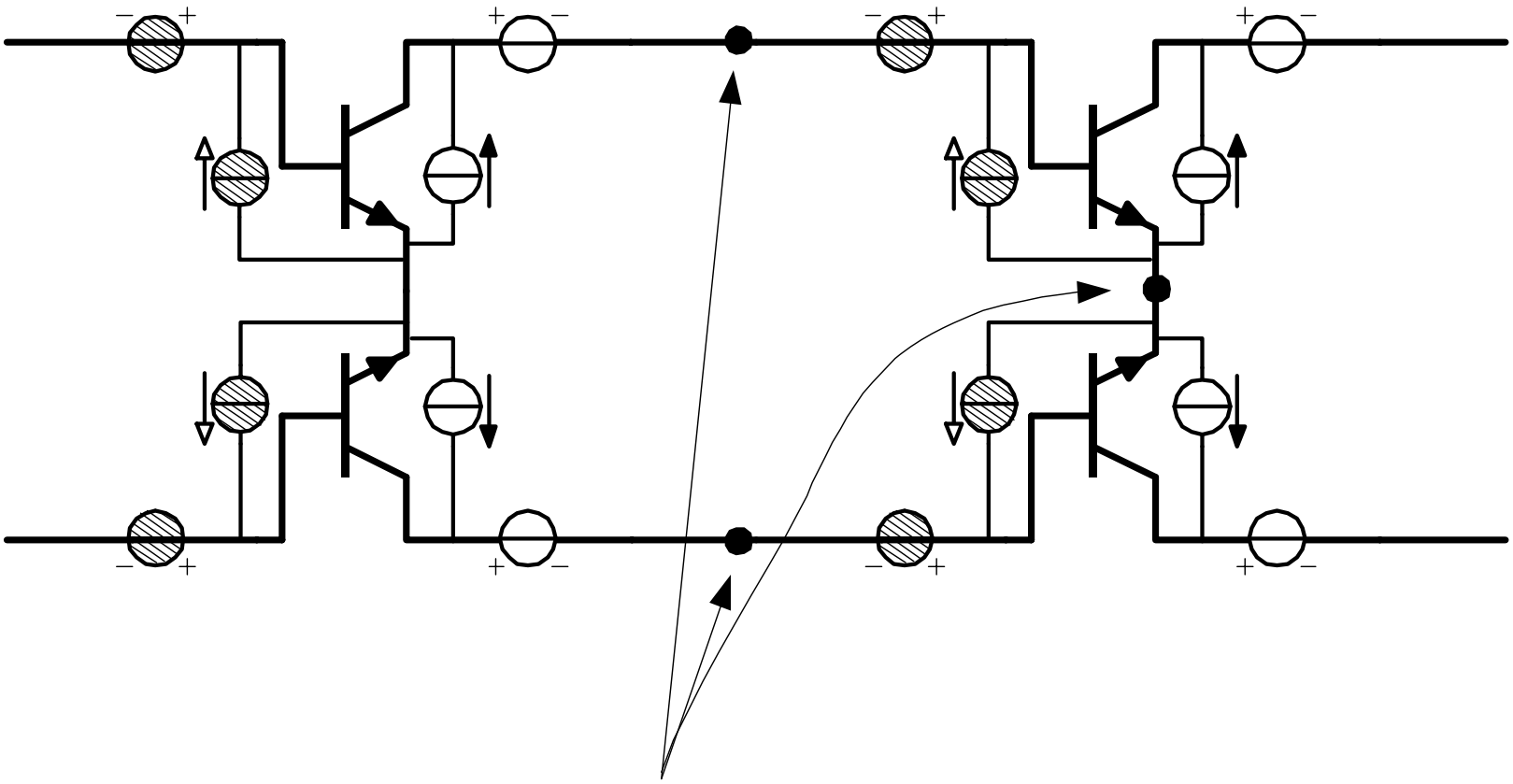
Frequency compensation bias loop



"Brute force" : $C_{biasfilter}$ large

"Delicate" : R_{Comp} **phantom zero**

Differential circuits

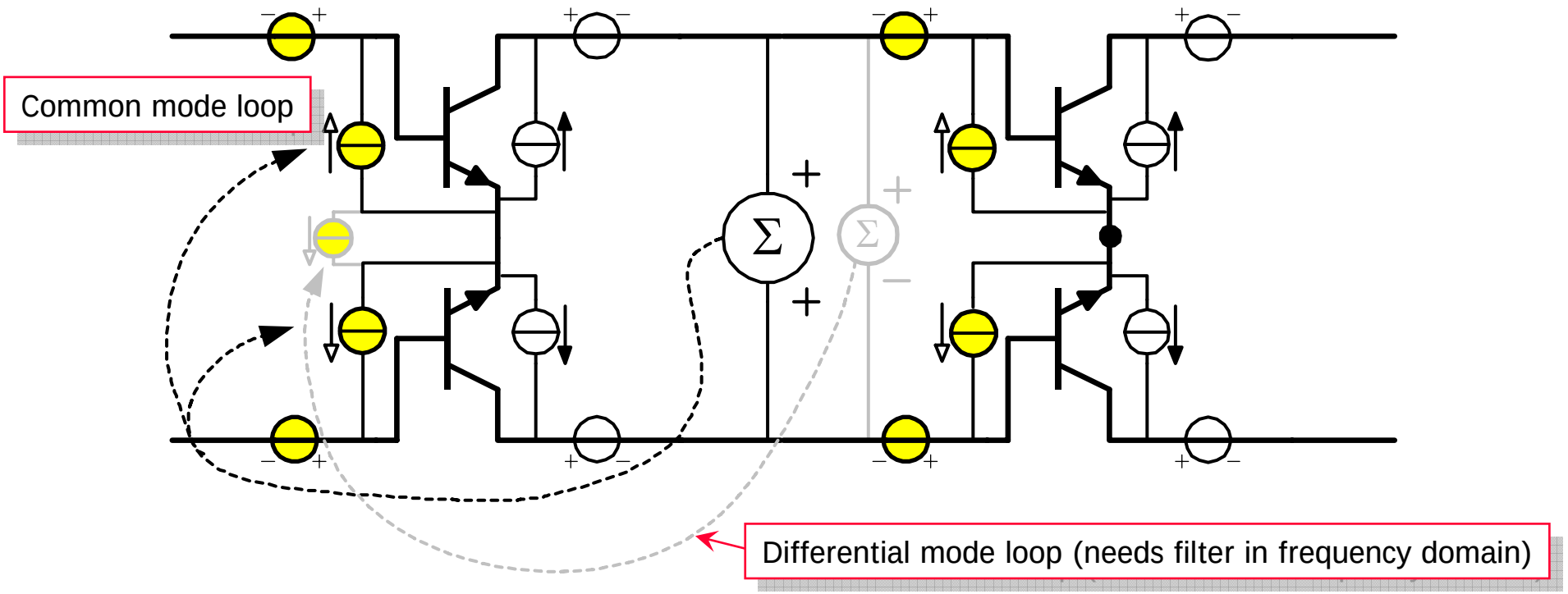


(b) Extra options that *can* be used as filter:

Nodes that carry no signal

Sum of node voltages that carries no signal

Differential/Common mode



Still 2 loops and 2 loop filters (1 in f domain, 1 to filter out common mode via adder)

Rely on matching, skip differential loop

Then no filter in frequency domain needed

Result: differential bias error

Summary of bias procedure

Insert bias sources

Reduce number of voltage control loops

Reduce number of current control loops

Shift voltage sources

Merge current sources

Implement current sensors

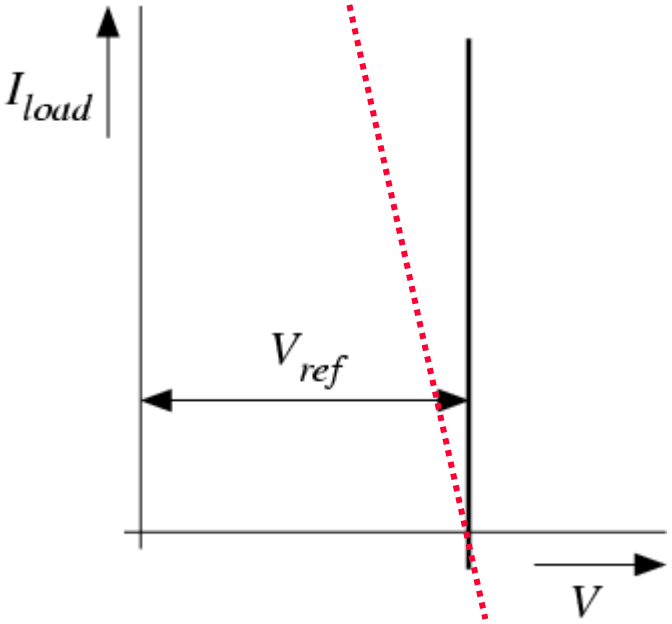
Try to implement local loops with capacitor

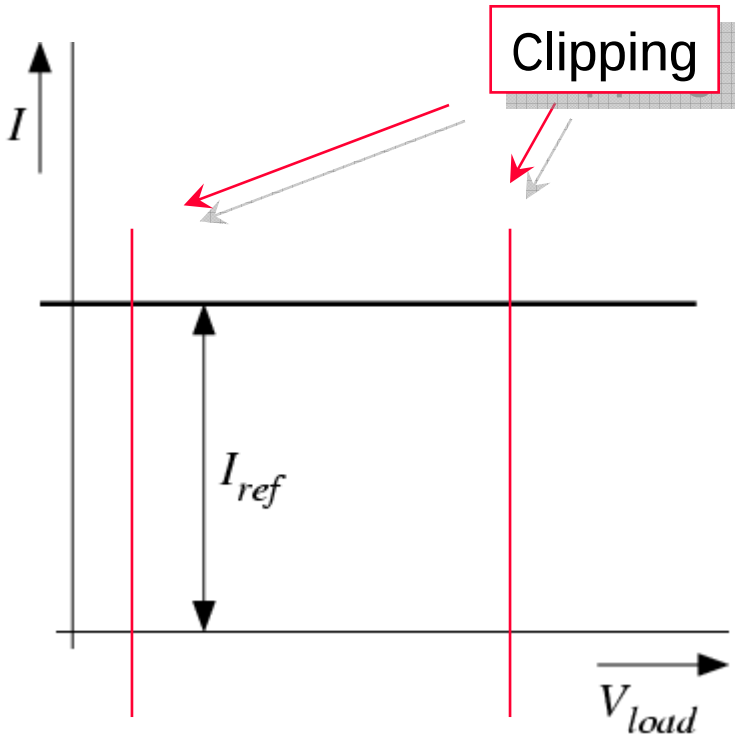
Implement bias filter

Do frequency compensation

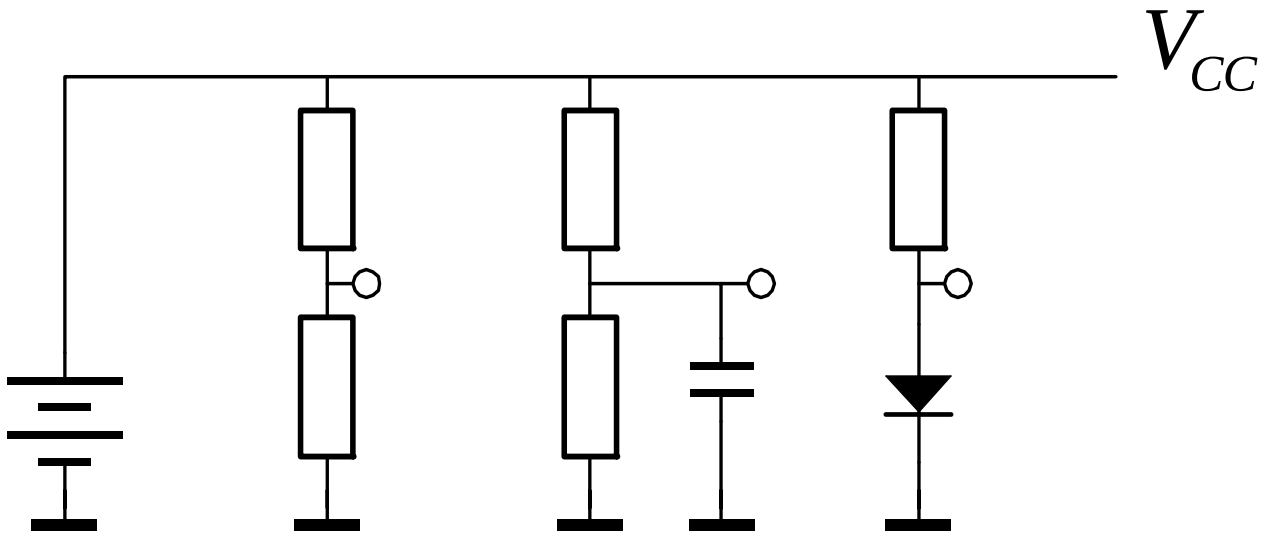
The finishing touch

Ideal sources



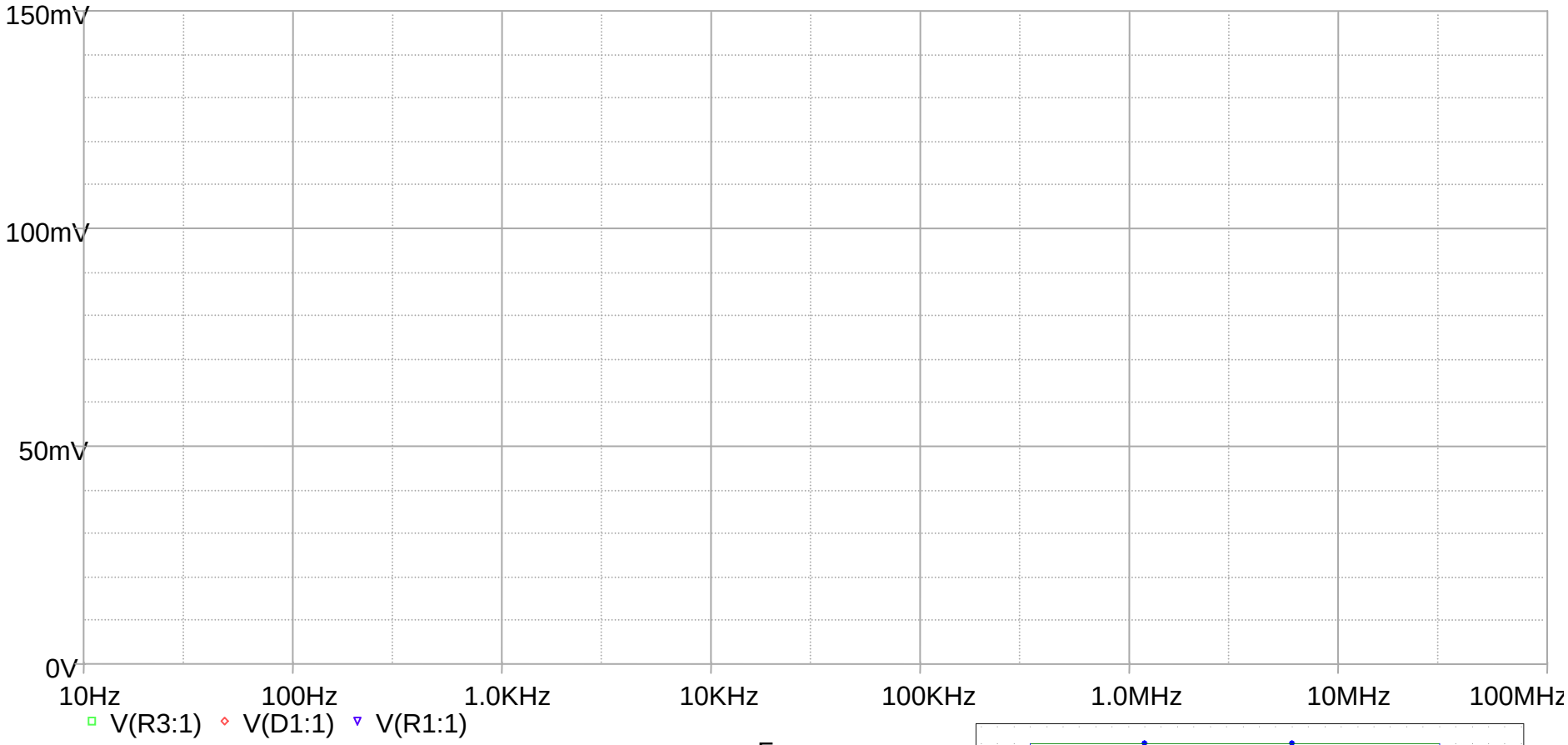


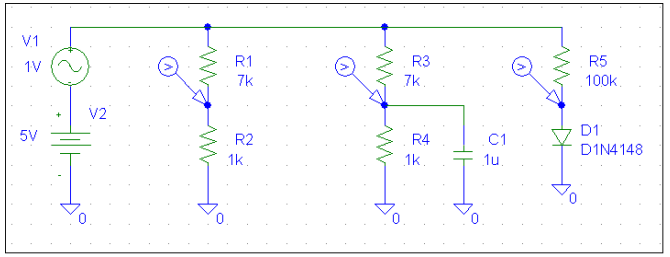
Practical voltage sources



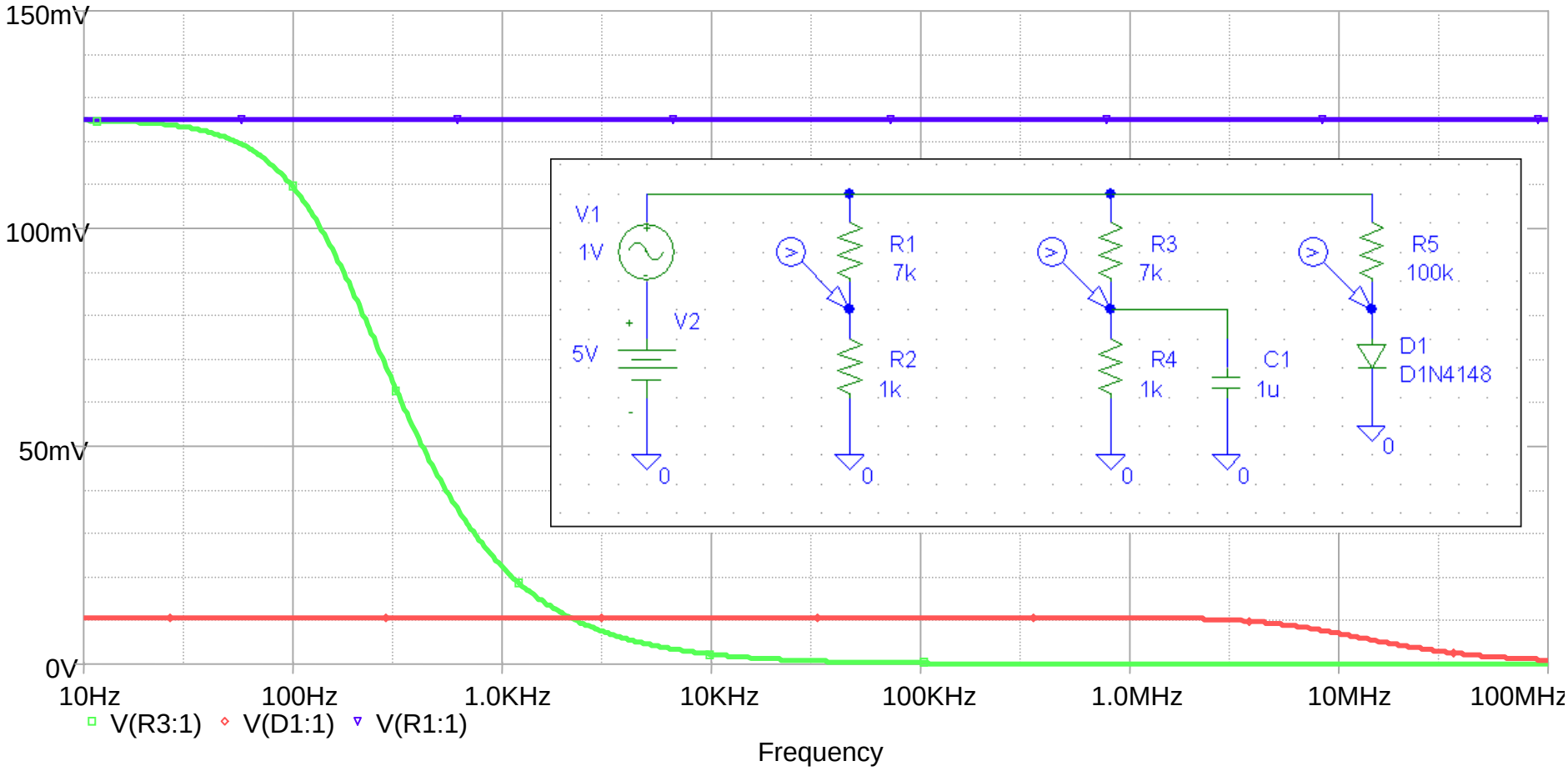
Battery
Voltage divider
Decoupled voltage divider
Non-linear voltage divider

Power supply rejection

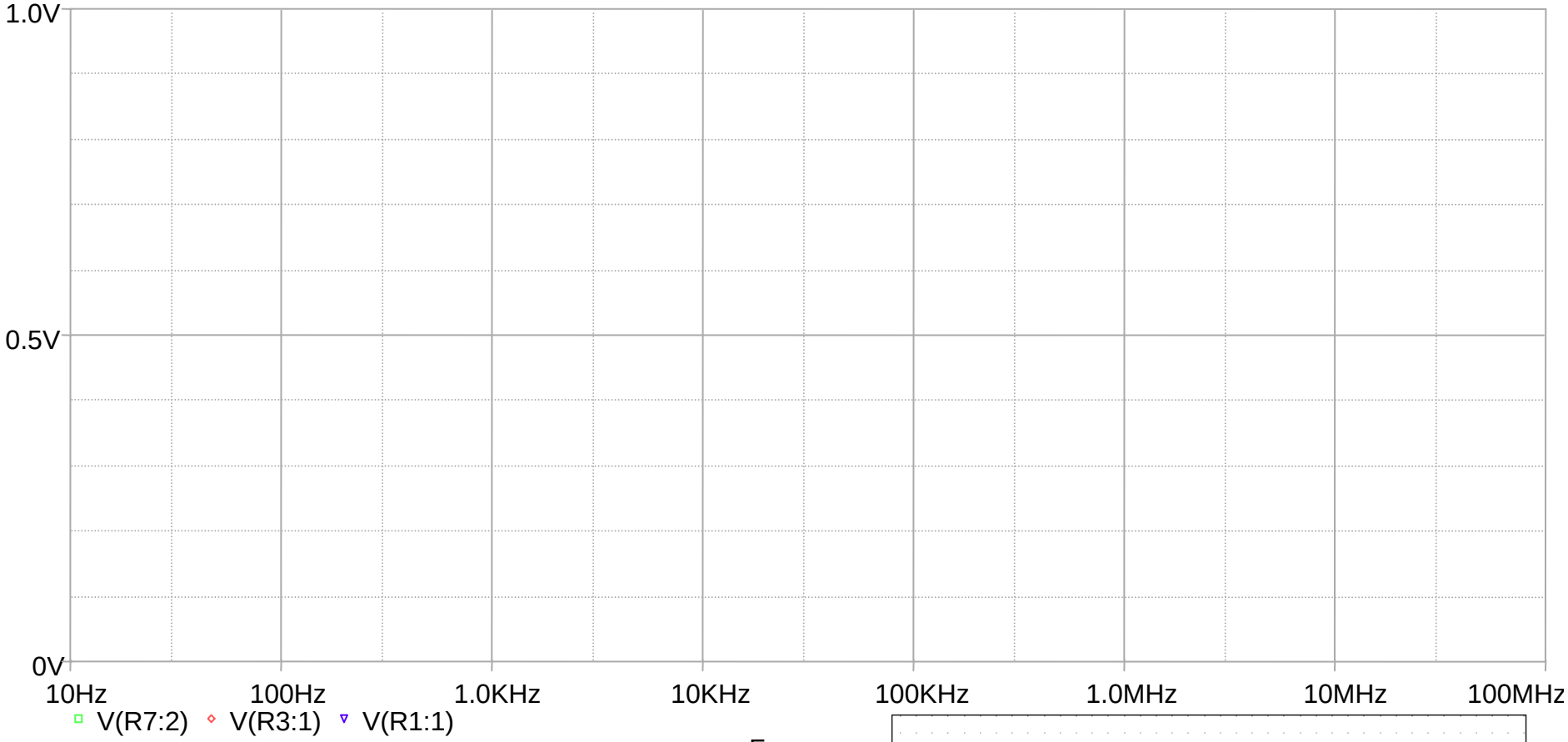


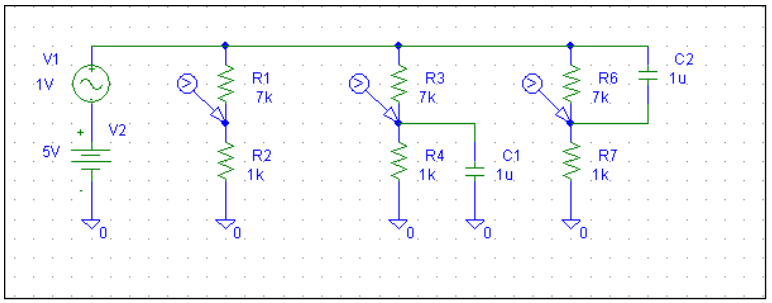


Power supply rejection

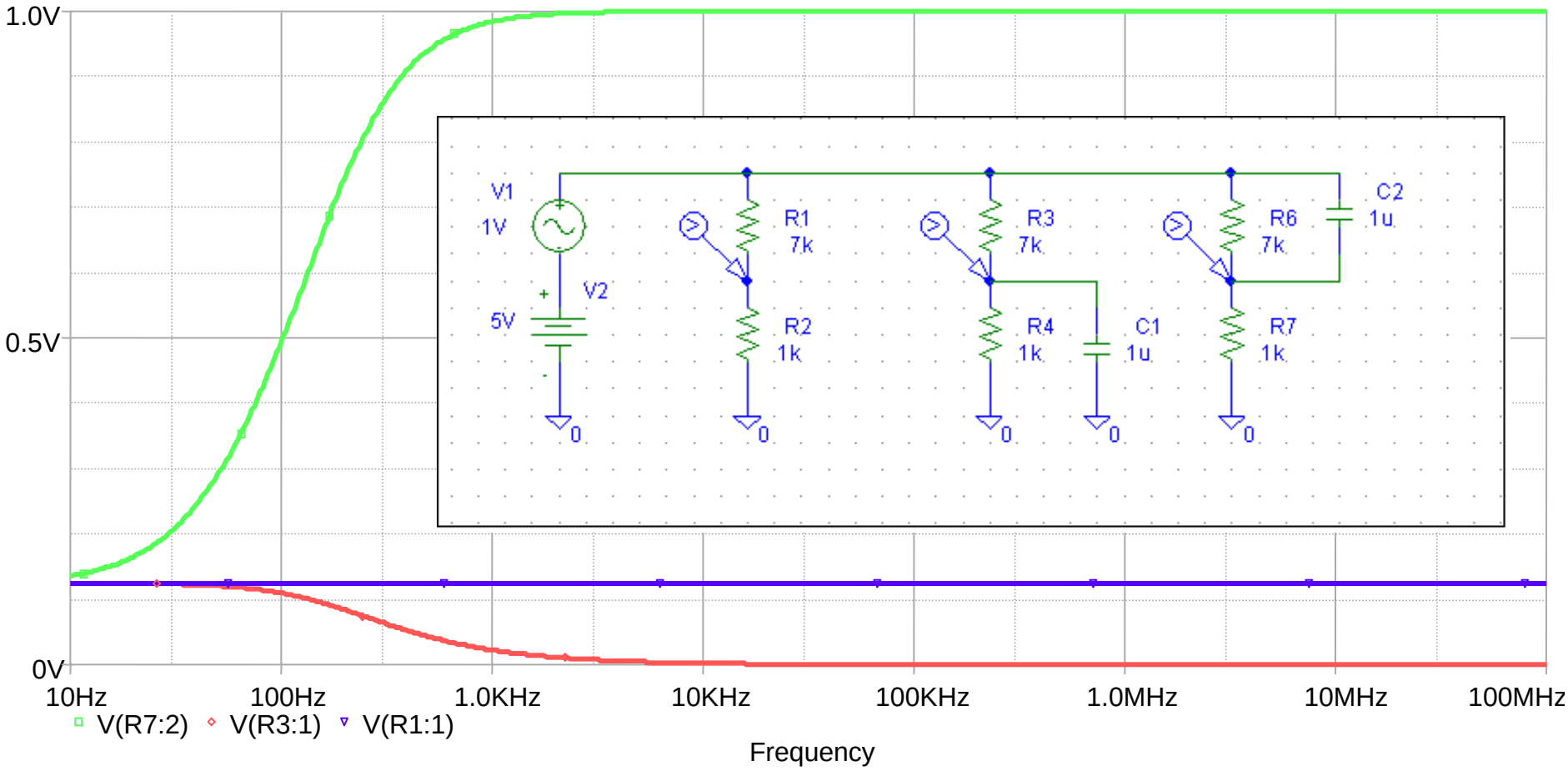


Decoupling…


1.0V
0.5V
0V
10Hz
100Hz
1.0KHz
10KHz
100KHz
1.0MHz
10MHz
100MHz
V(R7:2)
V(R3:1)
V(R1:1)
Frequency


V1
1V
V2
5V
R1
7k
R2
1k
R3
7k
R4
1k
C1
1u
R6
7k
R7
1k
C2
1u
0

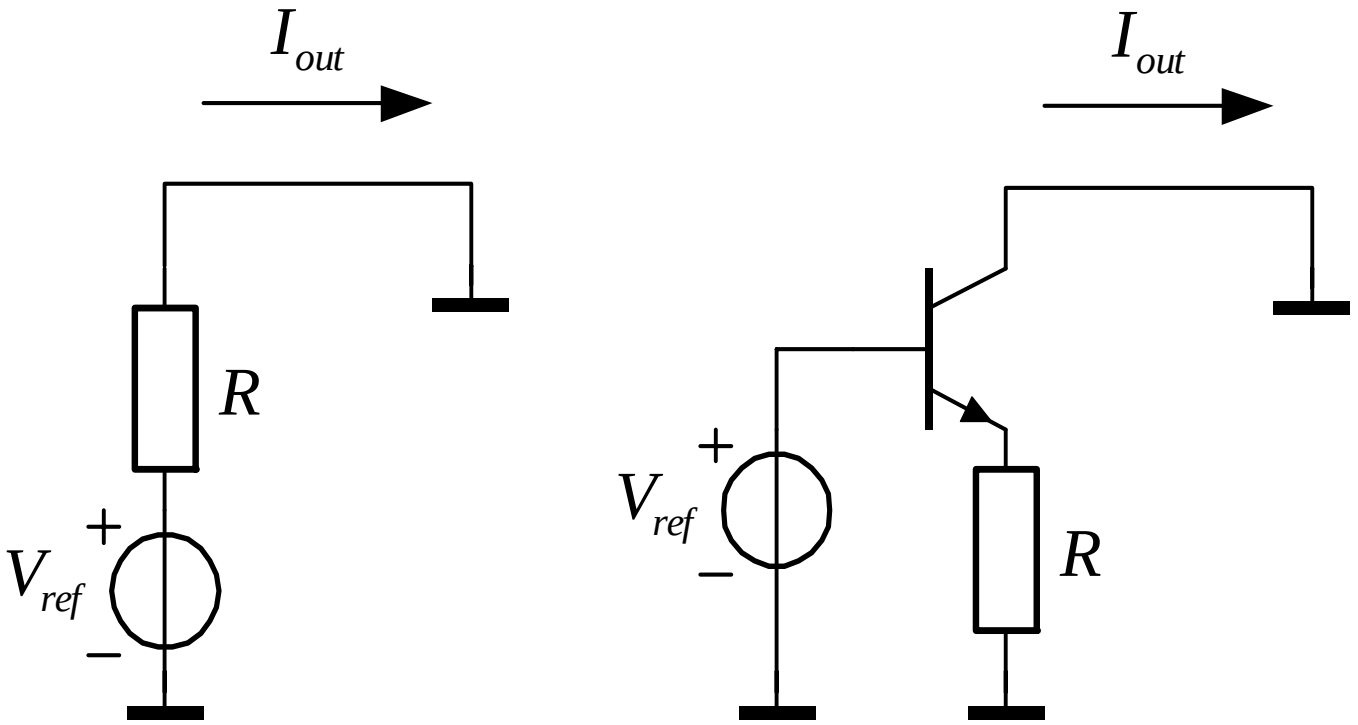
Decoupling…


1.0V
0.5V
0V
10Hz
100Hz
1.0KHz
10KHz
100KHz
1.0MHz
10MHz
100MHz
V(R7:2)
V(R3:1)
V(R1:1)
Frequency
V1
1V
V2
5V
R1
7k
R2
1k
R3
7k
R4
1k
C1
1u
R6
7k
R7
1k
C2
1u
0

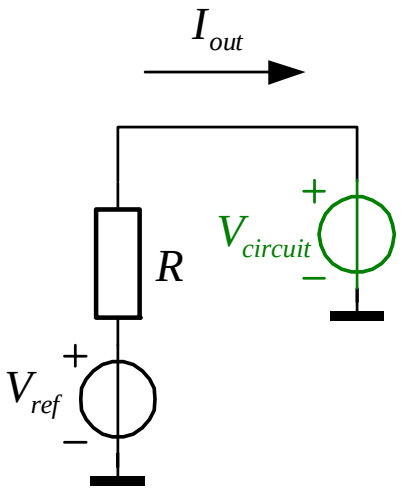
Current source: implementation

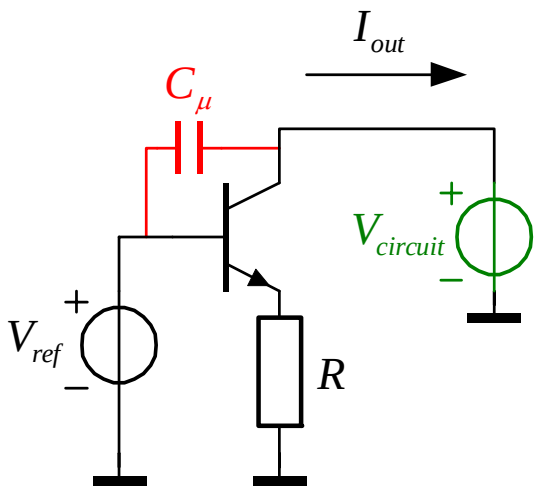
Resistor

Transistor



Influence on the circuit





$$I_{out} = \frac{\left(V_{ref} - V_{circuit}\right)}{R}$$

$$r_{out} = R$$

$$S_{i_n} = \frac{4kT}{R}$$

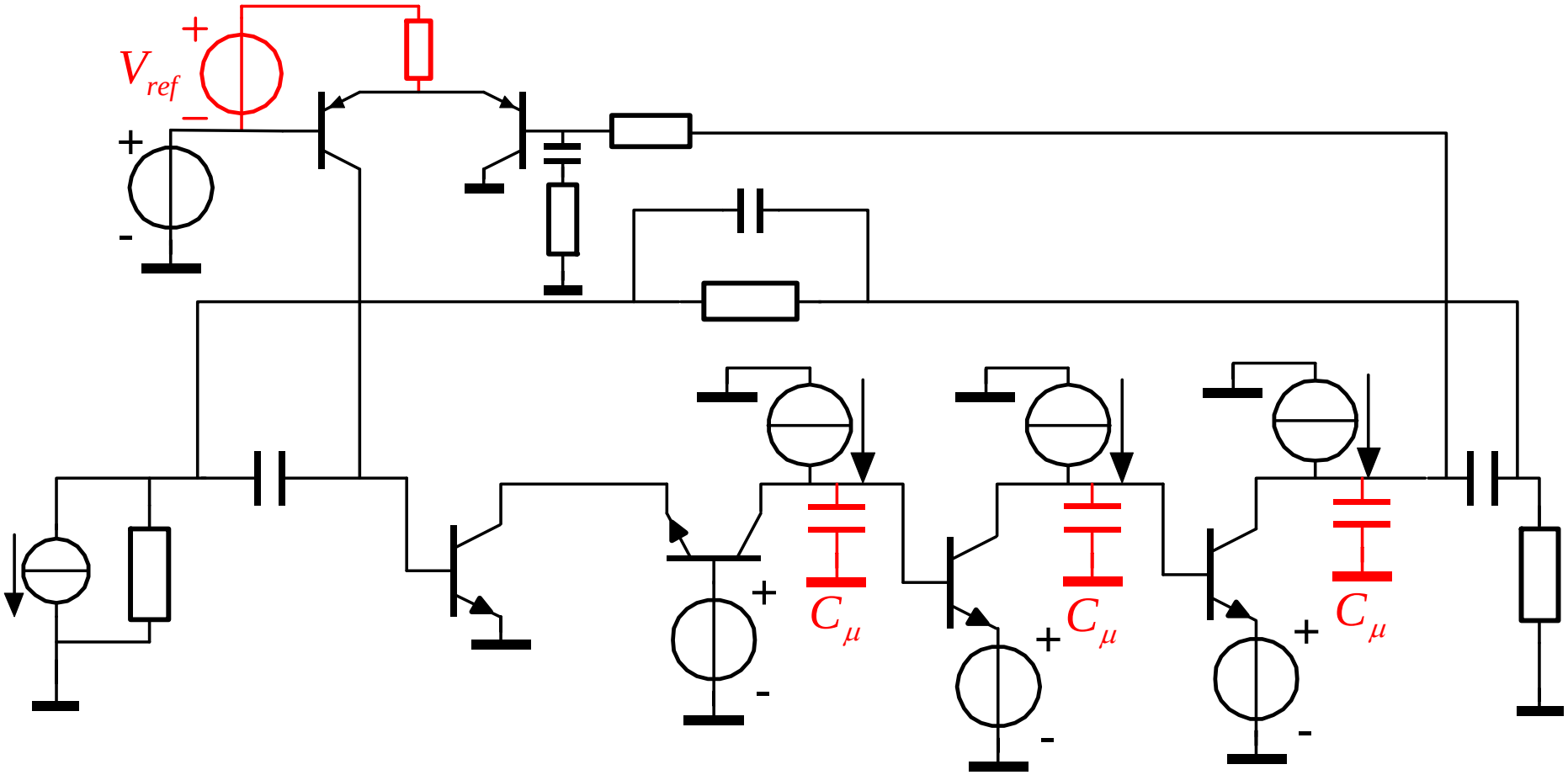
$$I_{out} = \frac{\left(V_{ref} - V_{be}\right)}{R}$$

$$r_{out} = \frac{r_o}{D} = \beta_f r_o$$

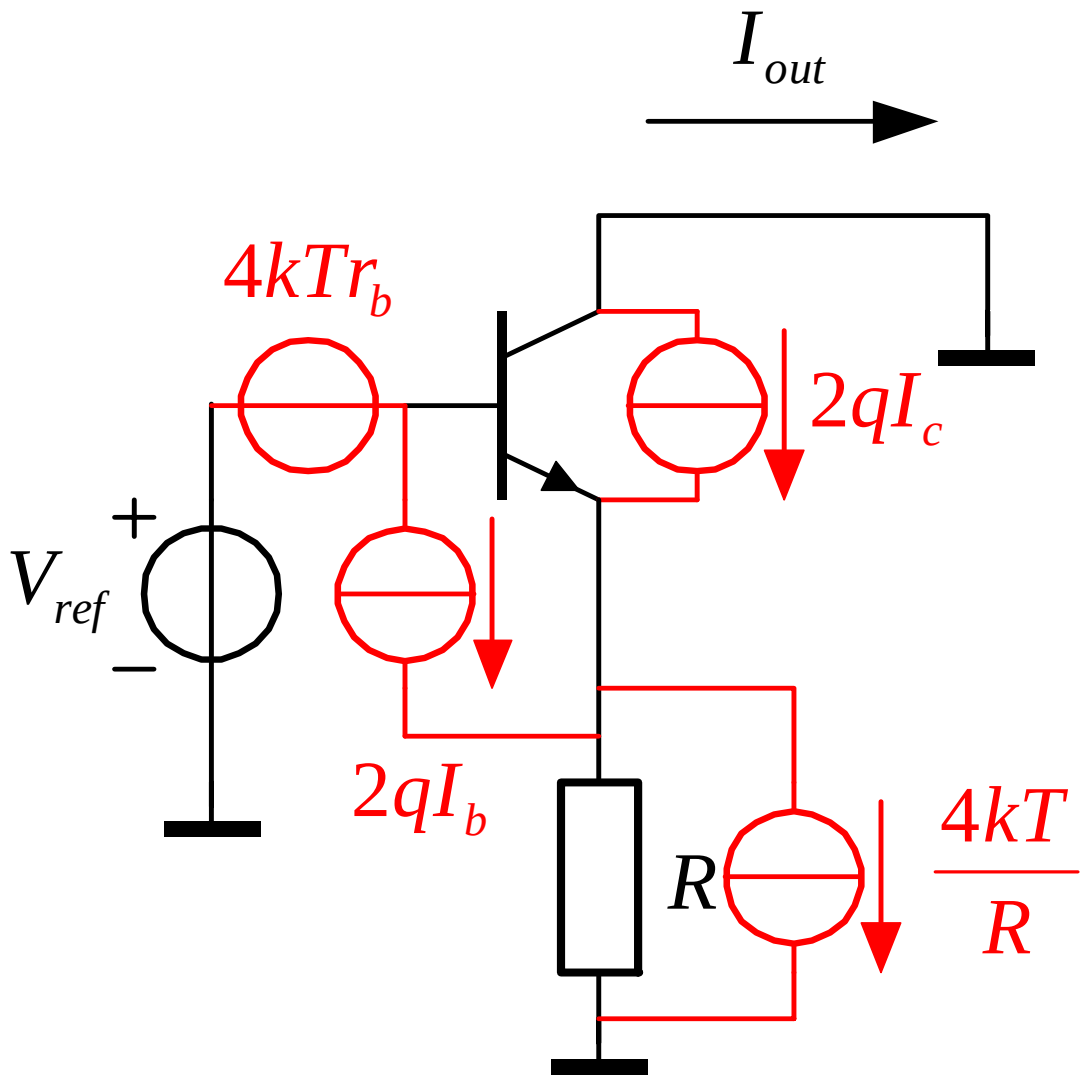
$$S_{i_n} = \frac{4kT}{R} + 2qI_b$$

Insert impedance only

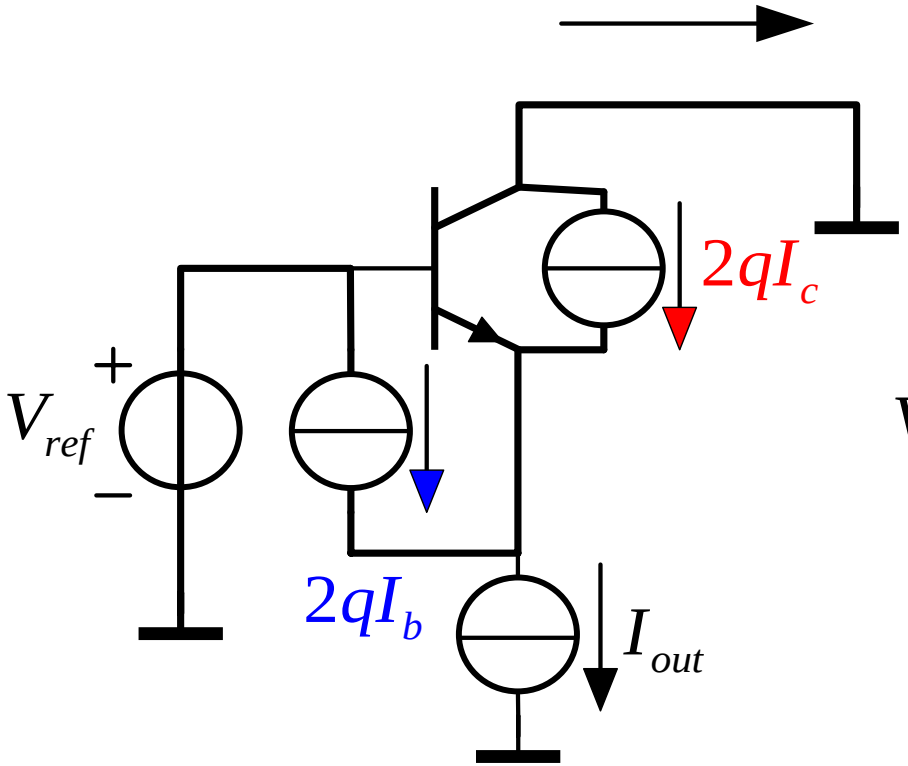
one by one...



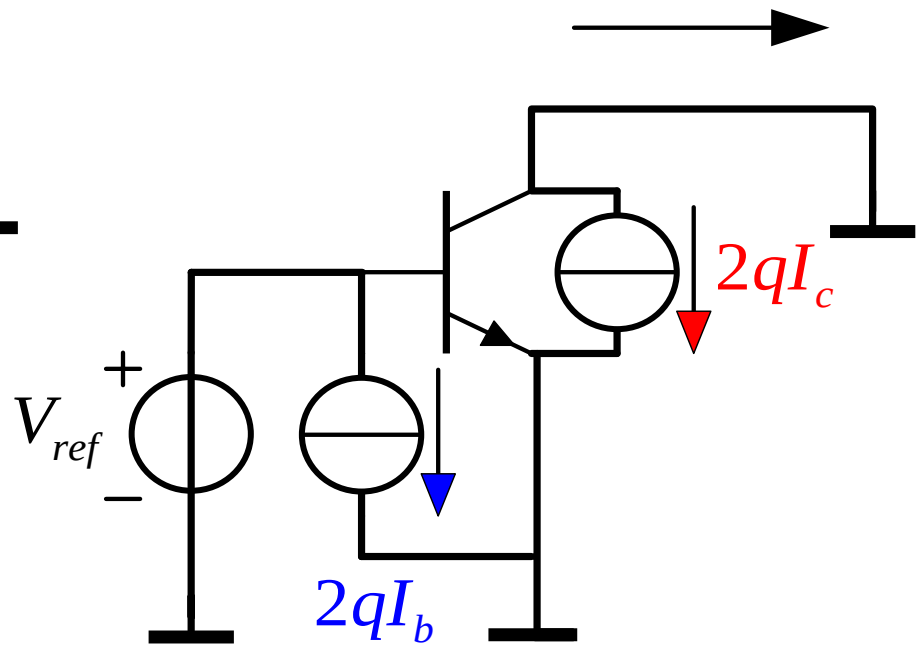
Current source: noise



Influence of R on noise

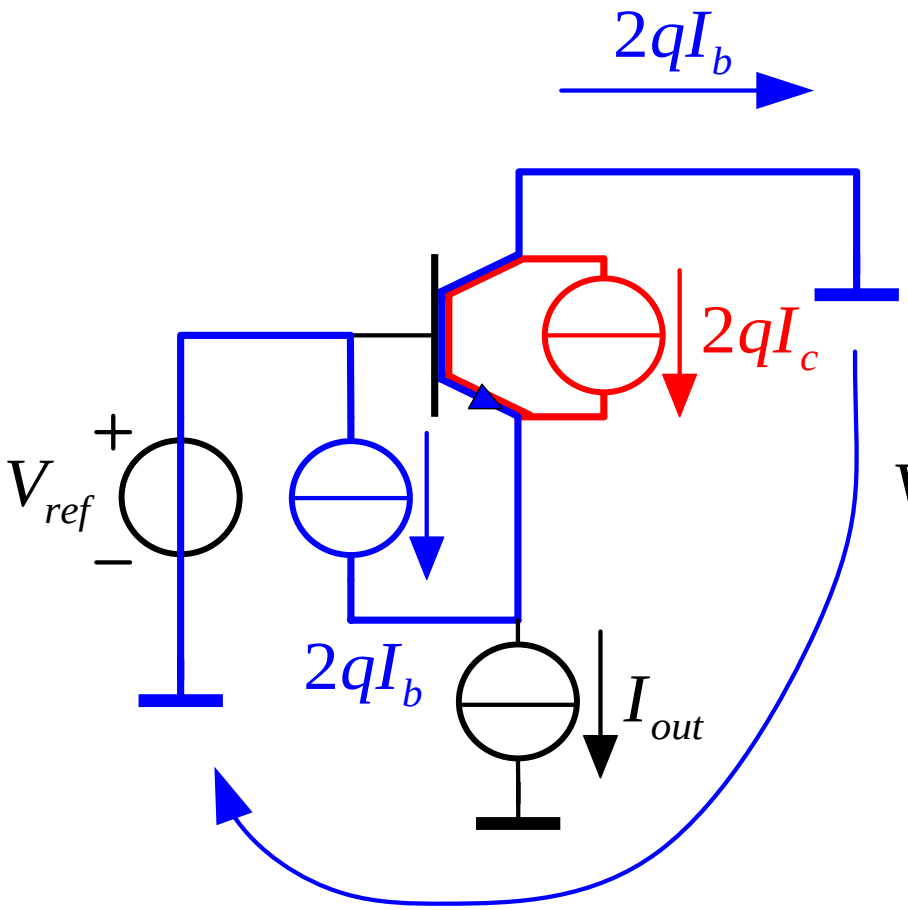


Extreme: $\lim R \to \infty$

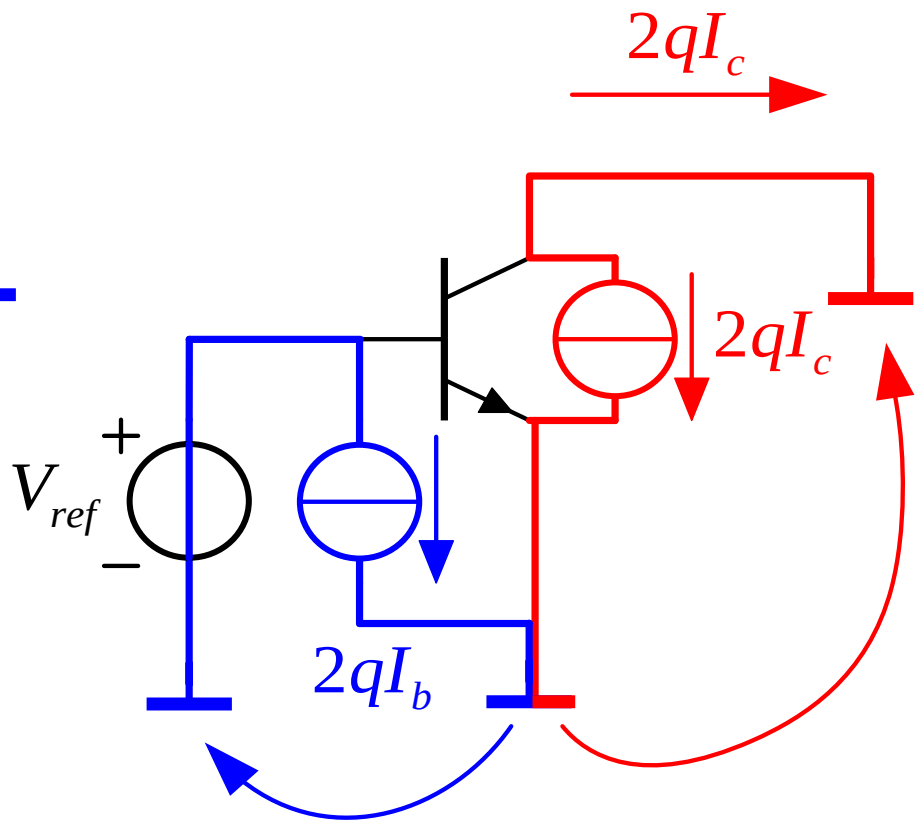


Extreme: $\lim R \to 0$

Influence of R on noise

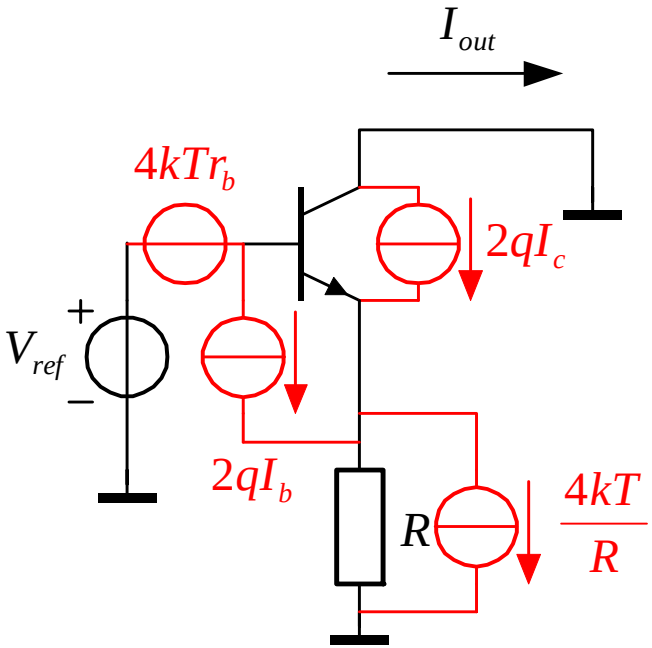


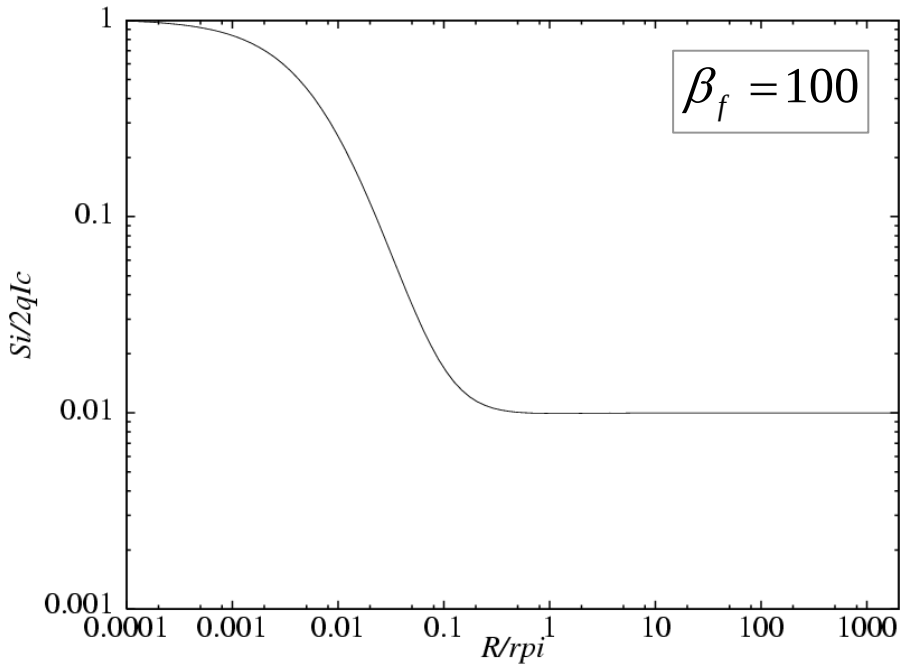
Extreme: $\lim R \to \infty$



Extreme: $\lim R \to 0$

Current source: noise





$$S_{i_{out}} = \frac{2qI_c}{\left(1+\frac{\beta_f R}{r_\pi}\right)^2} + \frac{2qI_b}{\left(1+\frac{r_\pi}{\beta_f R}\right)^2} + \frac{4kT(R+r_b)}{\left(R+\frac{r_\pi}{\beta_f}\right)^2}$$

Noise resistor = Shot noise

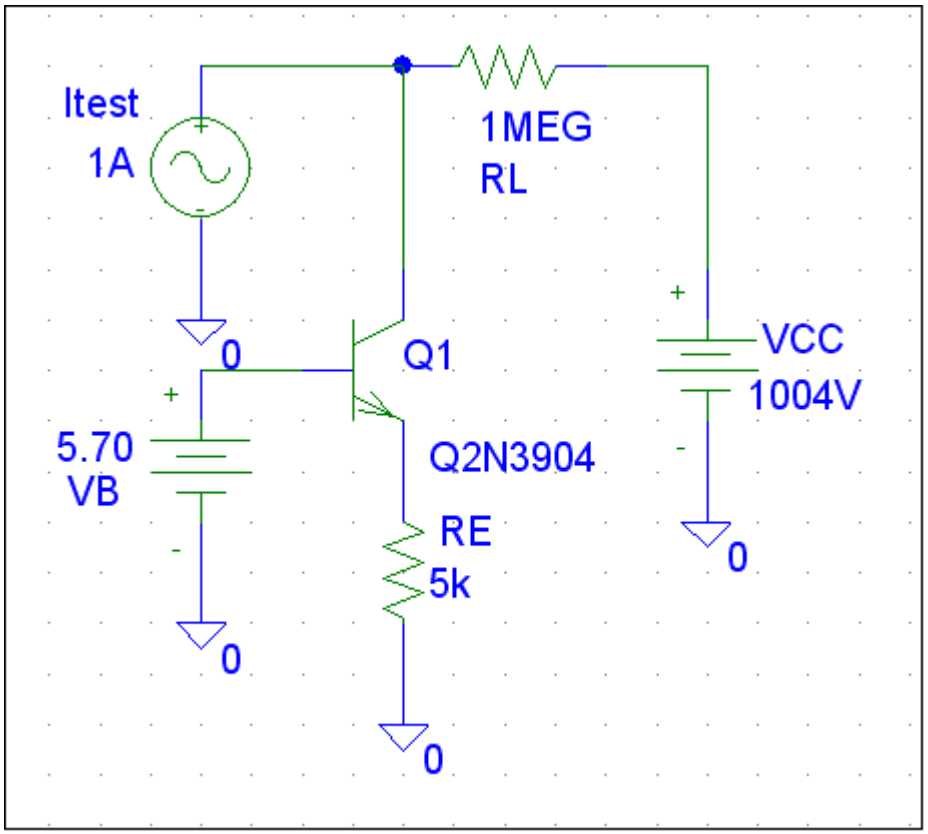
$$\frac{2qI_c}{\left(1+\frac{\beta_f R}{r_\pi}\right)^2}+\frac{2qI_b}{\left(1+\frac{r_\pi}{\beta_f R}\right)^2}=\frac{4kTR}{\left(R+\frac{r_\pi}{\beta_f}\right)^2}$$

$$R=2r_\pi \Rightarrow V_R=I_{out}R\approx 5\text{V}$$

$\beta_f=100$

$\frac{kT}{q}\approx 26\text{mV}$

Simulation



**** TRANSISTOR SQUARED NOISE VOLTAGES (SQ V/HZ)

RB	1.313E-17
RC	1.496E-20
RE	0.000E+00
IBSN	**6.280E-15**
IC	1.095E-16
IBFN	0.000E+00
TOTAL	**6.403E-15**

**** RESISTOR SQUARED NOISE VOLTAGES (SQ V/HZ)

	R_RL	R_RE
TOTAL	4.116E-17	**8.040E-15**

**** TOTAL OUTPUT NOISE VOLTAGE = **1.448E-14** SQ V/HZ
= 1.204E-07 V/RT HZ

Simulation output

**** TRANSISTOR SQUARED NOISE VOLTAGES (SQ V/HZ)

RB	1.313E-17
RC	1.496E-20
RE	0.000E+00
IBSN	**6.280E-15**
IC	1.095E-16
IBFN	0.000E+00

(5 kΩ)

TOTAL **6.403E-15**

**** RESISTOR SQUARED NOISE VOLTAGES (SQ V/HZ)

	R_RL	R_RE
TOTAL	4.116E-17	**8.040E-15**

**** TOTAL OUTPUT NOISE VOLTAGE = **1.448E-14** SQ V/HZ
= 1.204E-07 V/RT HZ

**** TRANSISTOR SQUARED NOISE VOLTAGES (SQ V/HZ)

RB	**1.754E-12**
RC	1.389E-20
RE	0.000E+00
IBSN	2.107E-15
IC	**2.310E-12**
IBFN	0.000E+00

(0 Ω)

TOTAL **4.066E-12**

**** RESISTOR SQUARED NOISE VOLTAGES (SQ V/HZ)

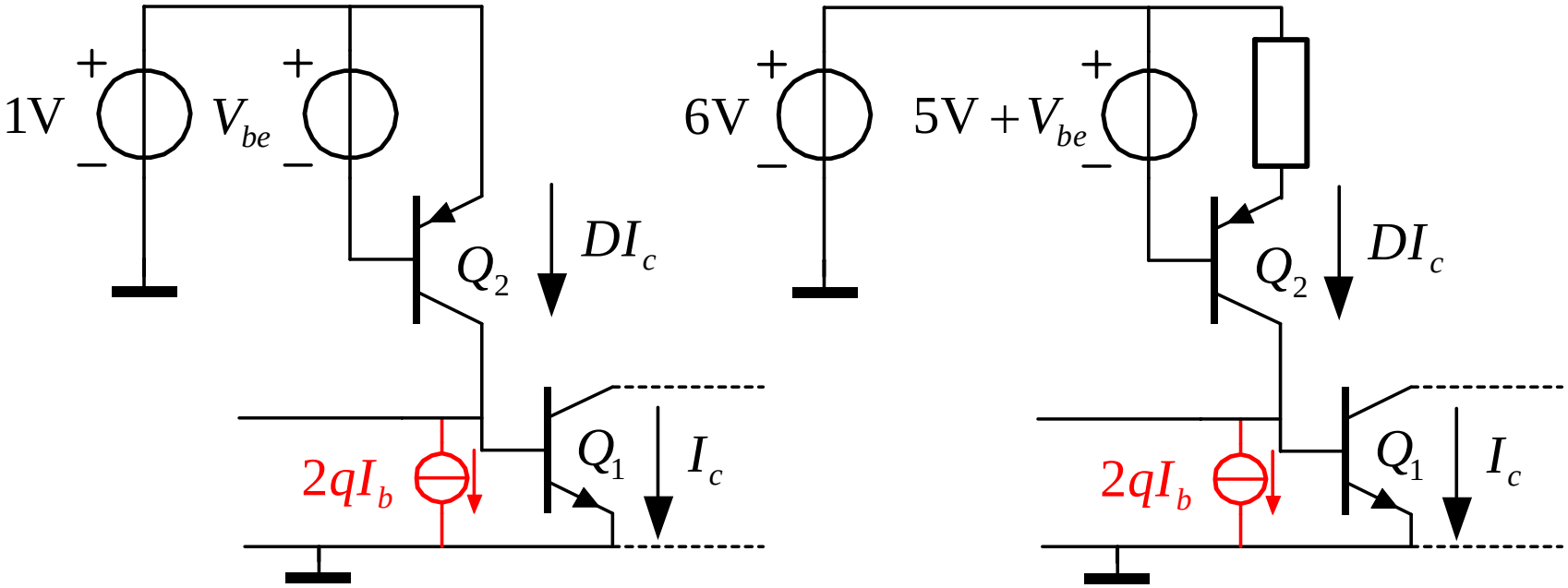
	R_RL
TOTAL	1.183E-16

**** TOTAL OUTPUT NOISE VOLTAGE = **4.066E-12** SQ V/HZ
= 2.017E-06 V/RT HZ

Low power – Low voltage

Injected noise: $2qDI_c = 2qI_b$

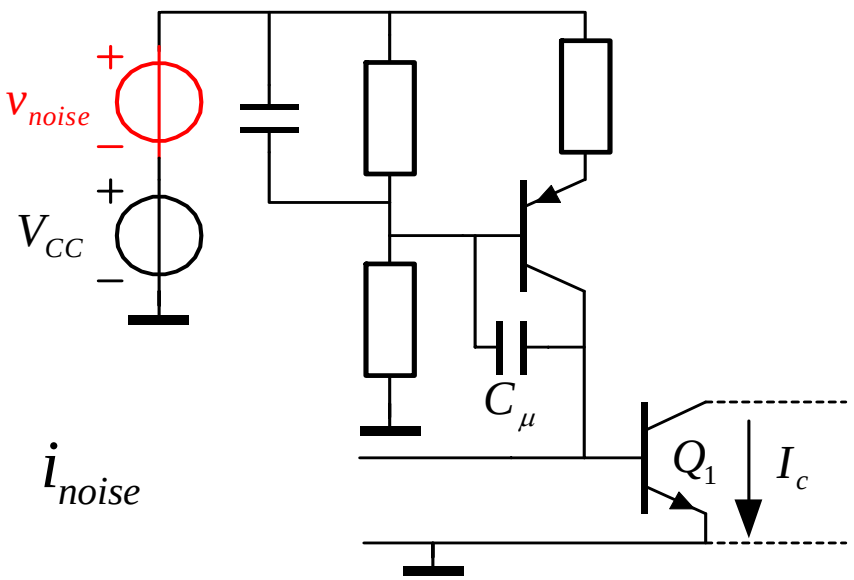
Injected noise: $\approx 4qD_I\left(DI_c\right) = 4qD_I I_b$



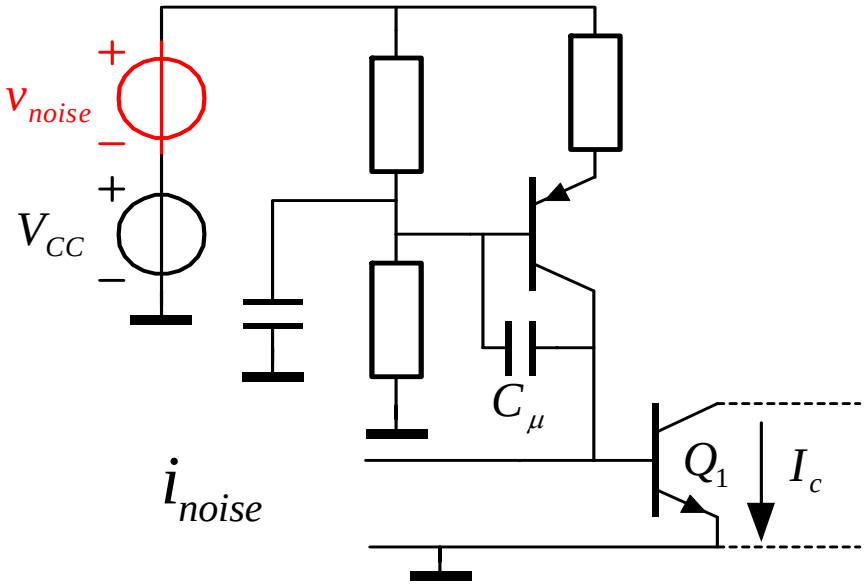
Double noise current

Negligible effect

Current source: power supply rejection

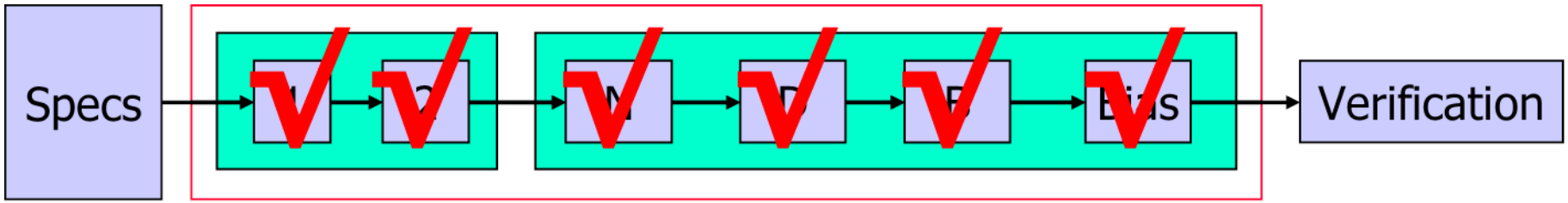


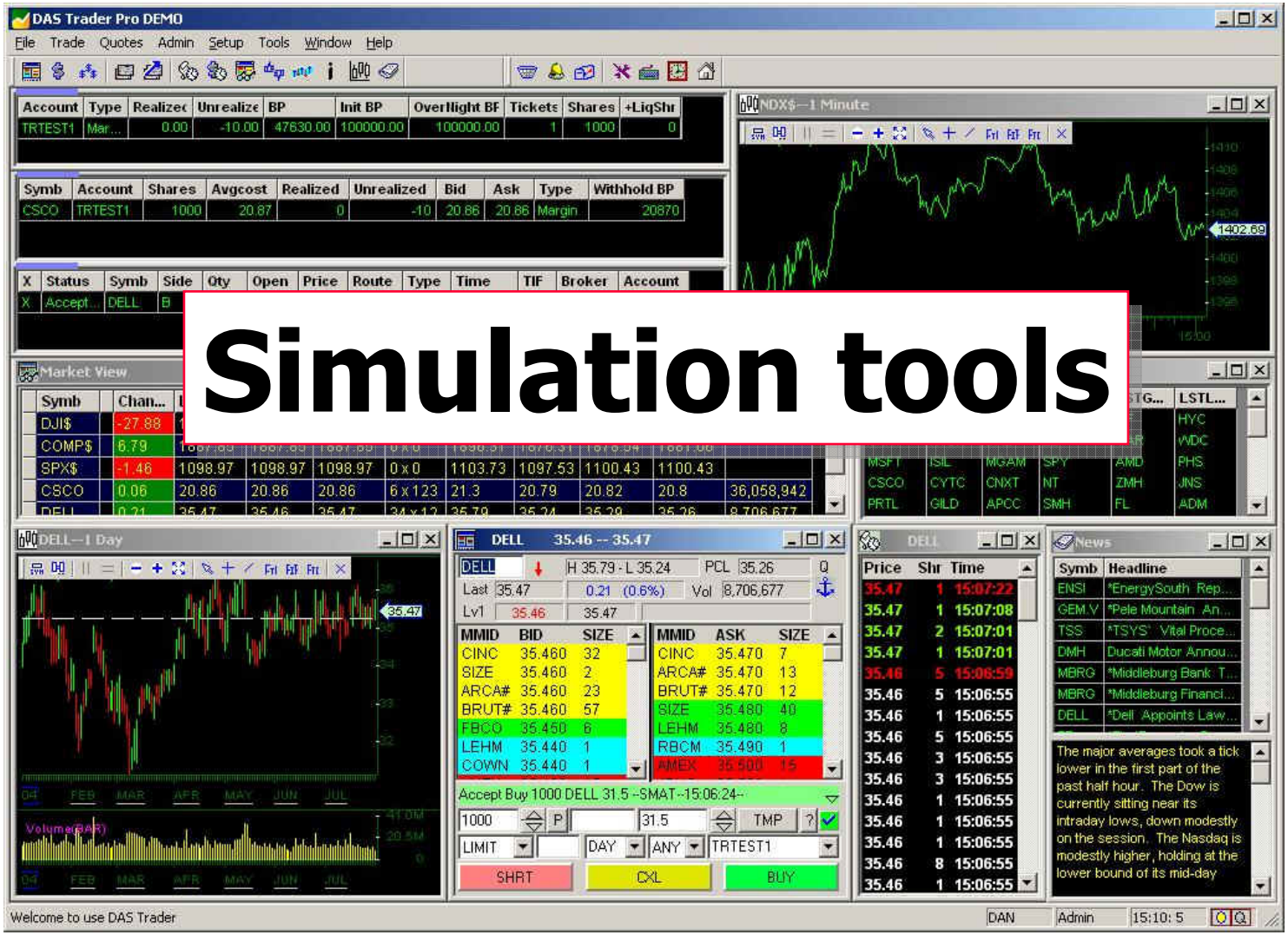
Only HF injection



Wide-band injection

Cascode does **not** reduce the effect


Specs
Verification


DAS Trader Pro DEMO
File Trade Quotes Admin Setup Tools Window Help
Simulation tools
Welcome to use DAS Trader

Simulation

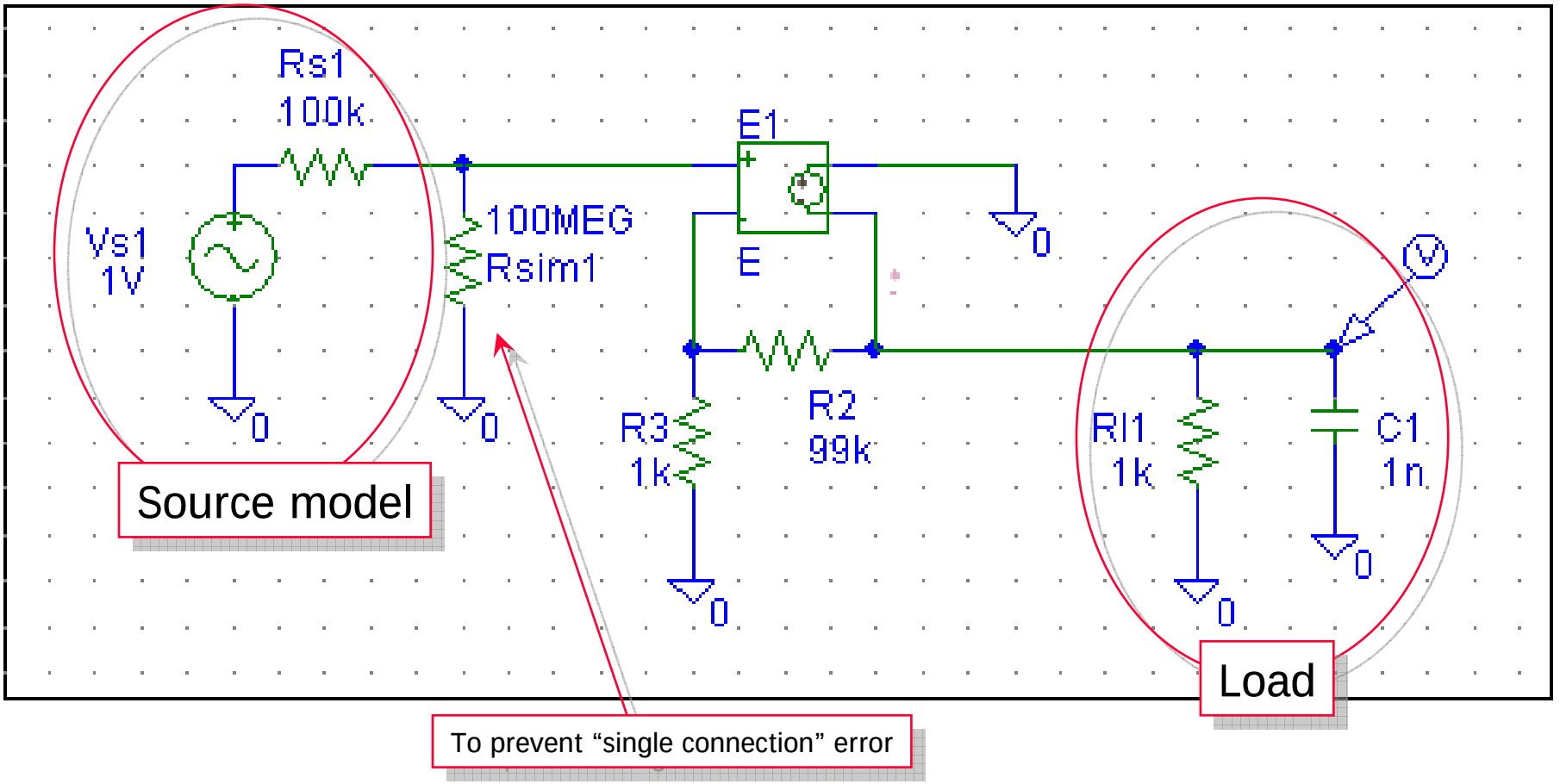
After design ☺

During the design

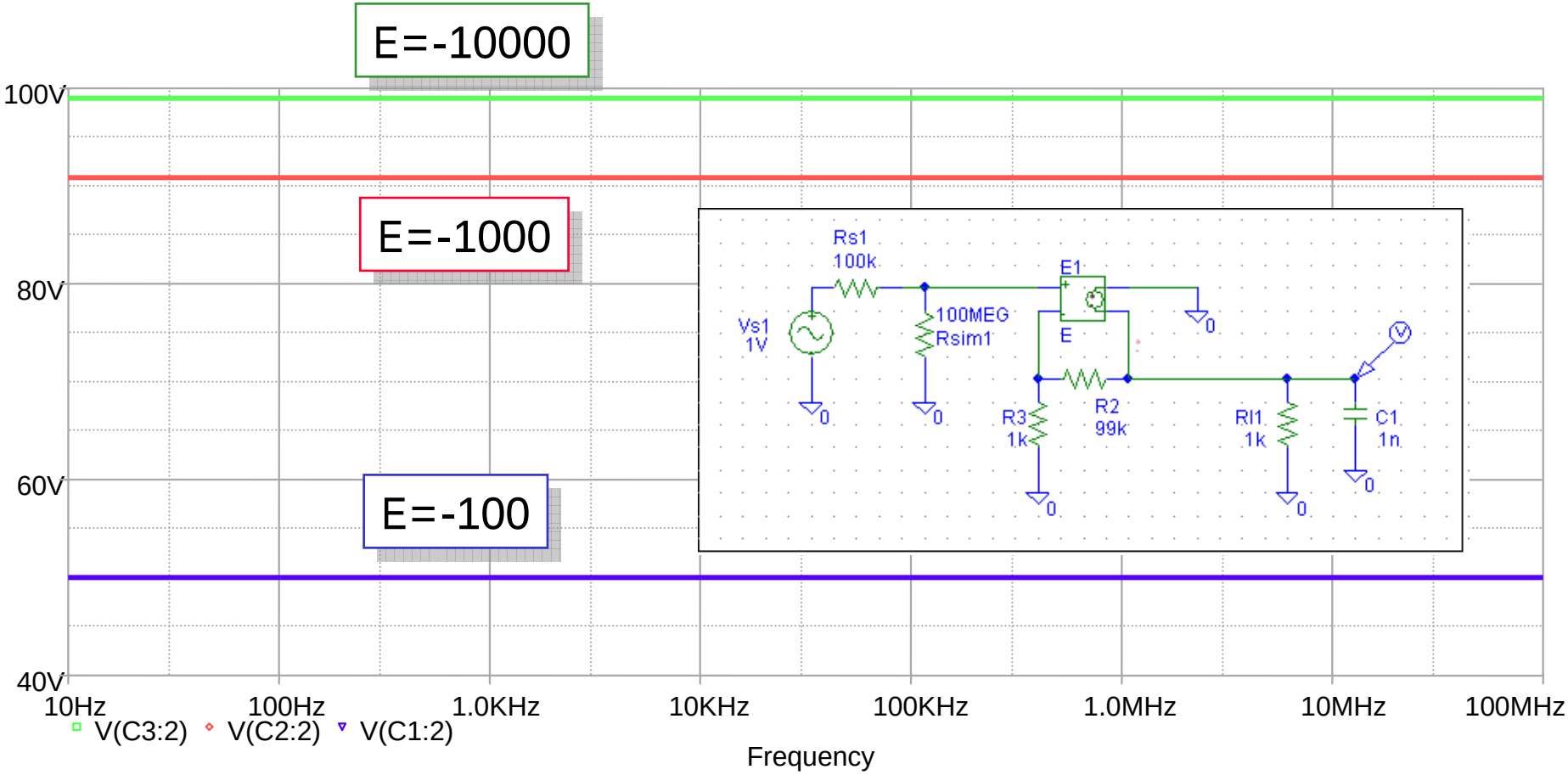
Simulation result is never a surprise

Nullator and norrator

- Voltage amplifier
- E-type nullor implementation is first choice

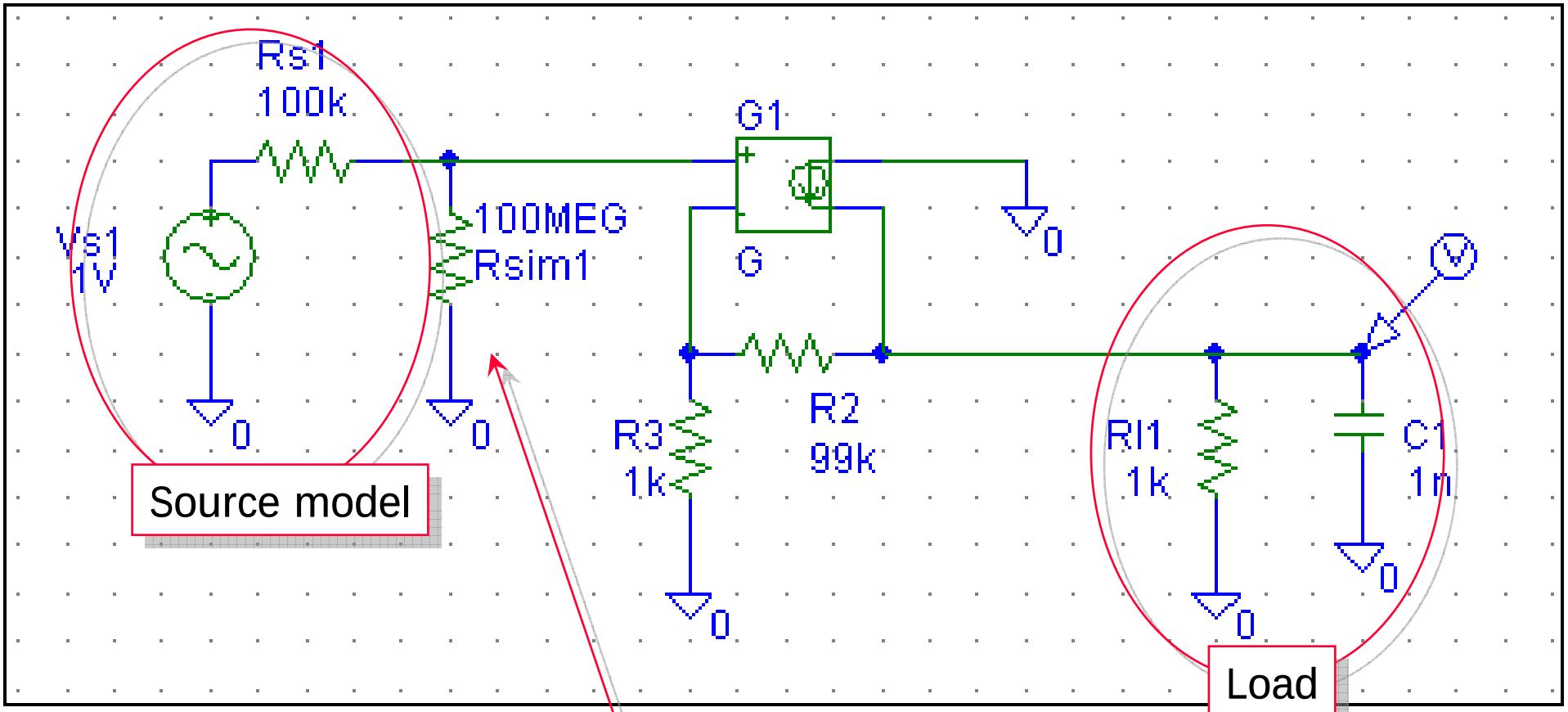


Simulation result

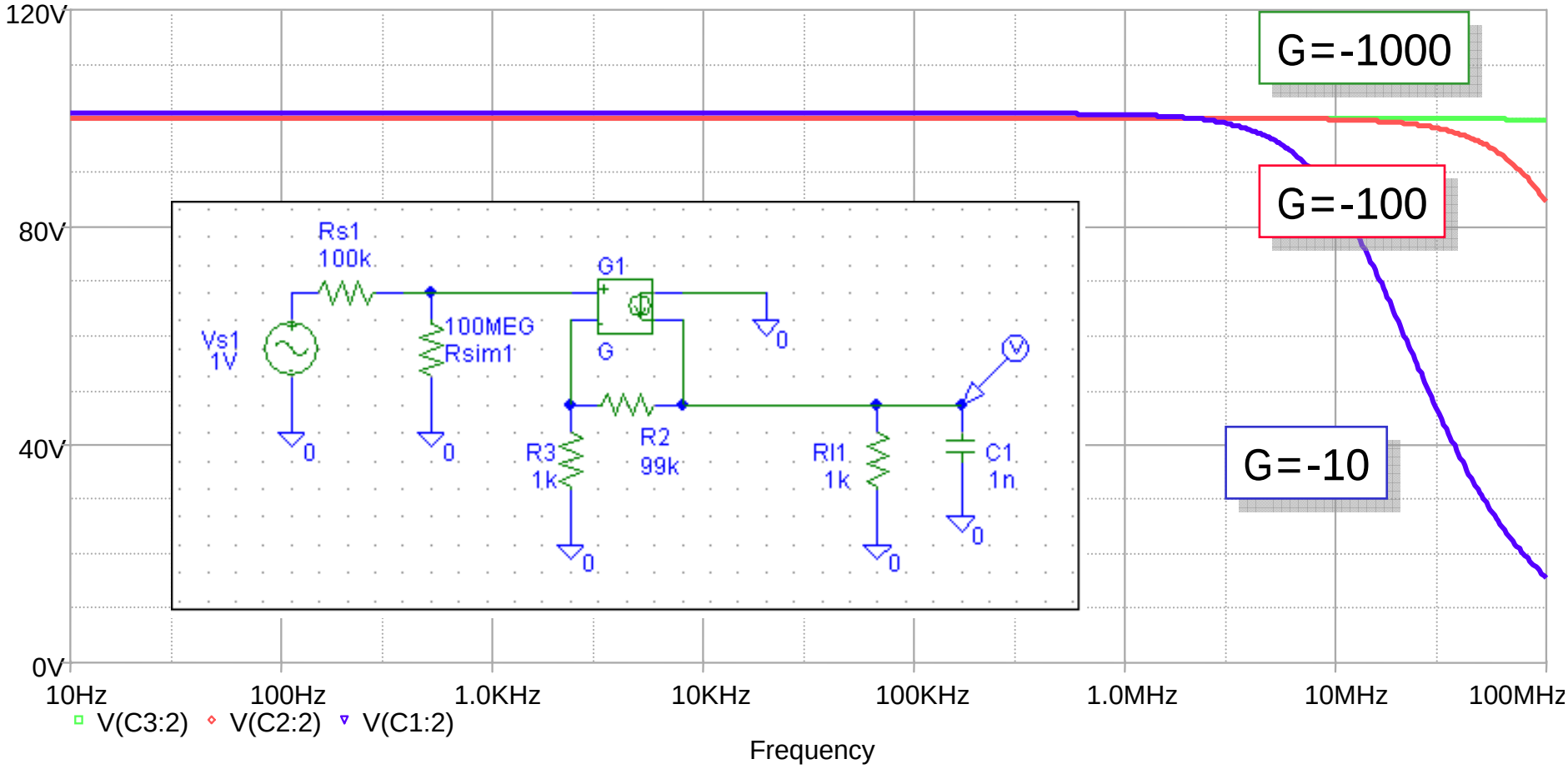


Nullator and norrator

- Voltage amplifier
- G-type nullor implementation

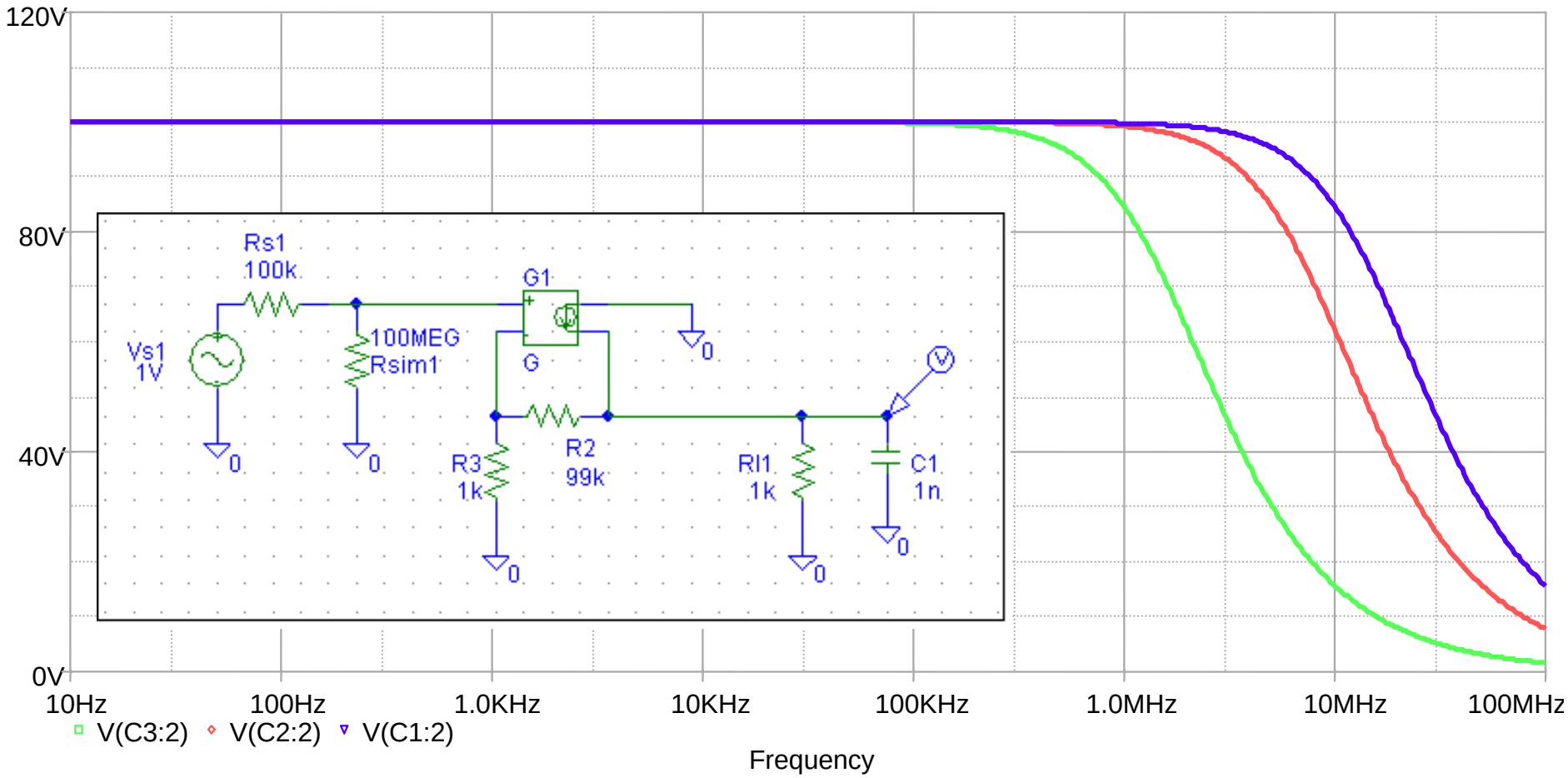


Simulation results

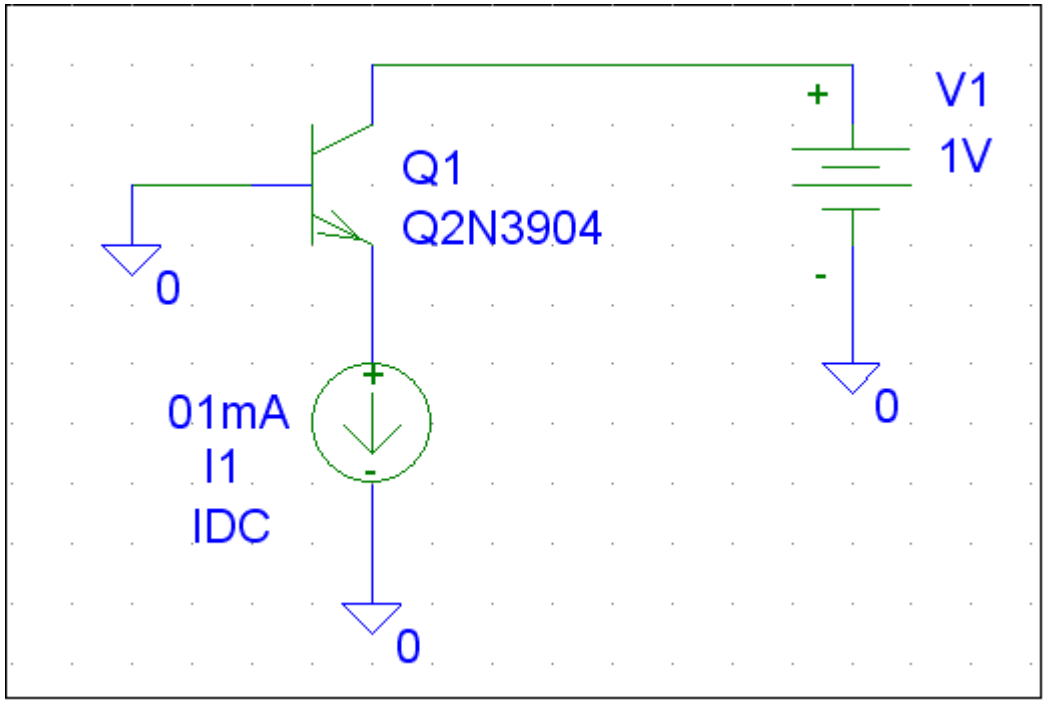


Simulation results

G=-100, C1=10n, 20n 100n



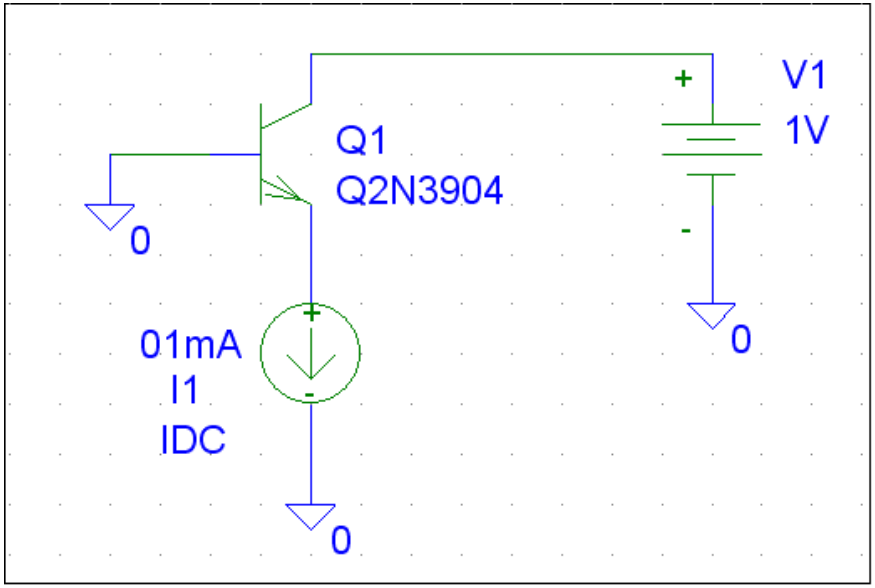
Transistor parameters



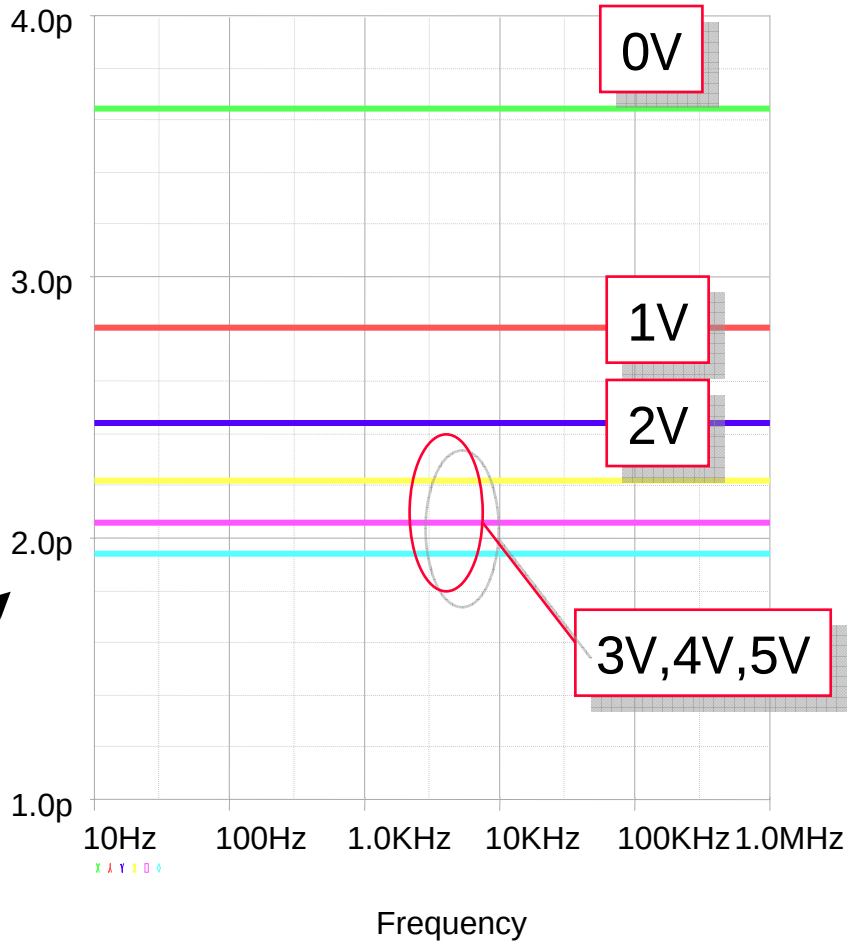
**** BIPOLAR JUNCTION TRANSISTORS

NAME	Q_Q1
MODEL	Q2N3904
IB	7.39E-06
IC	9.93E-04
VBE	6.65E-01
VBC	-1.00E+00
VCE	1.67E+00
BETADC	1.34E+02
GM	**3.78E-02**
RPI	**4.06E+03**
RX	1.00E+01
RO	7.56E+04
CBE	**1.79E-11**
CBC	**2.80E-12**
CJS	0.00E+00
BETAAC	**1.54E+02**
CBX/CBX2	0.00E+00
FT/FT2	**2.91E+08**

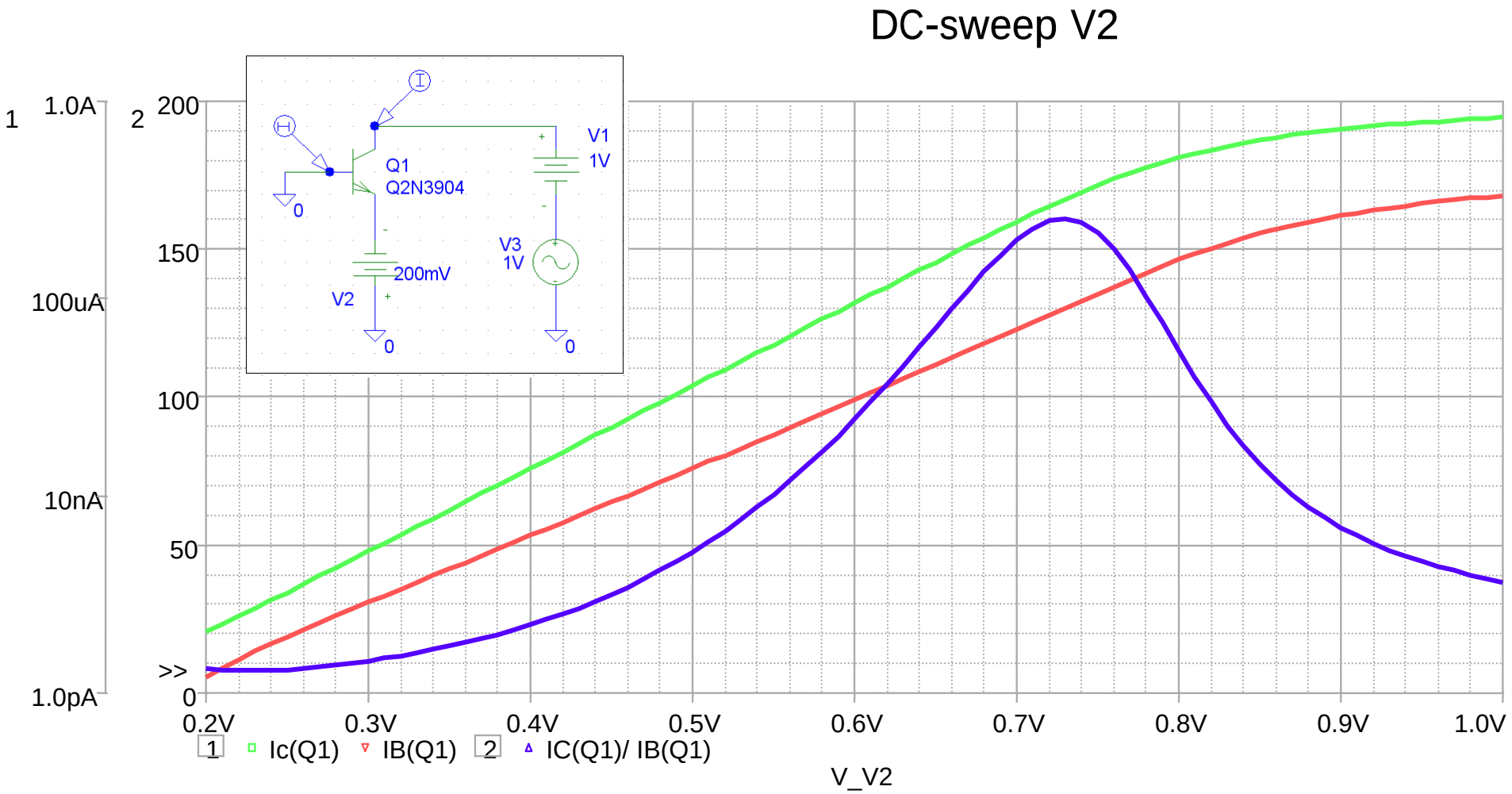
C_μ



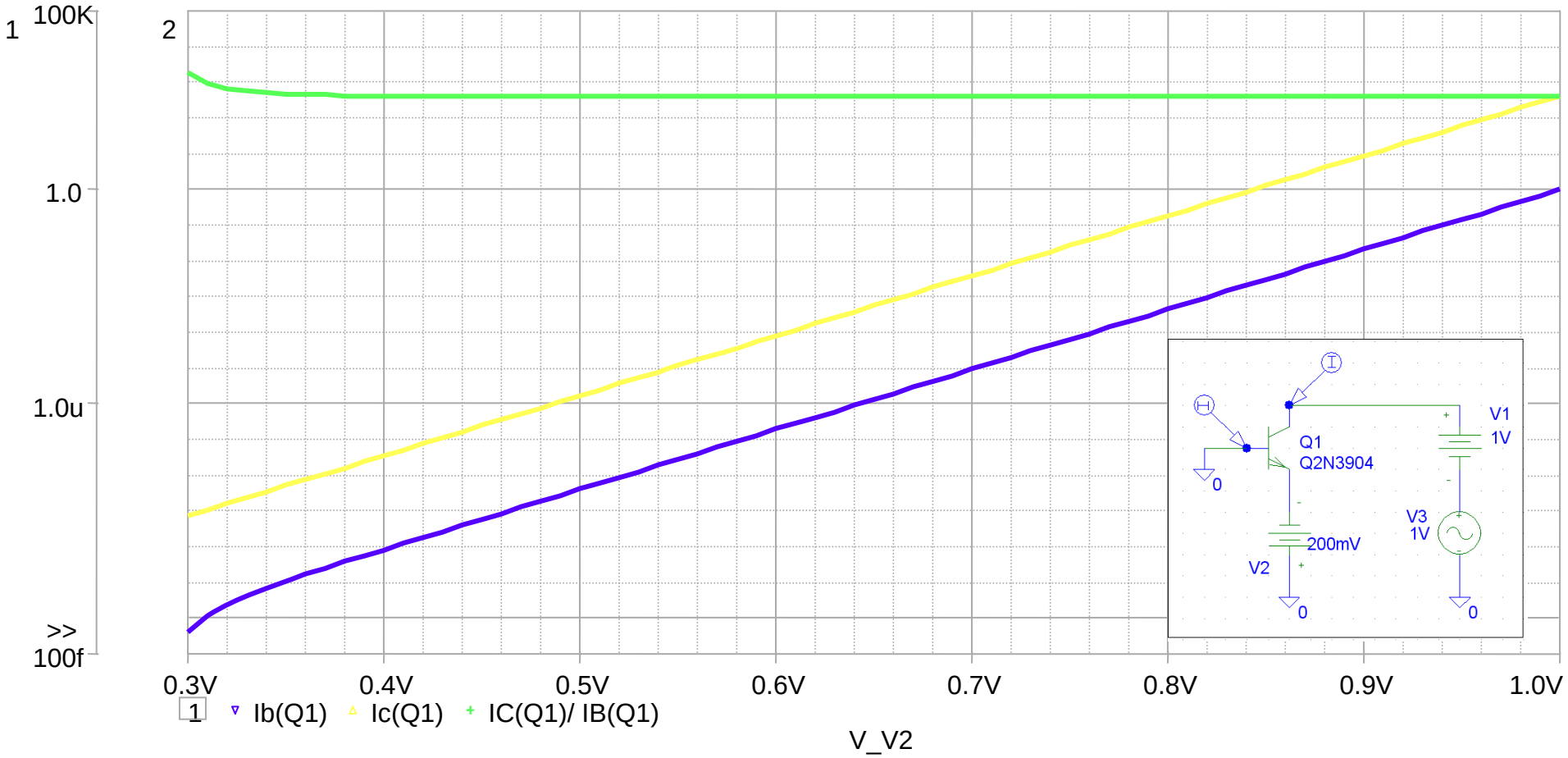
IMG(IC(Q1))/(6.28* Frequency)



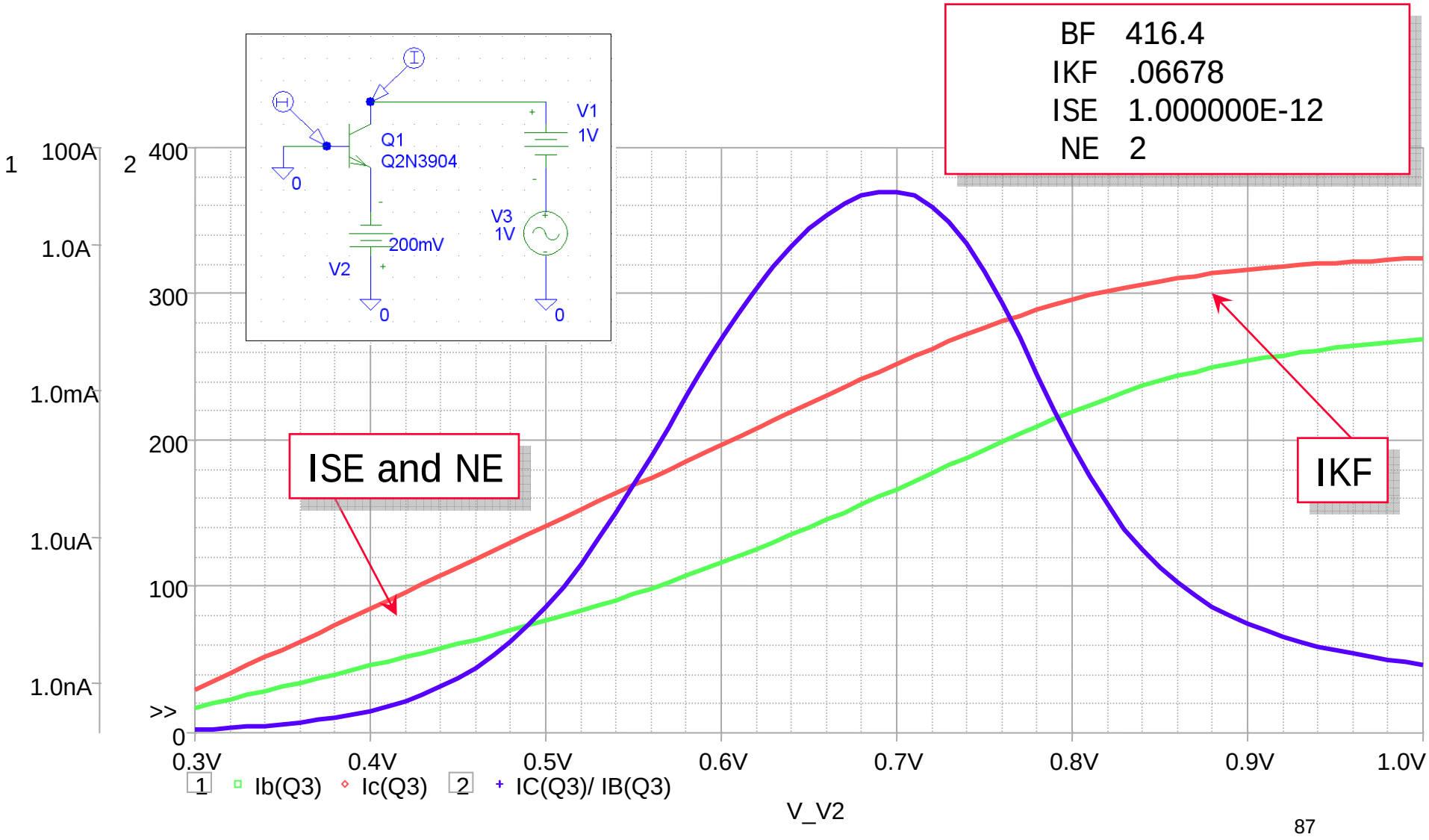
Gummel plot


DC-sweep V2
1
1.0A
100uA
10nA
1.0pA
2
200
150
100
50
>>
0
0.2V
0.3V
0.4V
0.5V
0.6V
0.7V
0.8V
0.9V
1.0V
Q1
Q2N3904
V1
1V
V3
1V
200mV
V2
0
1 Ic(Q1) IB(Q1) 2 IC(Q1)/ IB(Q1)
V_V2

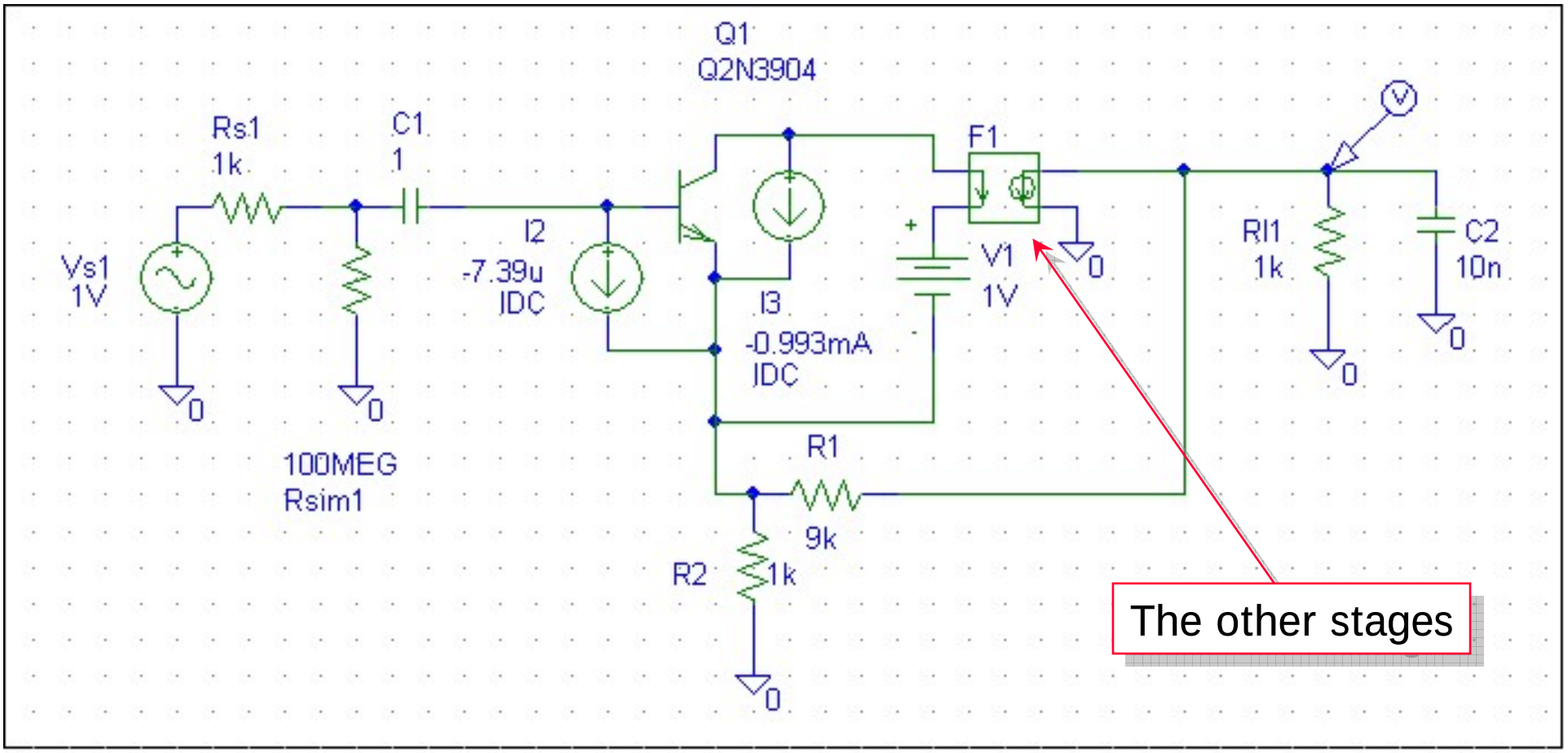
Ideal transistor



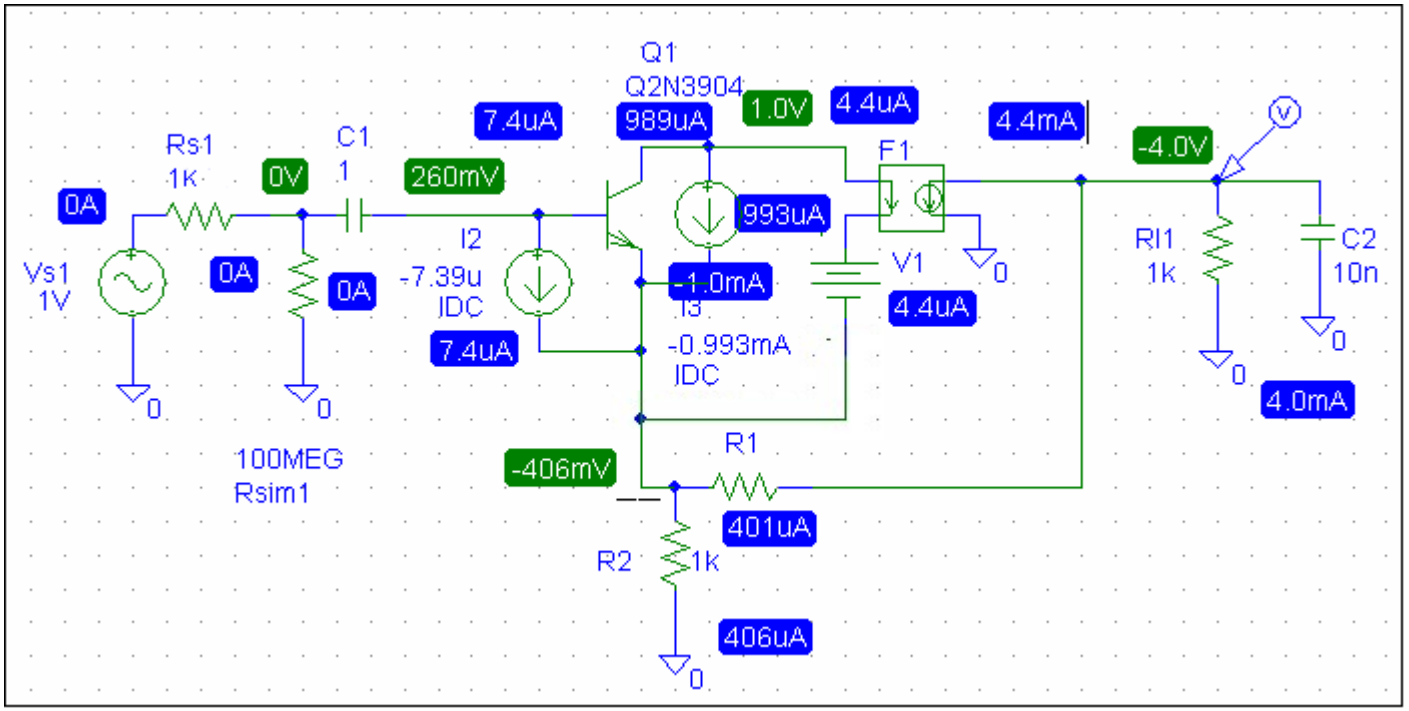
Non-ideal high and low current behavior



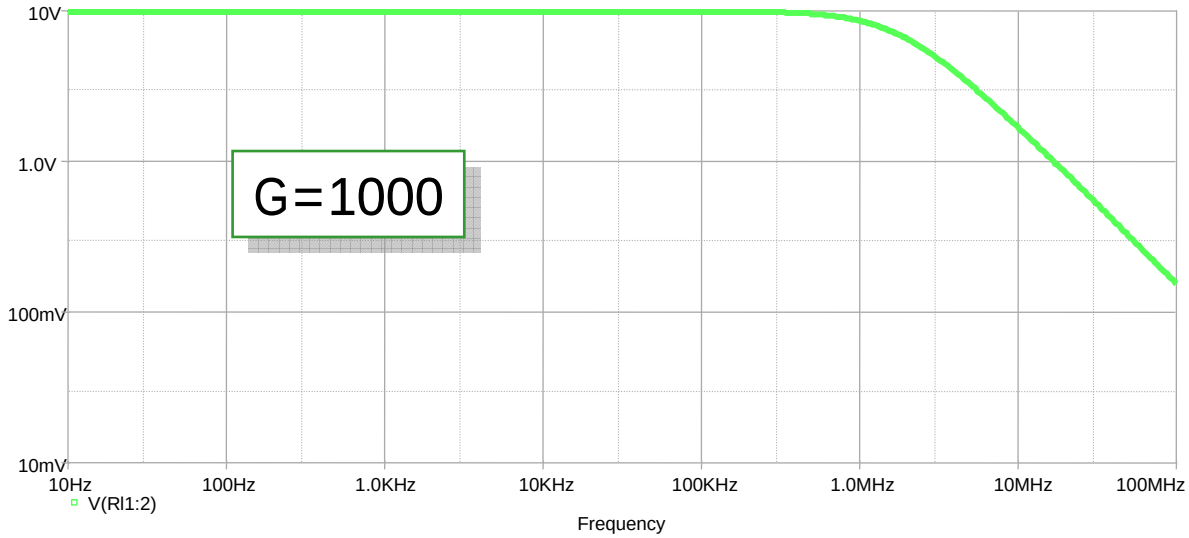
Biasing a transistor

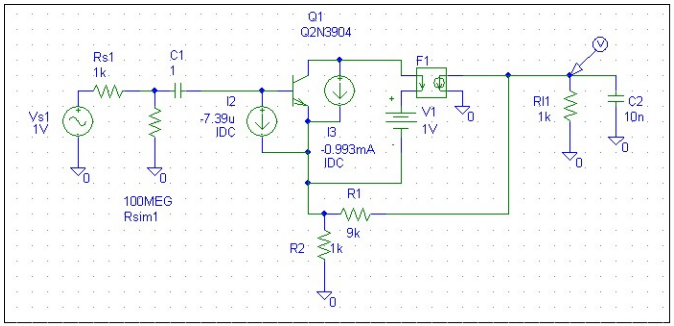


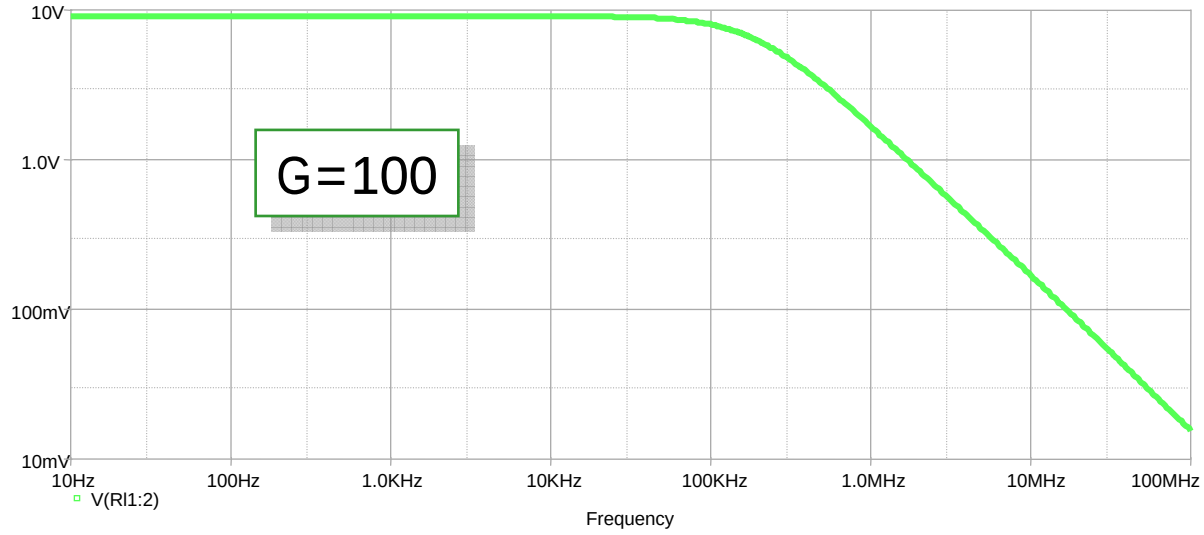
Take current values from Gummel plot



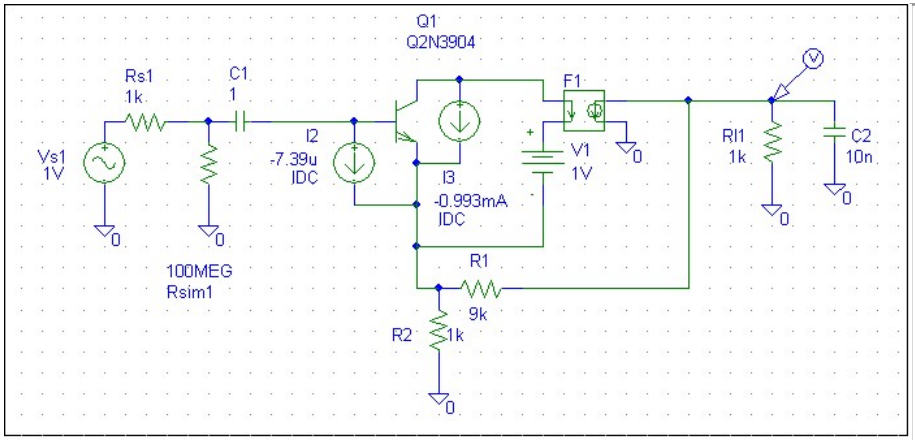
NAME	Q_Q1
MODEL	Q2N3904
IB	7.39E-06
IC	9.89E-04
VBE	6.65E-01
VBC	**-7.40E-01**
VCE	1.41E+00
BETADC	1.34E+02
GM	3.77E-02
RPI	4.07E+03
RX	1.00E+01
RO	7.56E+04
CBE	1.78E-11
CBC	2.94E-12
CJS	0.00E+00
BETAAC	1.53E+02
CBX/CBX2	0.00E+00
FT/FT2	2.89E+08


10V
1.0V
100mV
10mV
G=1000
10Hz
100Hz
1.0KHz
10KHz
100KHz
1.0MHz
10MHz
100MHz
V(Rl1:2)
Frequency


Q1
Q2N3904
Rs1
1k
C1
1
Vs1
1V
I2
-7.39u
IDC
I3
-0.993mA
IDC
F1
V1
1V
Rl1
1k
C2
10n
100MEG
Rsim1
R1
9k
R2
1k
0


10V
1.0V
100mV
10mV
G=100
10Hz
100Hz
1.0KHz
10KHz
100KHz
1.0MHz
10MHz
100MHz
V(Rl1:2)
Frequency

Noise



**** TRANSISTOR SQUARED NOISE VOLTAGES (SQ V/HZ)

Q_Q1

RB	1.360E-17
RC	3.681E-25
RE	0.000E+00
IBSN	7.087E-16
IC	3.975E-17
IBFN	0.000E+00
TOTAL	7.620E-16

**** RESISTOR SQUARED NOISE VOLTAGES (SQ V/HZ)

	R_R1	R_R2	R_Rsim1	R_Rl1	R_Rs1
TOTAL	1.249E-16	1.101E-15	1.360E-20	1.199E-19	1.360E-15

**** TOTAL OUTPUT NOISE VOLTAGE = 3.348E-15 SQ V/HZ

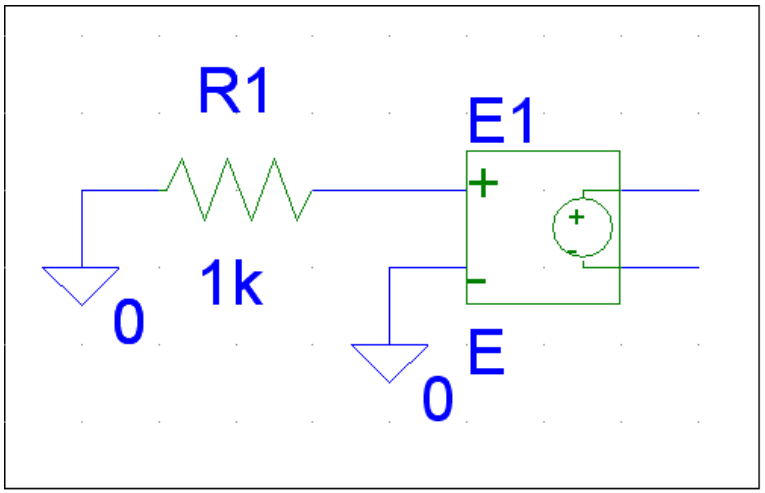
= 5.787E-08 V/RT HZ

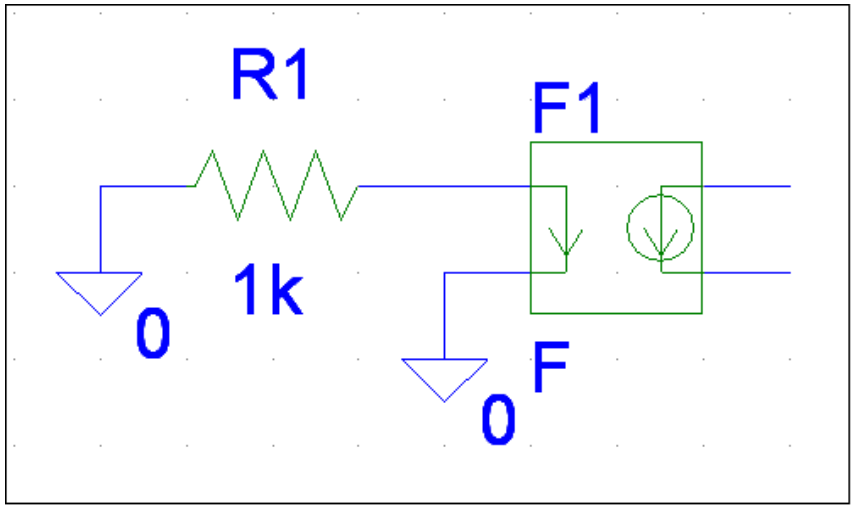
TRANSFER FUNCTION VALUE:

V($N_0003)/V_Vs1 = 9.060E+00

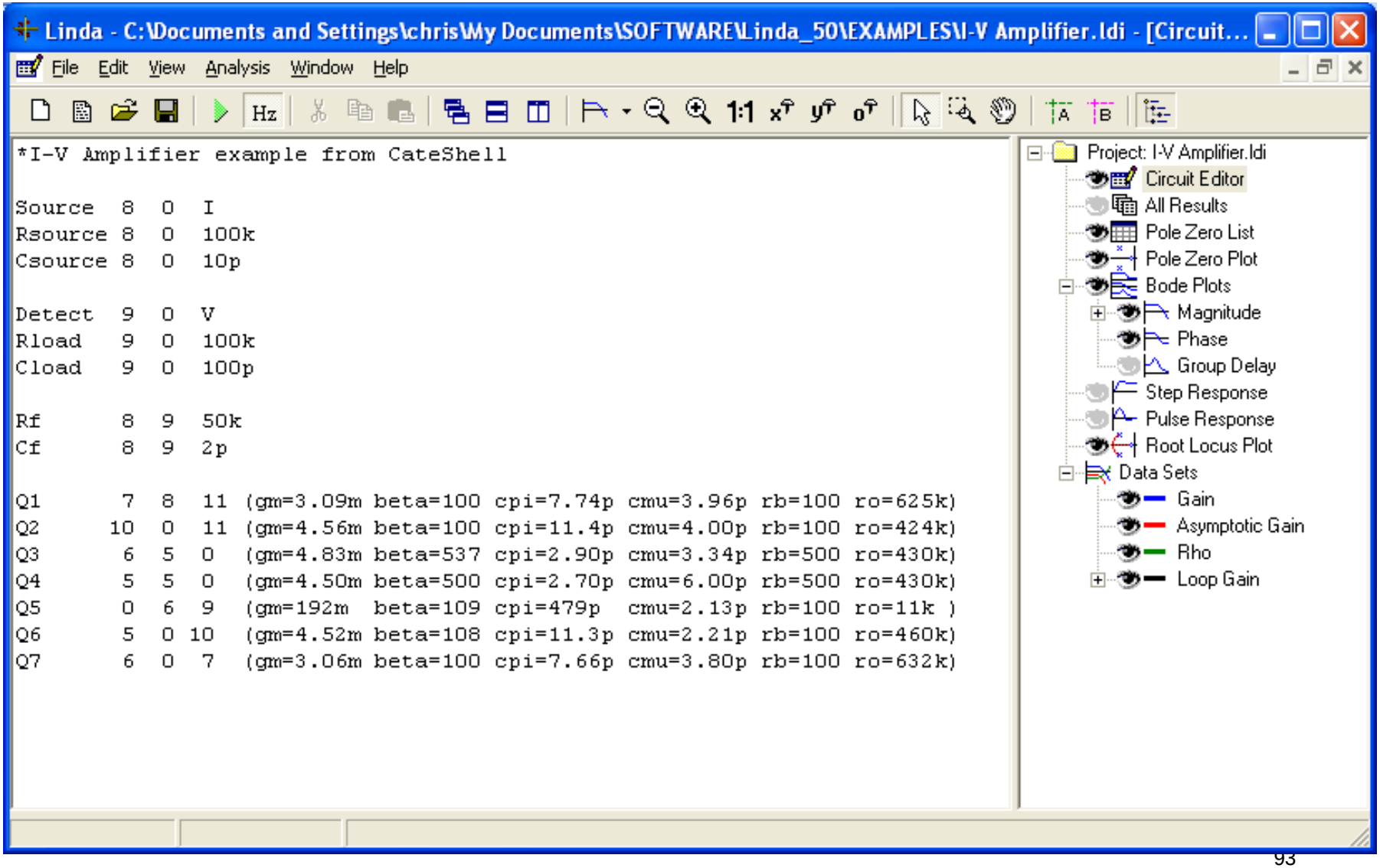
EQUIVALENT INPUT NOISE AT V_Vs1 = 6.387E-09 V/RT HZ

Creating noise sources

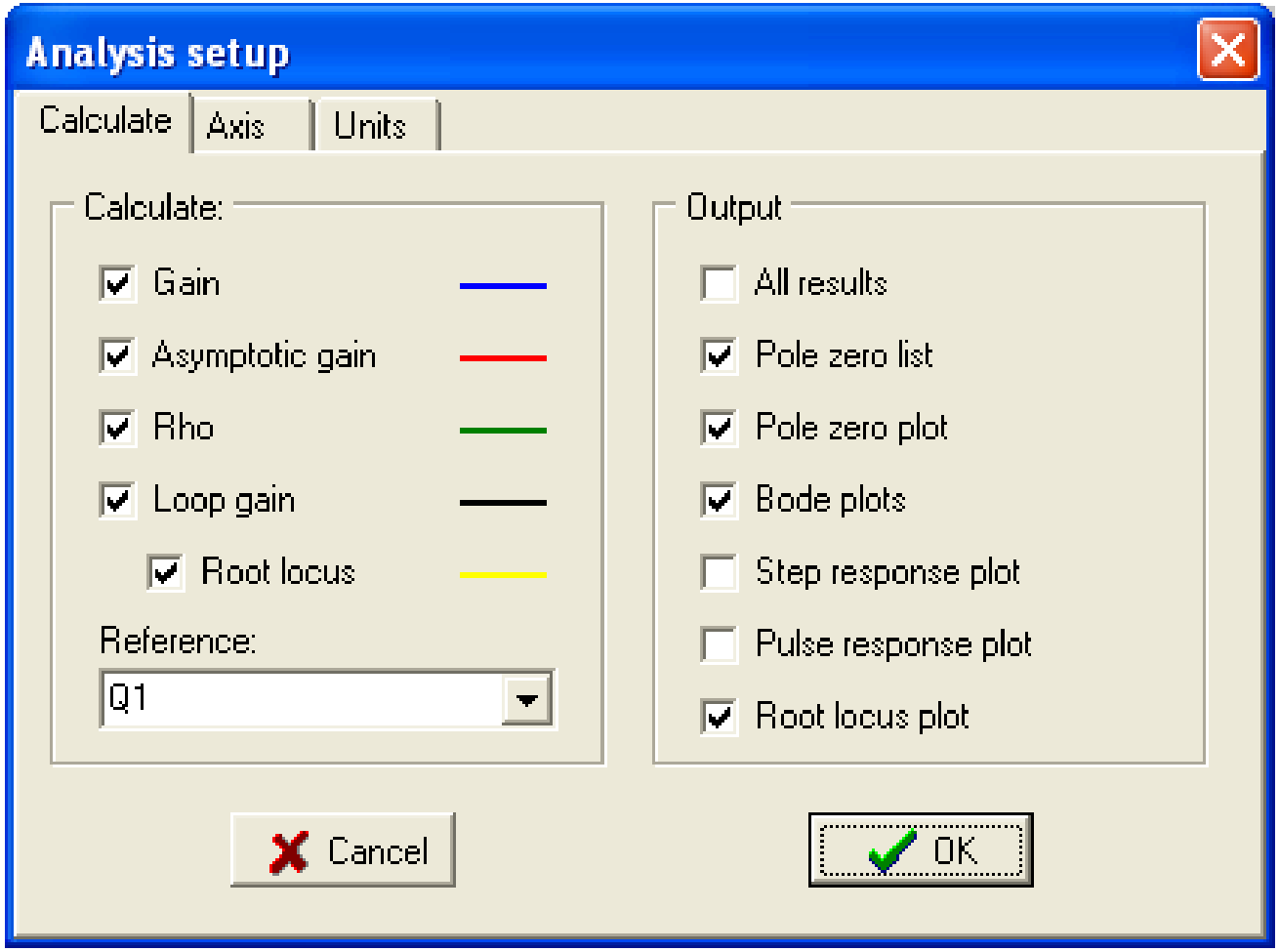




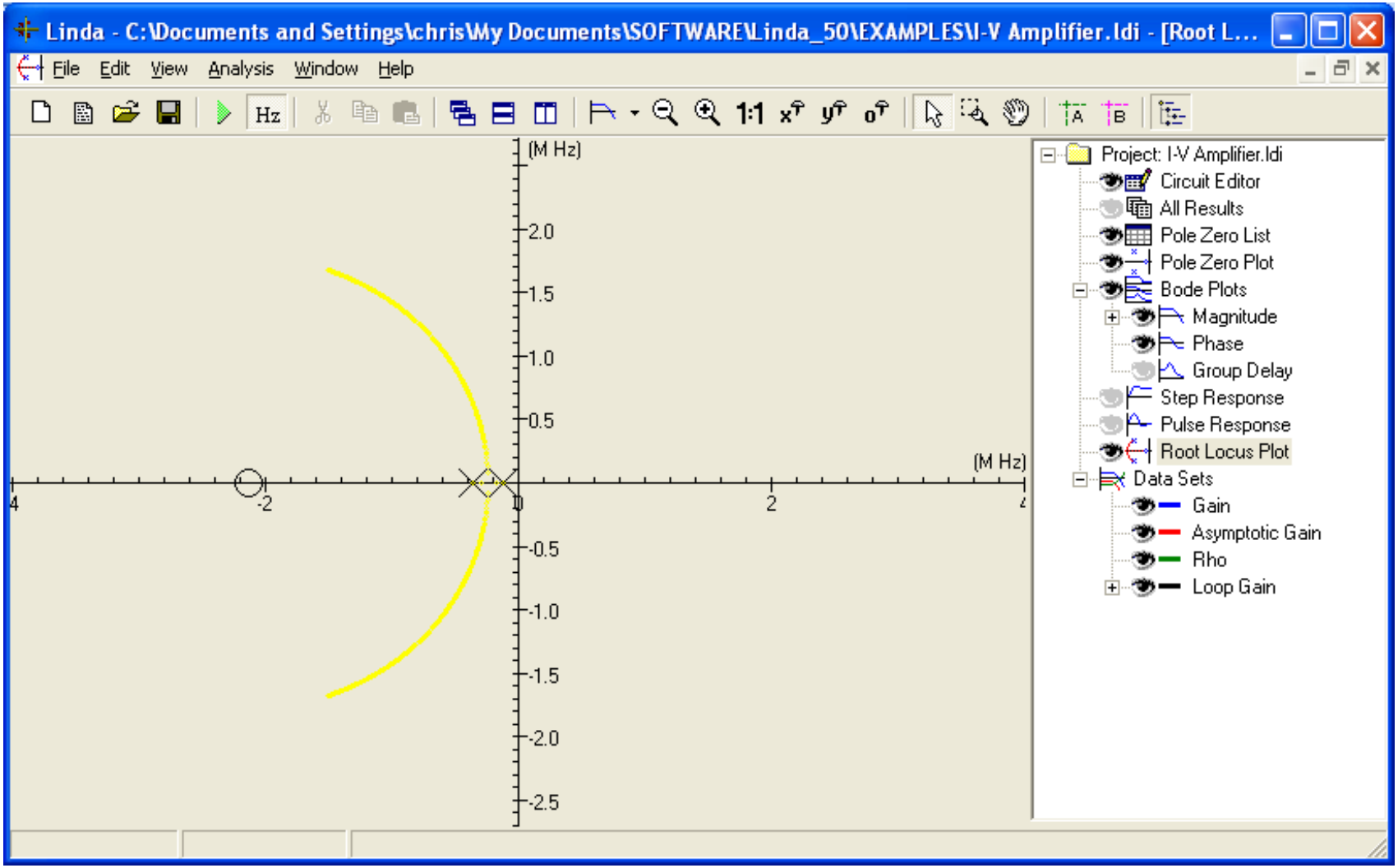
Linda


Linda - C:\Documents and Settings\chris\My Documents\SOFTWARE\Linda_50\EXAMPLES\I-V Amplifier.ldi - [Circuit...
File Edit View Analysis Window Help
Hz
1:1
*I-V Amplifier example from CateShell
Source 8 0 I
Rsource 8 0 100k
Csource 8 0 10p
Detect 9 0 V
Rload 9 0 100k
Cload 9 0 100p
Rf 8 9 50k
Cf 8 9 2p
Q1 7 8 11 (gm=3.09m beta=100 cpi=7.74p cmu=3.96p rb=100 ro=625k)
Q2 10 0 11 (gm=4.56m beta=100 cpi=11.4p cmu=4.00p rb=100 ro=424k)
Q3 6 5 0 (gm=4.83m beta=537 cpi=2.90p cmu=3.34p rb=500 ro=430k)
Q4 5 5 0 (gm=4.50m beta=500 cpi=2.70p cmu=6.00p rb=500 ro=430k)
Q5 0 6 9 (gm=192m beta=109 cpi=479p cmu=2.13p rb=100 ro=11k)
Q6 5 0 10 (gm=4.52m beta=108 cpi=11.3p cmu=2.21p rb=100 ro=460k)
Q7 6 0 7 (gm=3.06m beta=100 cpi=7.66p cmu=3.80p rb=100 ro=632k)
Project: I-V Amplifier.ldi
Circuit Editor
All Results
Pole Zero List
Pole Zero Plot
Bode Plots
Magnitude
Phase
Group Delay
Step Response
Pulse Response
Root Locus Plot
Data Sets
Gain
Asymptotic Gain
Rho
Loop Gain

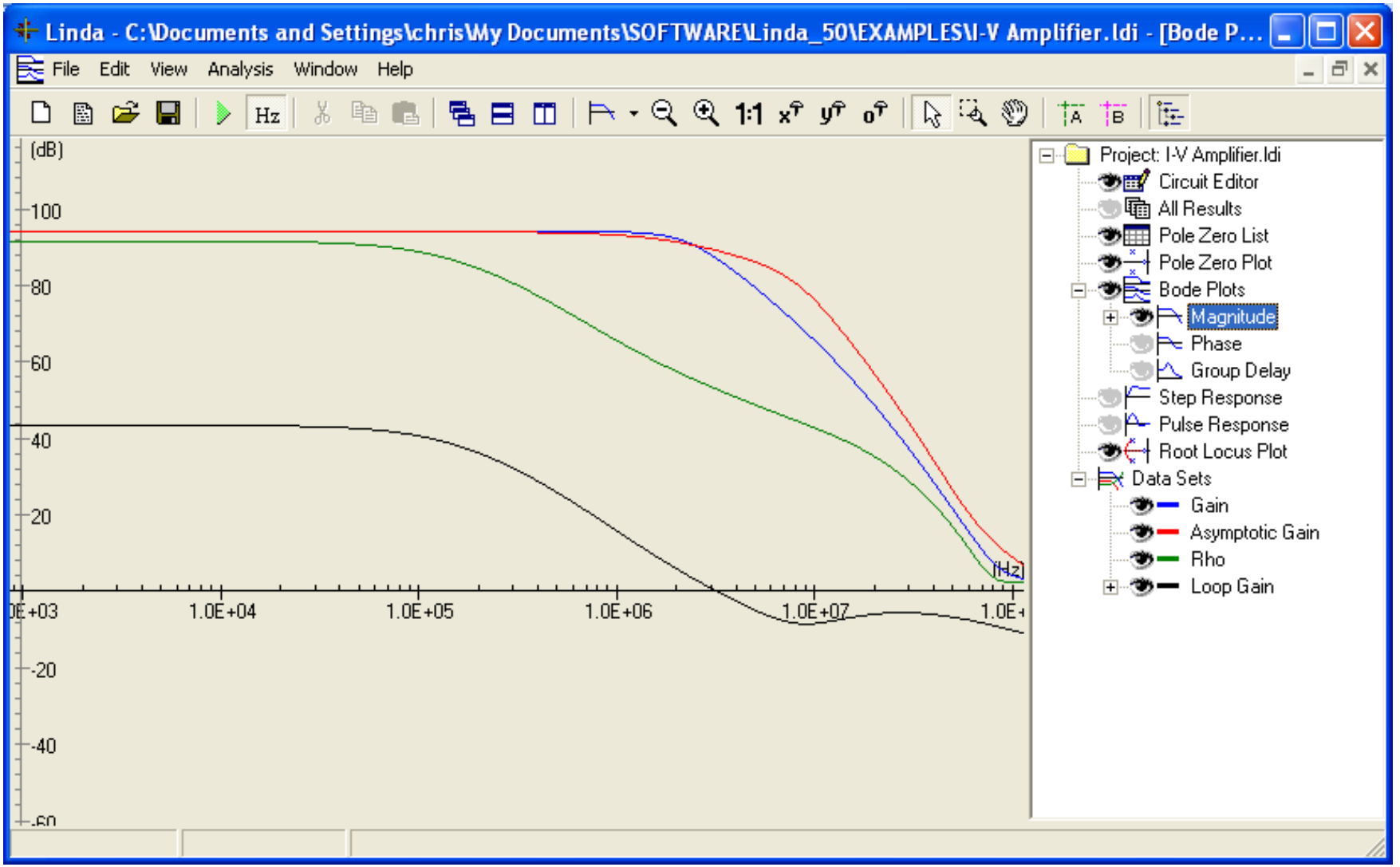
Linda simulation



Linda: root locus



Linda: bode plot (magnitude)



Conclusions

- Idealized circuits can be simulated
  - For verification
  - To find transistor parameters
  - To obtain transistor characteristics
  - To see more complex information (e.g. f-behavior noise)
  - **Never a surprising result**

- Linda
  - To see synthesis parameters (Loopgain, $A_{t\infty}$ etc.)