ET8-16 Structured Electronic Design

2005

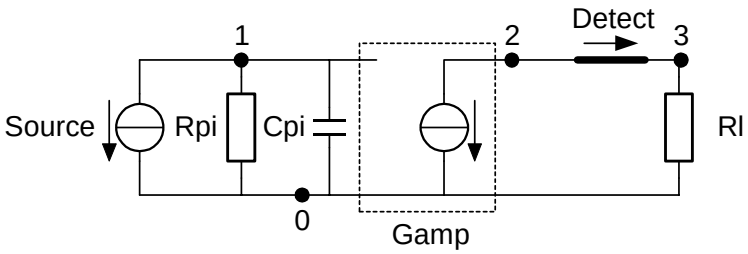
Computer Exercises

(Pspice and Linda)

Transistors

Small-signal model

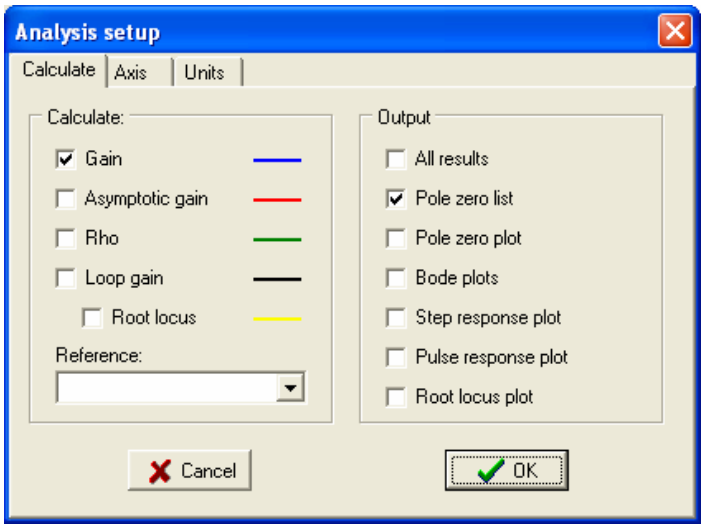
File: {smc}
The file contains a small-signal model of a bipolar transistor which is connected as a CE-stage.




```
* Small signal model

Source   1   0   I

Gamp     2   0   1   0 38m
Rpi      1   0   4k
Cpi      1   0   18p

Rl       3   0   1
Detect   2   3   I
```

The small-signal diagram we have now is the simplest model that can be used to evaluate the frequency behaviour of a transistor. In this exercise the validity of this model is verified.

1. Determine the f_T of this small-signal model with LINDA by calculating the gain and generating the bodeplots.
2. Determine the influence of the load resistance `Rl` on the f_T.
3. Determine the pole of the circuit and again determine the influence of the load resistance. (use both “Pole zero list” and “Pole zero plot”)



Add a resistance that models the output impedance of the transistor. Use a resistance of 30k

4. Repeat questions 1,2 and 3. What is your conclusion with respect to the influence of the output impedance of the transistor?

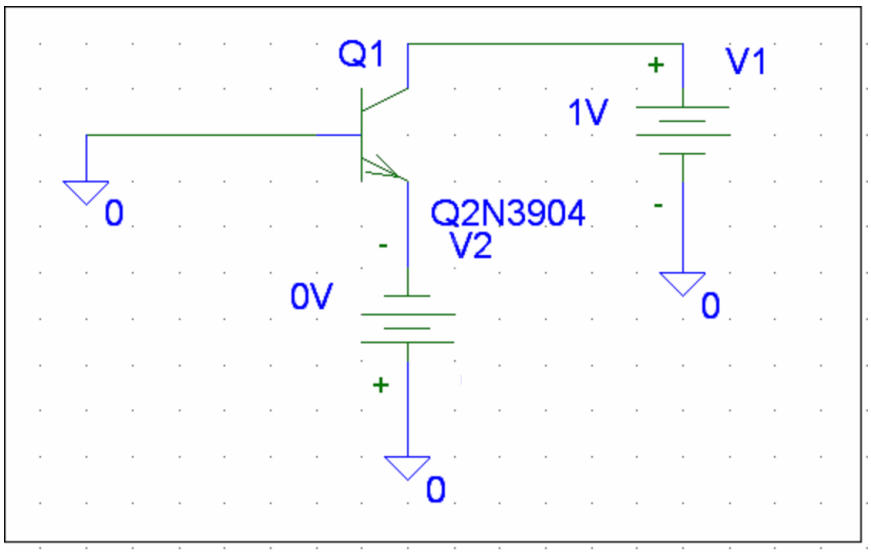
Add a Cmu of 4pF.

5. Short-circuit the transistor at its output (or terminate with 1Ω) and determine the pole/zero pattern.
6. Vary the load resistance and determine its influence on the pole/zero pattern. (An additional pole is created which is, however, non-dominant. Do not spend too much time for explaining it.)

Bipolar transistors

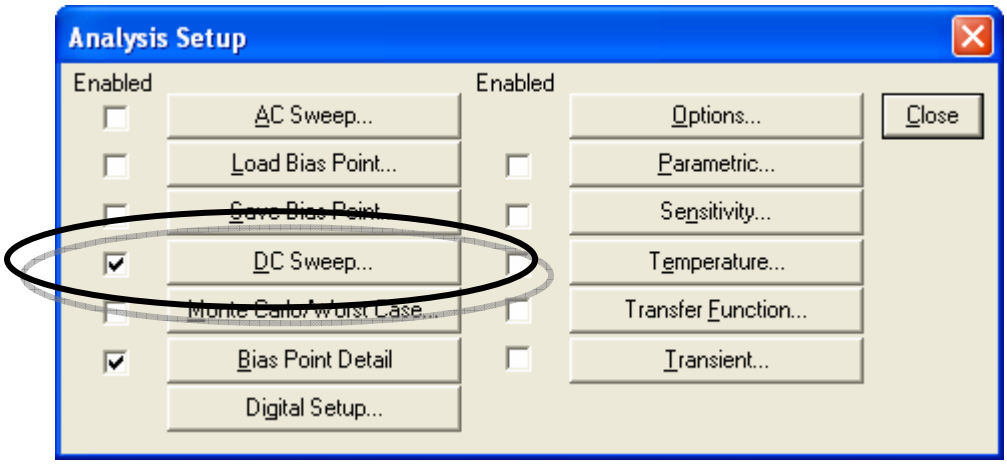
NPN, small signal parameters with Pspice

Start up the Pspice Design Manager and load schematic file: {bipdc}



1. Set-up a DC simulation to plot the collector current and the base current as a function of the base-emitter voltage.

(In Pspice Schematics Menu: Analysis → Setup…)

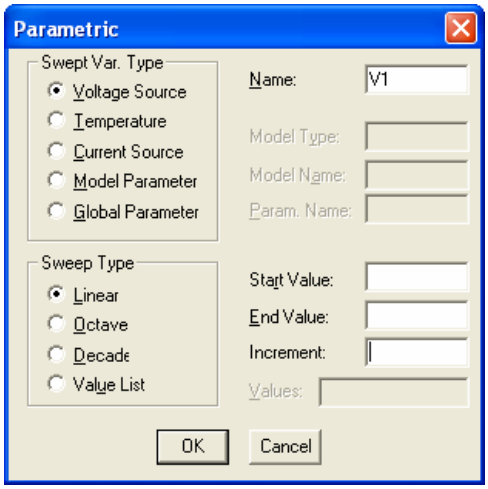


2. Make a plot of the current-gain (β_f) of the transistor as a function of the collector current.

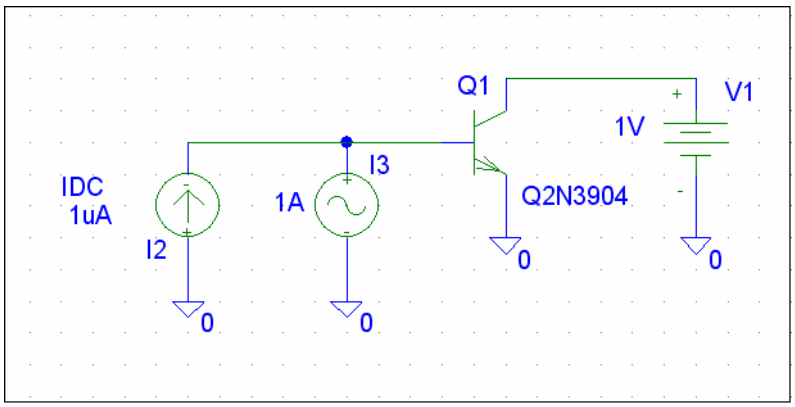
Find the value for Vbe that results in a collector current of about 1mA and set source V2 to that value.

3. Check in the output file the correctness of the collector current. (In Pspice Schematics Menu: Analysis → Examine output)
4. Find the relevant small signal parameters, like f_T .

With the "Parametric" option in the simulator, it is possible to do a simulation for various values of a certain parameter. In this case V1 can be varied to obtain a plot in which the influence of the collector voltage on the current gain can be seen.



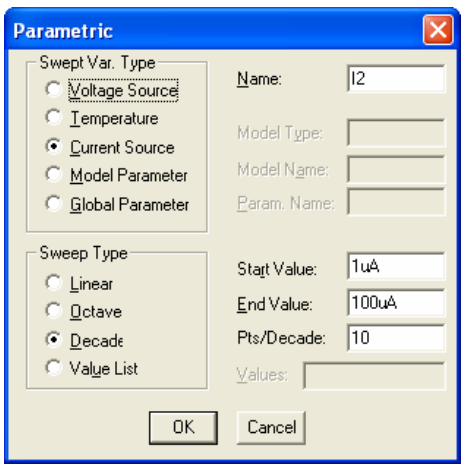
With the help of the AC analysis, the current-gain as a function of the frequency can be determined. This can be done with the circuit below. (File {bipac})



5. Set IDC to the correct value to obtain a collector current of 1mA and setup an AC simulation and determine the f_T of the transistor.
6. How can you see the influence of Cmu and how can you determine that it results in a *right*-half-plane zero?

In this case the simulation can be done for various values of I2 with the "Parametric" option. In this way, the f_T as a function of the collector current can be found.

Generate a set of curves that gives an insight in the current dependency of the f_T .

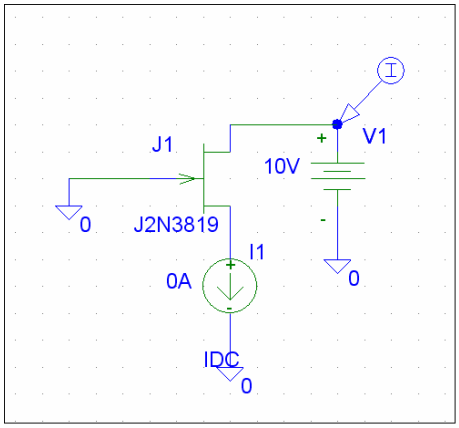


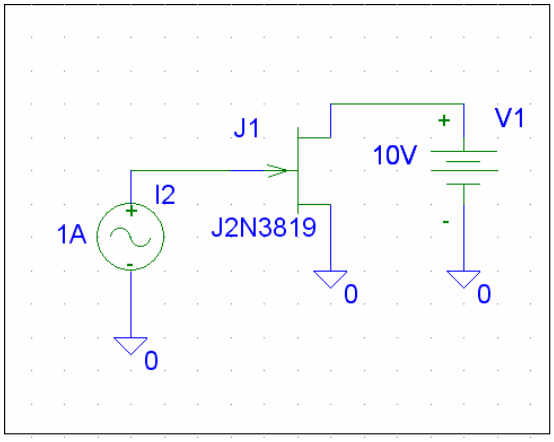
7. Do the same simulations for the PNP-transistor Q2N3906. Important to see are the differences between the Q2N3904 and Q2N3906. New parts can be selected in the Pspice Schematics Menu: Draw → get new part. According to the data sheets they are complementary, i.e. they can be interchanged.

    a. Which differences have to do with the fact that one of the devices is a PNP and the other is a NPN?
    b. Compare the small signal parameters between the Q2N3904 and Q2N3906? Can it be seen from these parameters if the transistor is a PNP or an NPN?

J-FET

Files: {jfetdc} and {jfetac}





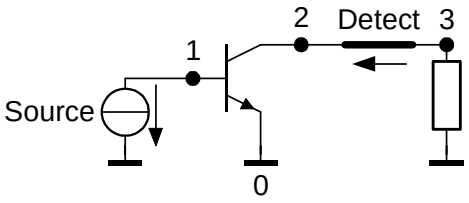
1. Use the circuit on the left to generate the Vgs-Id curve. The type for the J-FET to be used J2N3819.
2. Use the AC analysis in the circuit to the right to make a plot of the current-gain of the J-FET as a function of the frequency.
    a. What is the DC bias voltage V_{GS} in this simulation?
    b. Determine the f_T of the J-FET.

Add in the source lead a DC voltage source with a value of 3V, such that the Gate-source voltage becomes -3 V.

3. Repeat the simulations of the former question. What is the influence of the gate-source voltage on the f_T . (You could use the Parametric option to see more.)

Cascodes

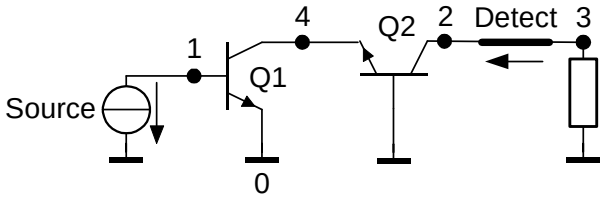
In file {casco1} you can find a circuit composed of the CE-stage and a load resistor of 1Ω.




```
* Bipolar transistor

Source  1   0   I

Q1      2   1   0 (gm=3.09m beta=100 cpi=7.74p cmu=3.96p rb=100 ro=625k)

Rl      3   0   1
Detect  3   2   I
```

1. Do the simulations for a load resistance of 1Ω and 1k. What is the influence of the load resistance?

The influence of the load resistance can be reduced by loading the transistor with a current-follower. The CB stage is an implementation of a current follower. Add a CB-stage.




```
* Bipolar transistor

Source  1   0   I

Q1      4   1   0 (gm=3.09m beta=100 cpi=7.74p cmu=3.96p rb=100 ro=625k)
Q2      2   0   4 (gm=3.09m beta=100 cpi=7.74p cmu=3.96p rb=100 ro=625k)


Rl      3   0   1
Detect  3   2   I
```

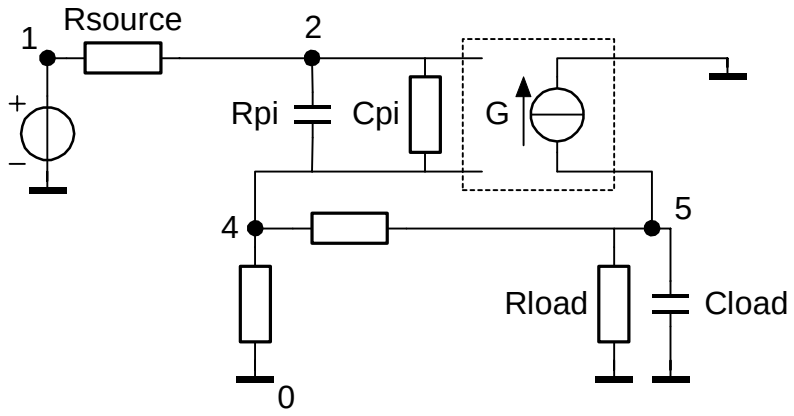
2. Determine again the pole/zero pattern and decide which are the most relevant ones. (For instance, which poles were also found in the previous simulation?) Vary the load resistance (1Ω, 1k and other interesting values). How much is the influence of this resistor on the amplifier behavior and is that a problem when designing a "normal" amplifier?

Negative Feedback

Simple amplifier

In file {trans} you can find a voltage-conductance amplifier which is realized with a simple transistor model (Gamp, Rpi, Cpi)

```
* Voltage amplifier with trans-conductance stage

Source  1   0   V
Rsource 1   2   10k

Gamp    5   0   2   4 -30m
Rpi     2   4   4k
Cpi     2   4   20p

R1      4   0   100
R2      4   5   900

Rload   5   0   100k
Cload   5   0   200p
Detect  5   0   V
```



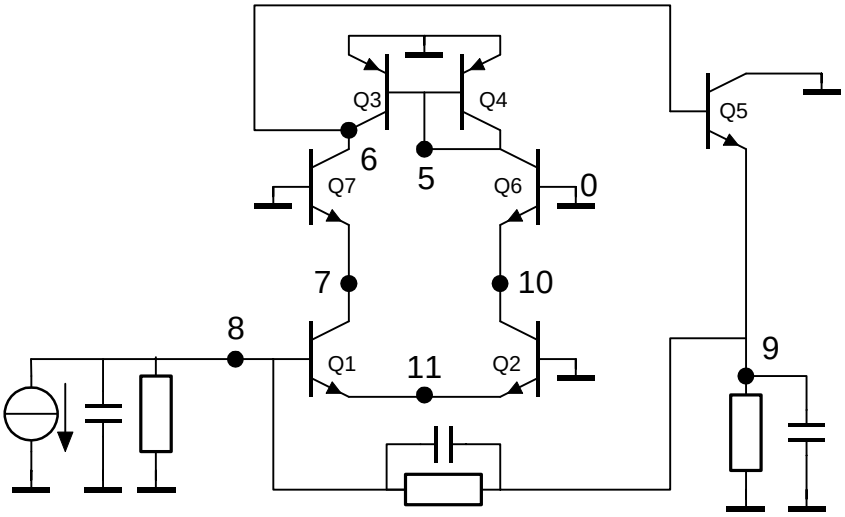
1. For which type of source and load is this configuration optimally suited?
2. Simulate the transfer, pole/zero plots etc. of the amplifier with LINDA for various values of the components.
    a. What is the influence of Rpi and Cload?
    b. What is the influence of the gain of G?
3. Set the gain of G to -1. Do a frequency compensation to get the dominant poles in Butterworth position. Where can a frequency compensation component be inserted?
    a. At the input?
    b. At the output?
    c. In the feedback network?

    Try to find and test as many options as possible en check the effect with LINDA.

IV amplifier

File {IVamp} contains an IV amplifier implemented with a number of transistors. The circuit schematic is shown below. Use this file to investigate the properties of this circuit with LINDA.

1. Why is the $A_{t\infty}$ frequency dependent?
2. Where is the frequency compensation?
3. Can this be done in another way?
4. What happens when there is variation in the choice of reference transistor?
5. Shouldn't the base of Q7 not be connected to node 11 instead of to the ground node? What is the difference?
6. What is your opinion on the output stage (Q5)?




```
*I-V Amplifier

Source  8   0   I
Rsource 8   0   100k
Csource 8   0   10p

Detect  9   0   V
Rload   9   0   100k
Cload   9   0   100p

Rf      8   9   50k
Cf      8   9   2p

Q1      7   8   11  (gm=3.09m beta=100 cpi=7.74p cmu=3.96p rb=100 ro=625k)
Q2     10   0   11  (gm=4.56m beta=100 cpi=11.4p cmu=4.00p rb=100 ro=424k)
Q3      6   5   0   (gm=4.83m beta=537 cpi=2.90p cmu=3.34p rb=500 ro=430k)
Q4      5   5   0   (gm=4.50m beta=500 cpi=2.70p cmu=6.00p rb=500 ro=430k)
Q5      0   6   9   (gm=192m  beta=109 cpi=479p  cmu=2.13p rb=100 ro=11k )
Q6      5   0  10   (gm=4.52m beta=108 cpi=11.3p cmu=2.21p rb=100 ro=460k)
Q7      6   0   7   (gm=3.06m beta=100 cpi=7.66p cmu=3.80p rb=100 ro=632k)
```

File {IVamp} is also available for Pspice. The circuit topology is comparable with the Linda circuit, the small-signal parameters may differ.

7. Check the DC operating point. (You can use the buttons V and I to show the bias voltages in the schematic)
8. Plot the frequency response and determine the influence of capacitor Cf.
9. Check the noise behavior. This is done by checking the option “noise” in the setup of the AC analysis.
10. Which components are most dominant in the noise behavior?
11. Check the influence of bias currents on the noise behavior