Electronic Instrumentation

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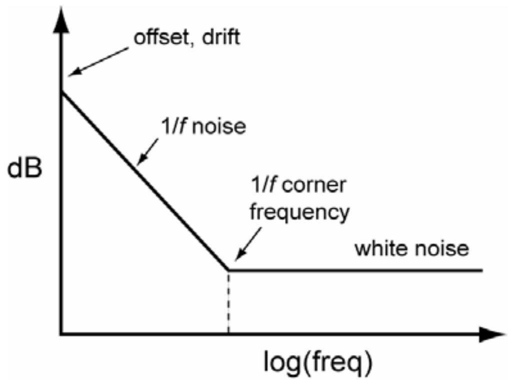
Introduction

- Synonyms: coherent detection, synchronous demodulation, lock-in amplification, chopping??
- These are all modulation techniques that areused to improve the low frequency performance of measurement systems
- When square-wave modulation is employed, the technique is referred to as chopping
- Chopping leads to improved low-frequency specs e.g. reduced offset and 1/*f* noise, better CMRR and PSRR

Amplifier behavior near DC

Characterized by
- Offset, gain error
- Drift,1/*f* noise
- PSRR, CMRR

What can we do?



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What to do?

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- Offset, gain error and 1/*f* noise are caused by component mismatch and non-idealities
  ⇒ they are a part of life!
- But we can reduce their effects by
  - Static techniques like calibration and trimming
  - Dynamic techniques such as chopping, auto-zeroing and dynamic element matching

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Trimming

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- Involves measuring a static error of a system (e.g. offset or gain error) and then adjusting the value of a component in order to reduce the error to zero.

+ Low complexity
+ No bandwidth limitation
– Requires measurement equipment

- Also requires a memory element to store the trimmed value e.g. a potentiometer, or a PROM

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Dynamic Offset Cancellation Techniques

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- Techniques that continuously attempt to cancel the effect of system non-idealities to zero.

+ (Usually) do not require measurement equipment
+ Also compensate for drift and 1/*f* noise and improve CMRR and PSRR
– Requires more complex circuitry
– Reduced bandwidth

- Two main Dynamic Offset Cancellation (DOC) techniques are: **Chopping** and **Auto-zeroing**

Auto-zeroing and chopping

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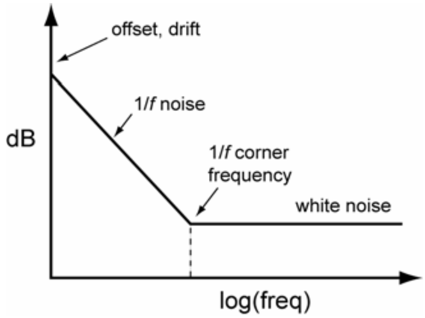

- Time domain ⇒ Auto-zeroing ⇒ periodically measure the offset (noise) and subtract it from the input signal
- Frequency domain ⇒ Chopping ⇒ modulating the input signal above the 1/*f* noise

Chopper amplifiers

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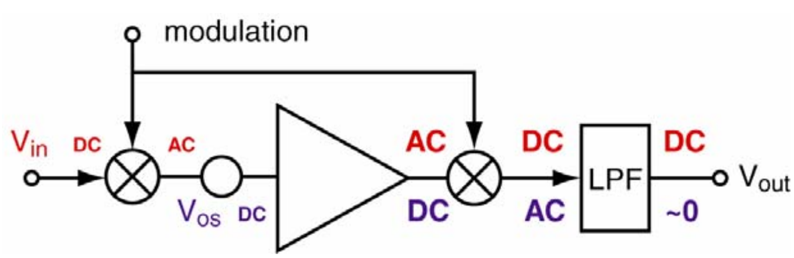

- Signal is modulated, amplified and then demodulated
- DC offset is modulated **once** and the resulting AC signal can be removed by a low-pass filter
- The modulators are usually implemented as polarity reversing switches, known as choppers
- The technique is known as “chopping”

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Square-wave modulation

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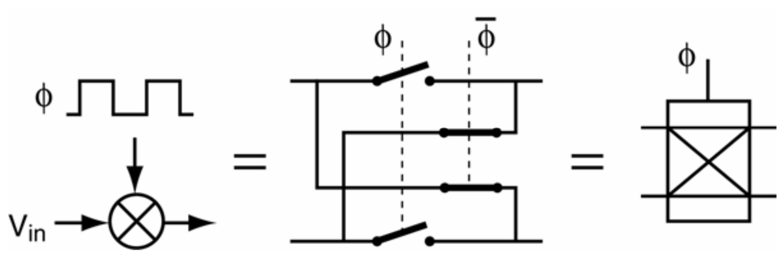

- Easily generated modulating signal
- Modulator is a simple polarity-reversing switch
- Switches are easily realized in CMOS

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Chopping in the time domain

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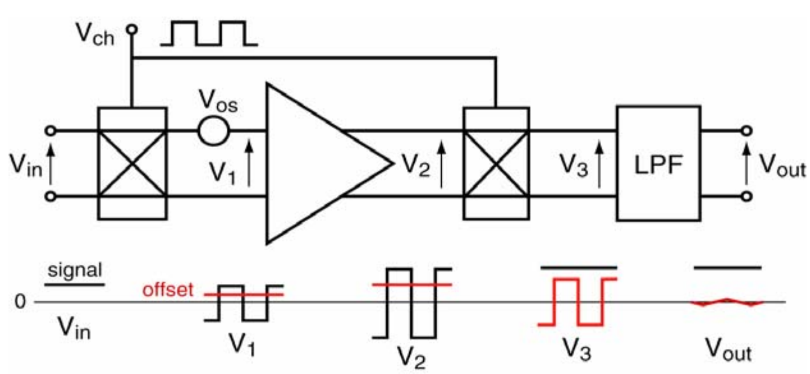

- Output chopper converts offset into a square-wave!
- To avoid residual offset, the duty-cycle of the square-wave should be exactly 50%
- Non-ideal LPF $\Rightarrow$ residual ripple

Chopping in the frequency domain

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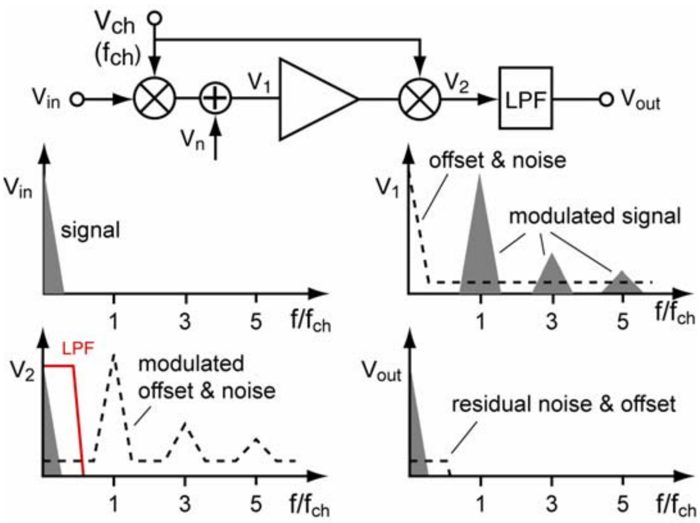

Residual noise of chopping

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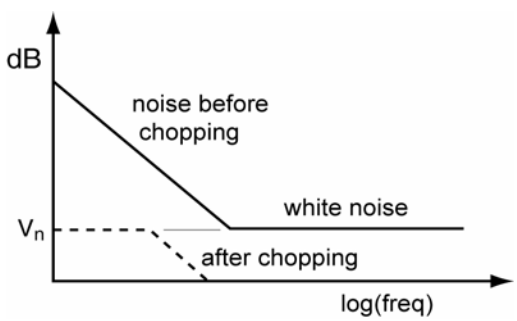

- **Complete** suppresion of 1/*f* noise if f_{ch} > 1/*f* corner freq. but harmonics => slightly (π^2/8) more noise power
- But up-modulated offset must be filtered out $\Rightarrow$ loss of signal BW and residual chopper “ripple”

C.C. Enz and G.C. Temes, “Circuit Techniques for Reducing the Effects of Op-Amp Imperfections: Autozeroing. Correlated Double Sampling, and Chopper Stabilization,” Proceedings of the IEEE, 1996

Charge injection & clock feed-through

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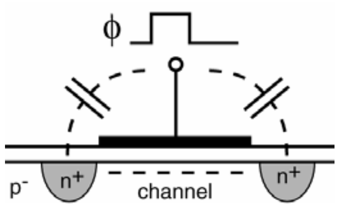

- Charge injection occurs when MOSFETs switch OFF
- Channel charge, $Q_{ch} = WLC_{ox}(V_{GS}-V_t)$
- Clock feed-through is caused by capacitive coupling via the overlap capacitance between gate and the source/drain diffusions

Residual Offset of chopping

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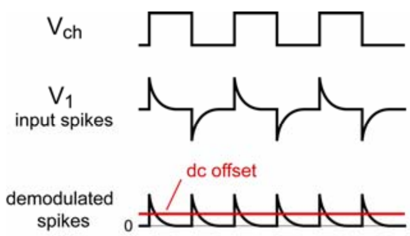

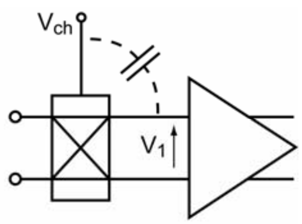

Main causes

- Clock asymmetry (non-50% duty-cycle)
- Clock feed-through and charge injection cause spikes at the amplifier’s input
- These spikes are then demodulated back to DC by the output chopper ⇒ residual offset (microvolts)
- Residual offset is proportional to chopping frequency

Bandwidth & gain accuracy

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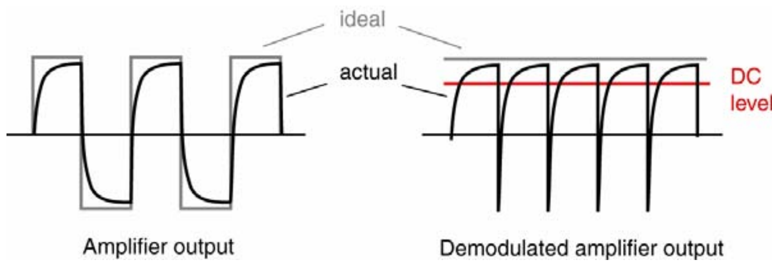

- Limited amplifier BW means that the output signal will not be a perfect square-wave $\Rightarrow$ less gain
- In other words chopping reduces DC gain!

Chopping: Summary

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- Chopping is a powerful technique that can be used to reduce offset and 1/f noise in amplifiers and systems
- Main drawback is the need for a LPF to remove the up-modulated offset $\Rightarrow$ bandwidth limitation
- Main non-idealities are caused by finite BW, clock asymmetry and chopper spikes
- Offsets as low as a few nV can be achieved!

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How far can we go?

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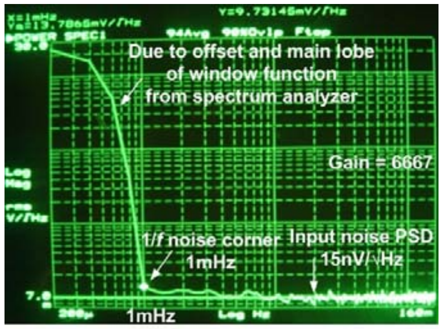

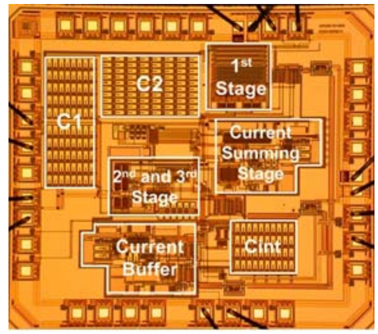

- Three-stage amplifier, first two stages are chopped
- Achieved a 1mHz 1/*f* corner frequency, 5uV offset voltage, CMRR and PSRR > 120dB

R. Wu, K.A.A. Makinwa and J.H. Huijsing, "A Chopper Current-Feedback Instrumentation Amplifier with a 1mHz 1/f Noise Corner and an AC-Coupled Ripple Reduction Loop," *J. Solid-State Circuits,* vol. 44, is. 12, pp. 3232 – 3243, Dec. 2009.

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Thermistor read-out IC

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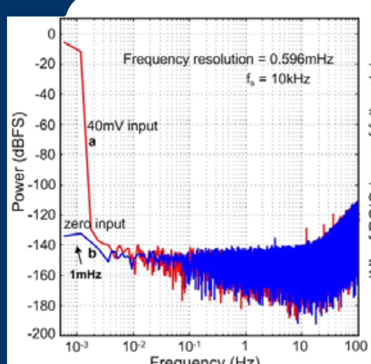

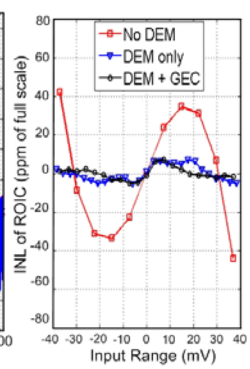

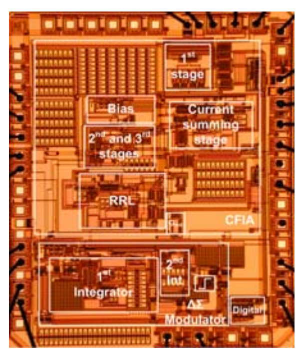

- Precision IA and a 21-bit ΣΔ ADC (10Hz BW)
- 200nV offset, 0.04% gain error, 10ppm linearity

R. Wu, K.A.A. Makinwa and J.H. Huijsing, ""A 21b ±40mV Range Read-Out IC for Bridge Transducers," J. Solid-State Circuits, vol. 47, is. 9, pp. 2152 – 2163, Sept 2012..

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Assignment 5

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- A thermistor is read out by incorporating it into a ¼ Wheatstone bridge with three other temperature-stable resistors whose value is equal to the thermistor's nominal value at room temperature
- The bridge and the amplifier are driven from a temperature-stable 5V supply
- The thermistor has a nominal value of 65kΩ at 25°C, and a temperature coefficient S = 0.04%/C
- The bridge is read out by an differential amplifier whose thermal noise is at the same level as that of the bridge. The amplifier also suffers from 1/f noise, with a corner frequency of 5kHz.
- The amplifier is followed by a 1^{st} order low-pass filter with a 100Hz cut-off frequency

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Assignment 5

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a) To deal with its 1/*f* noise and offset, the amplifier is chopped. If the noise at the output of the system is to be minimized, what is the lowest possible chopping frequency?

b) Assuming that the amplifier has an initial offset of 5mV, estimate the amplitude (input-referred) of the chopper ripple present at the output of the system.

c) Calculate the detection limit (in degrees Celsius) due to the thermal noise of the bridge and the amplifier.

d) If the differential amplifier has a finite CMRR and PSRR and the power supply can vary by ±10%, what CMRR and PSRR are required to ensure that the corresponding detection limit is less than 1mK?

Dynamic Offset Cancellation (DOC) Techniques

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- Techniques that continuously attempt to cancel the effect of system non-idealities to zero.

\+ (Usually) do not require measurement equipment

\+ Also compensate for drift and 1/*f* noise and improve CMRR and PSRR

– Requires more complex circuitry

– Reduced bandwidth

- Two main Dynamic Offset Cancellation (DOC) techniques are: **Chopping** and **Auto-zeroing**

Chopping and Auto-zeroing

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Two basic methods

1. Modulate the offset away from DC and then remove it with a low-pass filter it out ⇒ Chopping
2. Store the offset in a memory element and then subtract it from the input signal ⇒ Auto-zeroing

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Auto-zeroing

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- Basic idea is to remove the signal, measure and store the offset and subsequently subtract the stored offset from the input signal
- This means that the amplifier is not continuously available => bandwidth limitation
- A memory element is needed to store the offset

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Auto-zero Principle (1)

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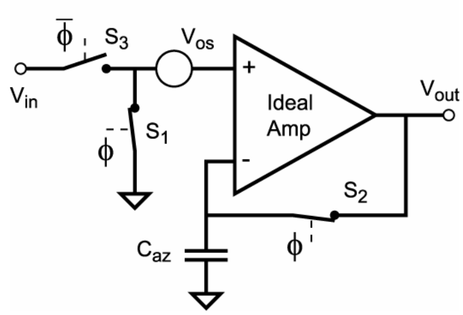

- $S_{1,2}$ closed $\Rightarrow V_{out} = V_{os}$
- So the amplifier's offset is stored on C_{az}

Auto-zero Principle (2)

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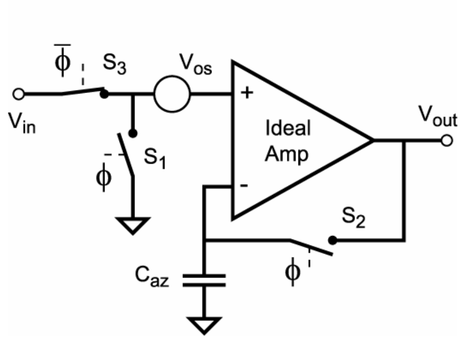

- S_3 closed ⇒ output signal is available
- For an amplifier with *finite* DC gain *A*, the residual offset is given by $V_{os}/(A+1)$

Residual Offset of Auto-zeroing

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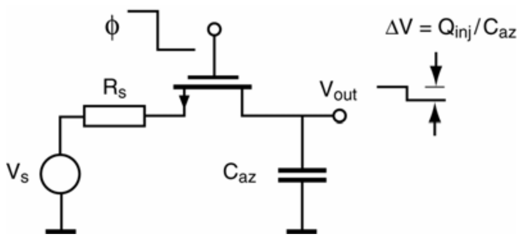

- Clock feed-through and charge injection ⇒ errors in stored offset
- Stored offset on C_{az} will slowly leak away
- In practice C_{az} is made as large as possible

Mitigating Charge Injection

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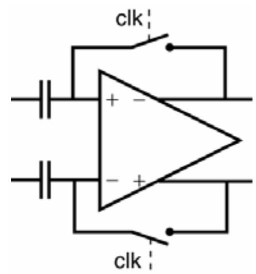
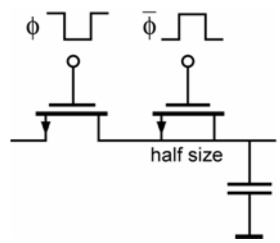
- Use minimum size switches (subject to noise & speed requirements)
- Use differential topologies $\Rightarrow$ 1st order cancellation



- For single-ended topologies dummy switches help [5,6]
- **But** main switch area will be ~2x minimum size $\Rightarrow$ more CI $\Rightarrow$ limited benefit



Sampling the offset: kT/C noise

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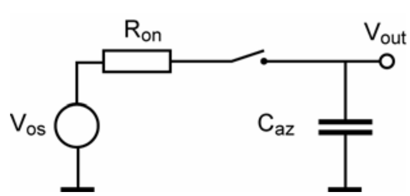

- Thermal noise of R_{on} is filtered by C_{az} (kT/C noise)
- Instantaneous value of the noise is “frozen” every time the switch opens $\Rightarrow$ noise is exacerbated
- Accurate sampling of V_{os} $\Rightarrow$ large C

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Residual Noise of Auto-Zeroing (1)

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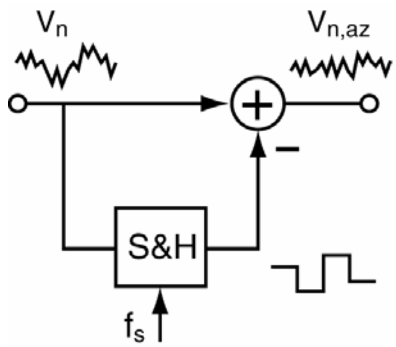
- $V_{n,az}(f) = V_n(f)*(1 - H(f))$
- H(f) is the frequency
- response of the S&H
- H(f) = sinc(f)

⇒ 1-H(f) is a HPF

⇒ Offset and 1/*f* noise reduction!



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Residual Noise of Auto-Zeroing (2)

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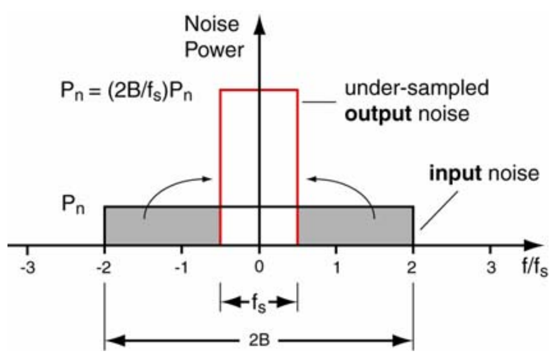

- Since B > f_s (settling!) ⇒ white noise is aliased
- Folded white noise is LP filtered by S&H i.e. by H(f)
- Baseband (1/*f*) noise is HP filtered i.e. by 1-H(f)

Residual Noise of Auto-Zeroing (3)

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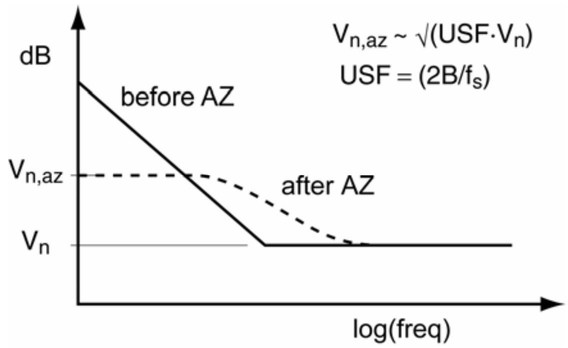

- 1/*f* noise is removed **but** noise foldover occurs
- For a 1st order LPF, noise bandwidth = $\pi f_c/2$

Auto-zeroing: Summary

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- Auto-zeroing is a powerful offset and 1/f noise reduction technique for amplifiers and systems
- Unlike chopping it does not suffer from ripple, but its noise performance is worse due to aliasing
- Main non-idealities are caused by switching spikes, leakage currents and (sometimes) by finite gain
- Offsets of a few microvolts can be reached

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Correlated Double Sampling (CDS)

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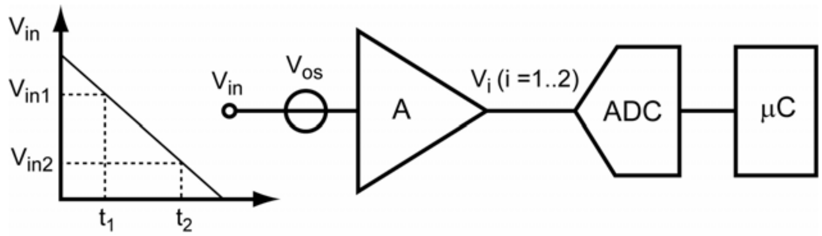

- Sometimes only a signal **difference** is of interest
  - Phase 1: $V_1 = A(V_{in1} + V_{os})$
  - Phase 2: $V_2 = A(V_{in2} + V_{os})$

  $\Rightarrow (V_1 - V_2) = A(V_{in1} - V_{in2})$

- To maximize suppression of 1/*f* noise, the interval $t_1 - t_2$, should be as short as possible

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Gain Error

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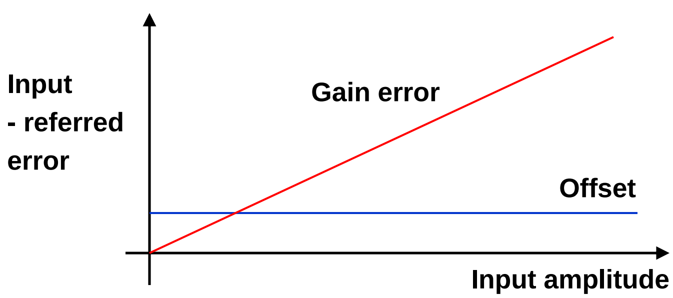

- For small signals, offset dominates, while for large signals, gain error dominates
- Gain error, like offset, is a static error, which can be removed by calibration and/or trimming
- It can also be removed by dynamic element matching

The Utility of Feedback

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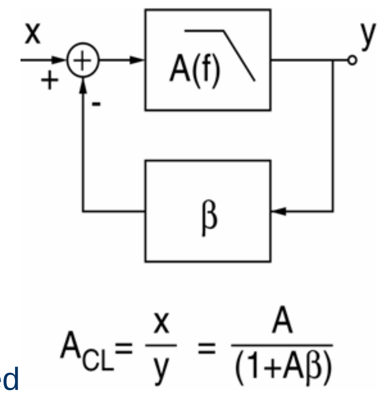
If $A(f) \cdot \beta >> 1 \Rightarrow A_{CL} \cong 1/\beta$.

For moderate $1/\beta$, op-amp **DC** gain is large enough!

$\beta \Rightarrow$ Resistor/Capacitor ratios.
Resistors $\Rightarrow$ 0.01%, 5 ppm/°C
Capacitors $\Rightarrow$ 1%, 500 ppm/°C

$\Rightarrow A_{CL}$ can be accurately defined

But can we do better?



The 3 Signal Method

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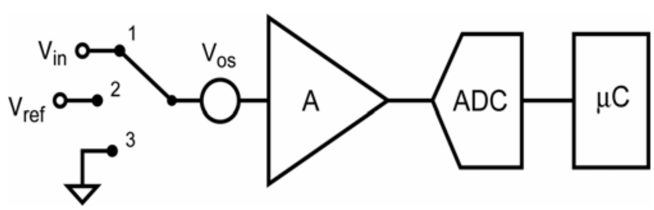

- Measurement requires 3 phases
  - Phase 1: $V_1=A(V_{os}+V_{in})$
  - Phase 2: $V_2=A(V_{os}+V_{ref})$
  - Phase 3: $V_3=AV_{os}$

$\Rightarrow$ A, V_{os} and V_{in} can be found

- Accuracy is limited by ADC resolution and noise

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Dynamic Element Matching

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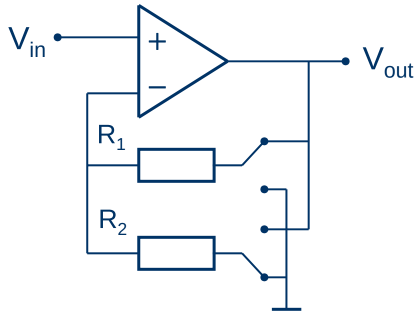

- Gain error can be further reduced by using Dynamic Element Matching (DEM)
- DEM involves swapping the **position** of nominally identical elements in a circuit
- This significantly reduces the <u>average</u> error

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Dynamic Element Matching

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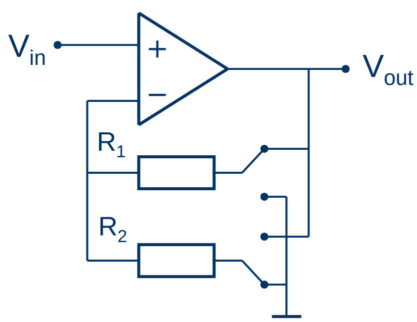

- Gain of 2 $\Rightarrow$ 2 <u>identical</u> resistors i.e. $R_1=R_2$
- DEM can be applied by using switches to swap the position of mismatched resistors in the circuit
- Accuracy is limited by mismatch of switch resistance

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Accurate x2 Amplifier with DEM (2)

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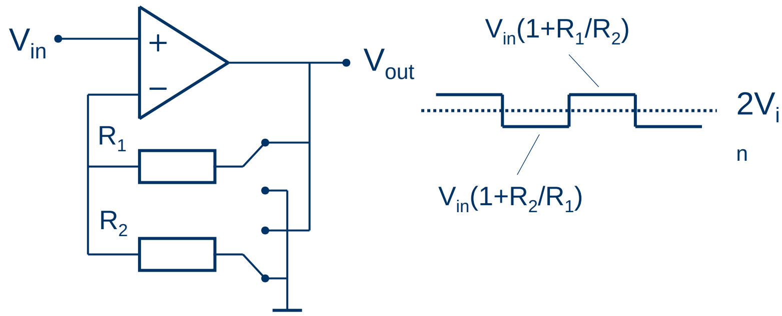

- Average value of $V_{out} \sim 2V_{in}$
- V_{out} contains AC components which must be removed by a LPF (like chopping)
- So chopping and DEM can be easily combined

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DEM in the Frequency Domain

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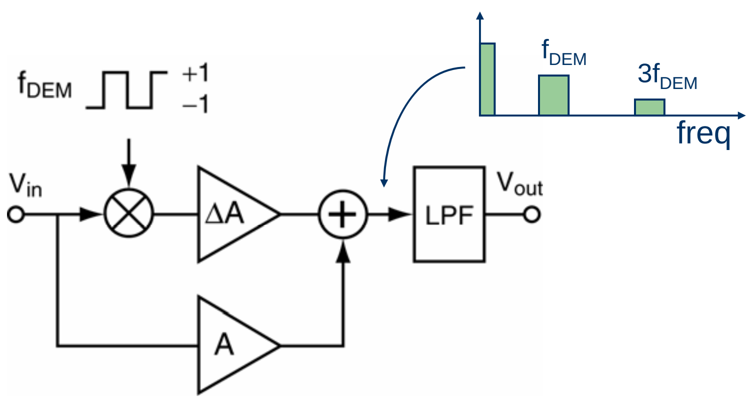

- Mismatch is shifted to harmonics of f_{DEM}
- To avoid unwanted intermodulation, $f_{in} < f_{DEM}/2$

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Differential Amplifier With DEM

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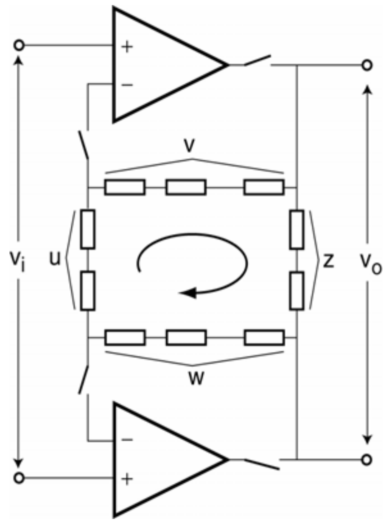
- Feedback via a chain of matched resistors.
- Chain is rotated by a **bank** of switches and the gain, A is averaged.
- $A = 1 + (v+w)/u$
- NB: Switch resistance has no effect, why?



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DEM: Pros and Cons

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PRO

- Gain (ratio) error can be reduced to ppm levels

CONS

- Switches are required to swap components
  ⇒ extra circuit complexity, switching transients
- Result must be averaged ⇒ BW reduction
- Input signal must be band-limited ($f_{in} < f_{DEM}/2$) to prevent inter-modulation products

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Summary

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- Precise gain can be achieved by feedback
  - discrete resistors ⇒ 0.01%
  - on-chip ⇒ 0.1% due to mismatch

- Better performance can be achieved by using DEM, but like chopping, this is at the expense of BW

- If the signal is digitized, the 3-signal method is also effective, but accuracy is limited by ADC resolution

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Assignment 6

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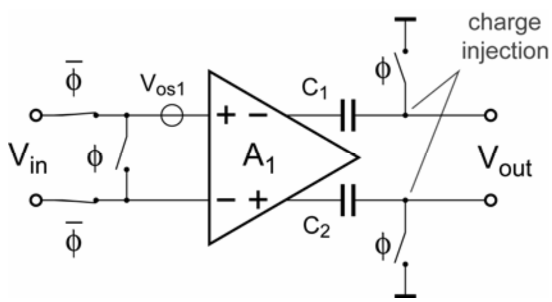

a) The amplifier shown above has 10mV offset and a gain of 1000. Each switch is associated with 100pC of charge injection. Assuming that their mismatch is less than 10%, how big must the capacitors be to achieve 20µV offset after auto-zeroing.

Assignment 6

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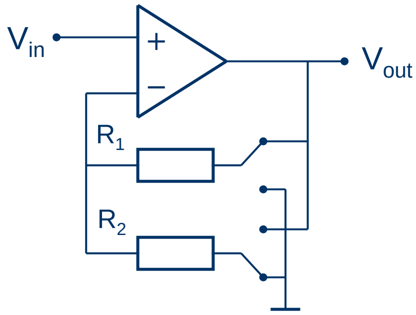

b) If the $R_1 \sim R_2$ and their mismatch is 1%,calculate the residual gain error after DEM

c) What is the residual gain error if the DEM control signal is asymmetric: with a 49% duty-cycle

d) What is the effect of finite switch resistance?

Assignment 6

ET8.017
El. Instr.

e) A measurement system employs the 3-signal method. If it makes use of a 5V reference, how many bits of resolution must its ADC have in order to achieve a residual offset of less than 20µV.