ad ET4054

The example from the book

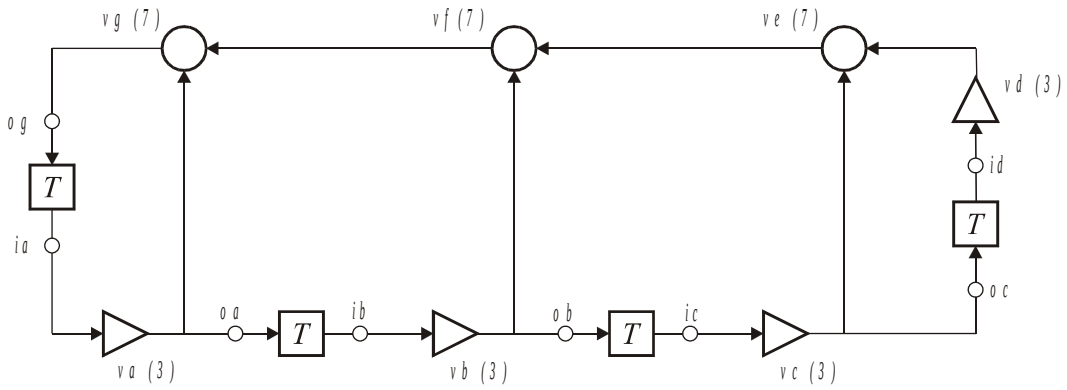
SYNTHESIS AND OPTIMIZATION OF DIGITAL CIRCUITS
Giovanni De Micheli

starting from
FIGURE 9.8 Example of synchronous network.

using the Scheduling Toolbox: retime_minCycles

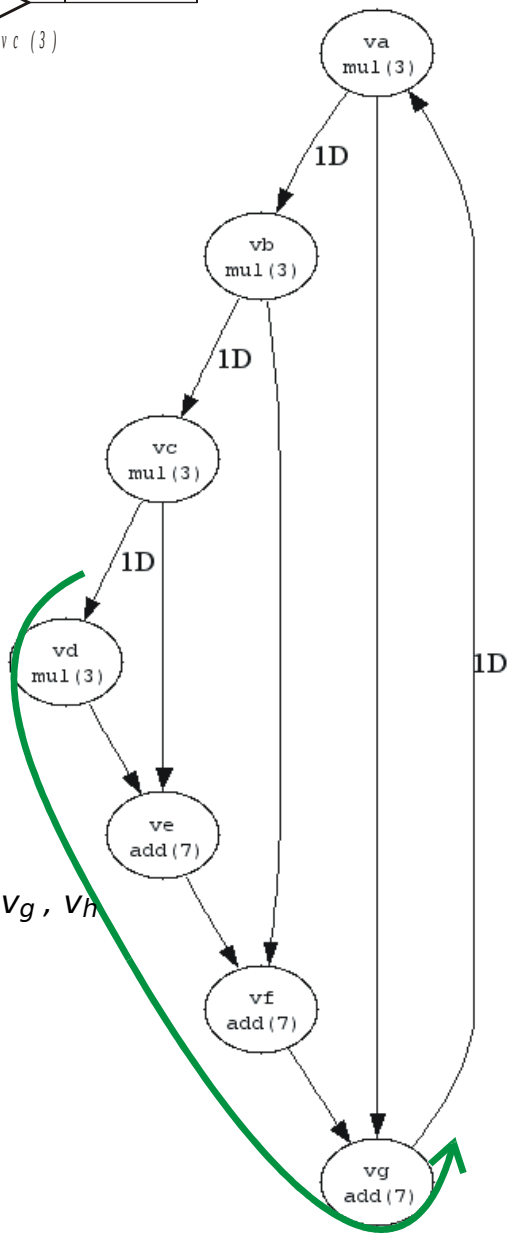
to obtain
FIGURE 9.10 Retimed network.

The original file **'DeMicheli_Fig98.cir'**:




```
iocDef = 'iokk';

va = ka * ia;
vb = kb * ib;
vc = kc * ic;
vd = kd * id;
ve = vc + vd;
vf = vb + ve;
vg = va + vf;

oa = va;
ib = Toa;
ob = vb;
ic = Tob;
oc = vc;
id = Toc;
og = vg;
ia = Tog;
oh = ia;
```

not needed, has been removed



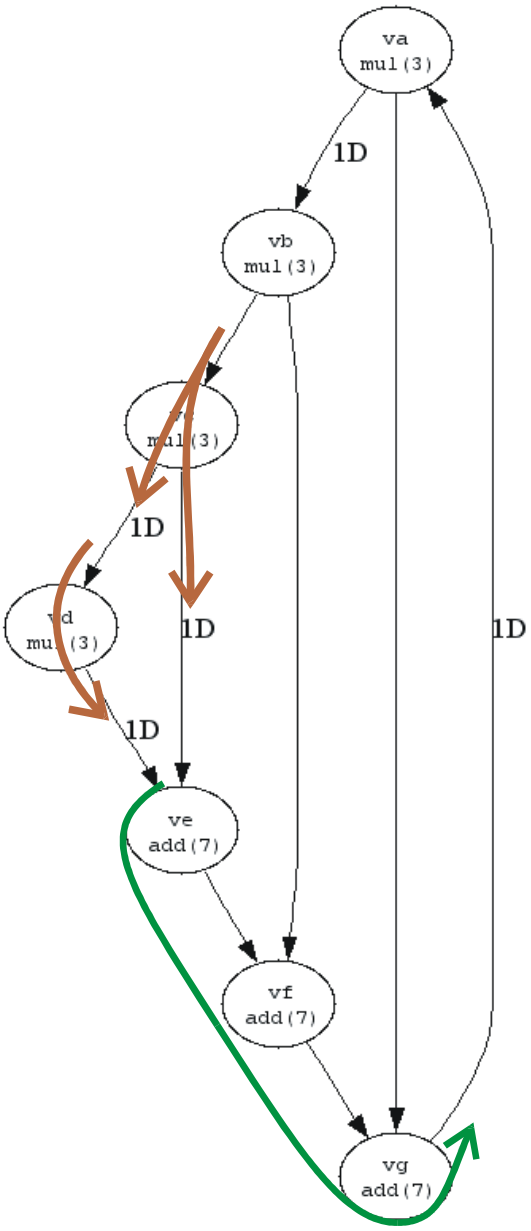
De Micheli (**Example 9.3.8**):

"The topological critical path is (v_d , v_e , v_f , v_g , v_h), whose delay is 24 units."

Note: $v_h = 0$ and has been removed

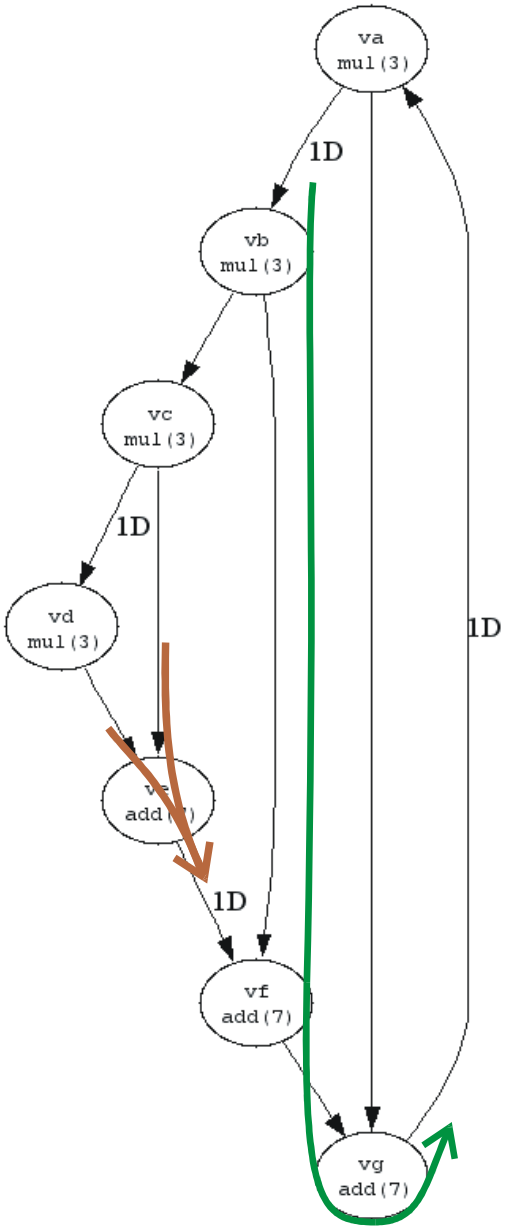
```
>> retime_minCycles('DeMicheli_Fig98.cir',3,7);
Originally, the longest path needs 24 states
```

```
Retiming possible to decrease longest path to 21 state(s)
Actions needed:
       Change 1T delay from vb to vc into a straight connection.
       Change connection from vc to ve into a 1T delay.
       Change connection from vd to ve into a 1T delay.

Created file 'DeMicheli_Fig98_21cyc.cir' for this retimed circuit ...
```



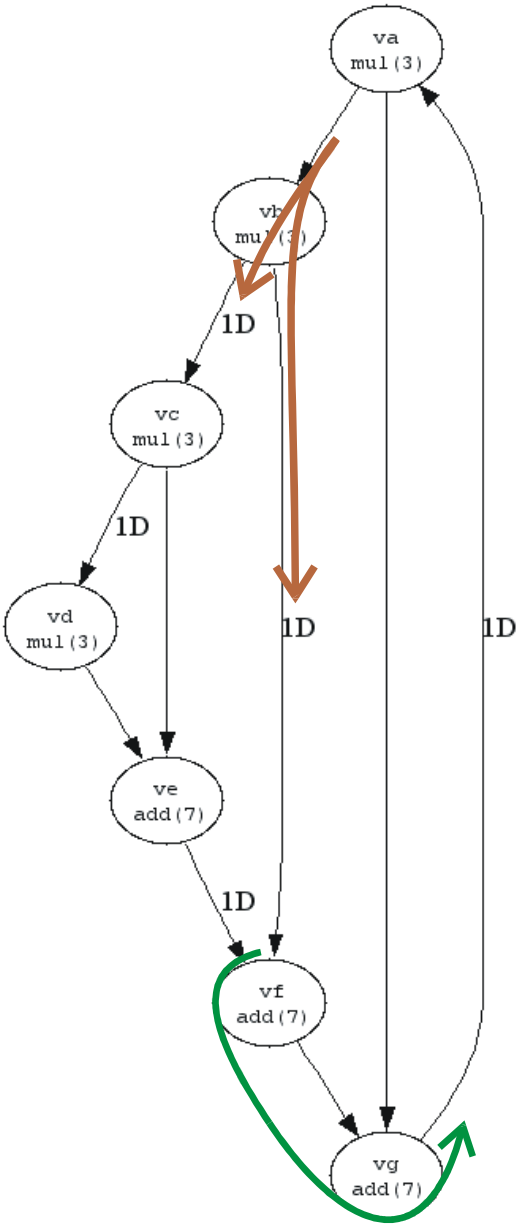
The topological critical path becomes (v_e , v_f , v_g), with a delay of 21 units ...

```
Retiming possible to decrease longest path to 17 state(s)
Actions needed:
       Change 1T delay from vb to vc into a straight connection.
       Change connection from ve to vf into a 1T delay.

Created file 'DeMicheli_Fig98_17cyc.cir' for this retimed circuit ...
```



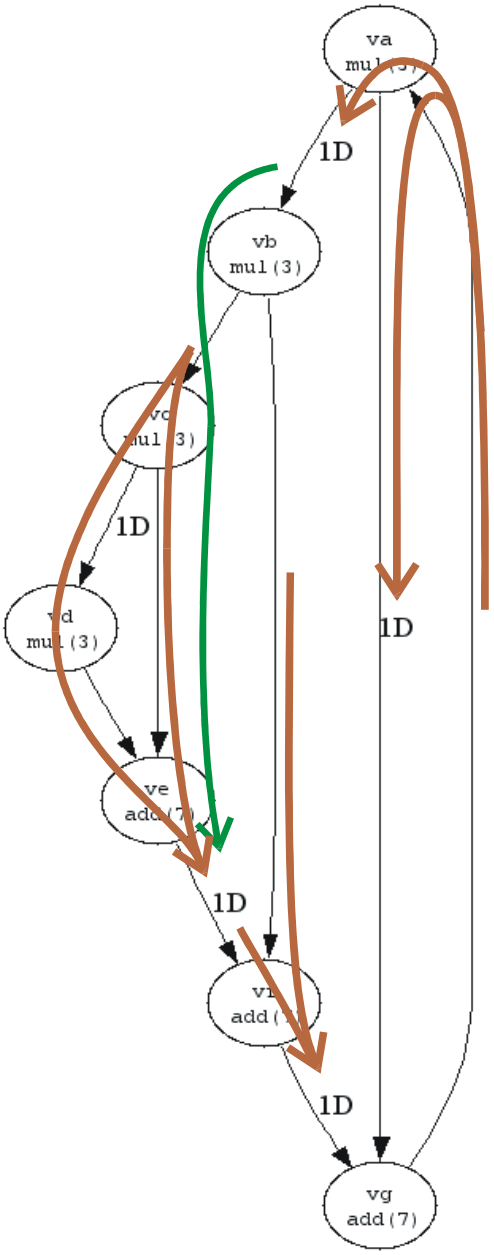
The topological critical path becomes (v_b , v_f , v_g), with a delay of 17 units ...

```
Retiming possible to decrease longest path to 14 state(s)
Actions needed:
       Change 1T delay from va to vb into a straight connection.
       Change connection from vb to vf into a 1T delay.
       Change connection from ve to vf into a 1T delay.

Created file 'DeMicheli_Fig98_14cyc.cir' for this retimed circuit ...
```



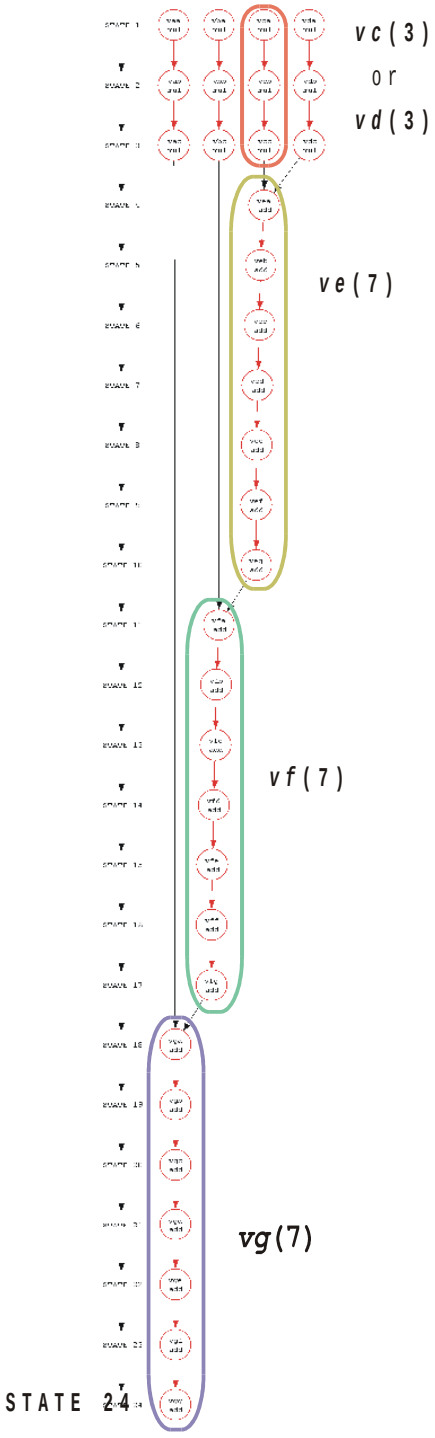
The topological critical path becomes (v_f, v_g), with a delay of 14 units ...

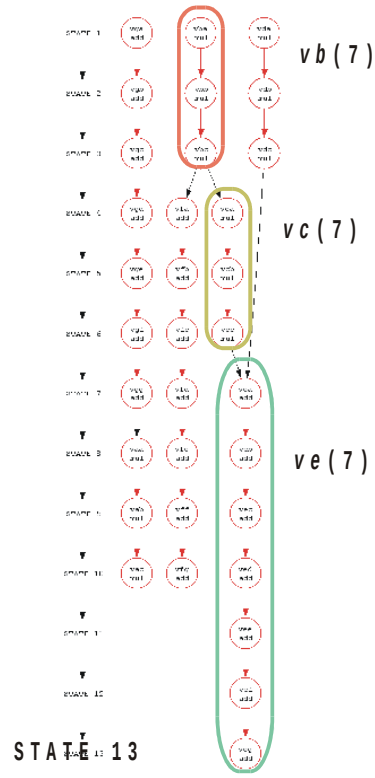
```
Retiming possible to decrease longest path to 13 state(s)
Actions needed:
       Change 1T delay from vg to va into a straight connection.
       Change 1T delay from vb to vc into a straight connection.
       Change connection from ve to vf into a 1T delay.
       Change connection from va to vg into a 1T delay.
       Change connection from vf to vg into a 1T delay.

Created file 'DeMicheli_Fig98_13cyc.cir' for this retimed circuit ...
```



De Micheli (**Example 9.3.8**):

"The topological critical path is (v_b , v_c , v_e), whose delay is 13 units."


vc(3)
or
vd(3)
ve(7)
vf(7)
vg(7)
STATE 24


vb(7)
vc(7)
ve(7)
STATE 13

```
Decreasing longest path to 12 cycles is not feasible ...
>>
```

So, the final retimed **.**cir-file becomes `'DeMicheli_Fig98_13cyc.cir'`:

```
% ... changed by retime_minClkPer.m on 11-Dec-2006 16:18:20
% ... 13 cycles only if delayMUL = 3, delayALU = 7 ...

iocDef = 'iokk';

va = ka * vg;
vb = kb * ib;
vc = kc * vb;
vd = kd * id;
ve = vc + vd;
vf = vb + i_xx1;
vg = ib + i_xx2;

oa = va;
ib = Toa;
oc = vc;
id = Toc;

% ADDITIONAL DELAY(S) FOR RETIMING:
o_xx1 = ve;
i_xx1 = To_xx1;
o_xx2 = vf;
i_xx2 = To_xx2;


% (c) HJLA, 2006
% [EOF]
```