et 4054 Methods and Algorithms for system design

Rene van Leuken, Amir Zjajo,
Alexander de Graaf
(part I, part II, lab)

EWI/ME/CAS

https://cas.tudelft.nl/Education/courses/et4054/index.php

https://cas.tudelft.nl/Education/msc_projects.php

TU Delft
Delft University of Technology

Agenda

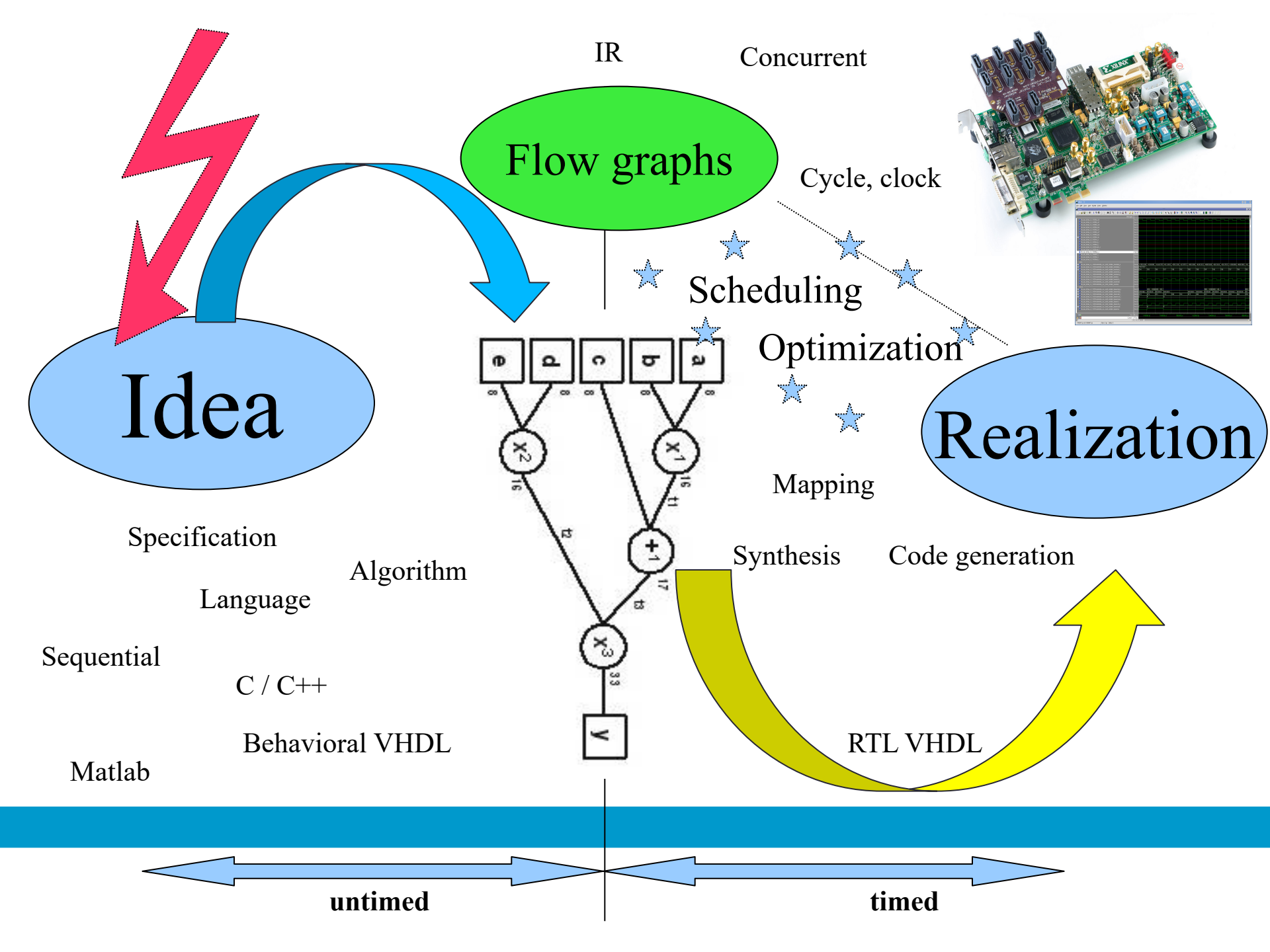
- What's this all about?
- Practicalities
- Example
- Chapter 3, Hardware Modeling

Goal

Digital hardware system design is the central topic of this course. We move beyond the methods developed in *circuit* design and consider situations in which the **functional behavior** of a **system** is the first object under consideration.

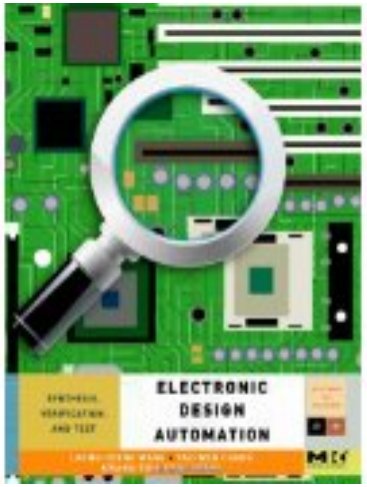
Behavioral synthesis is an design process that interprets an **algorithmic description** of a desired behavior and creates hardware that implements that behavior.

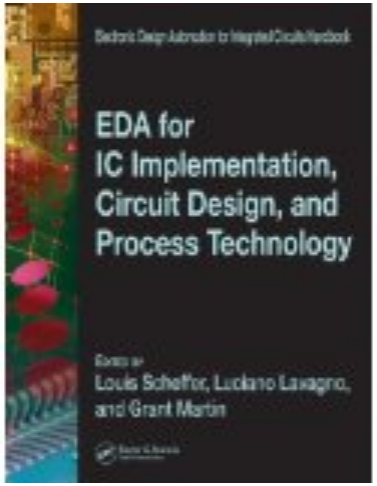
Starting with an algorithmic description in a high-level language, behavioral synthesis creates the **cycle-by-cycle detail (time&resources)** needed for **hardware** implementation.


IR
Concurrent
Flow graphs
Cycle, clock
Scheduling
Optimization
Idea
Realization
Mapping
Specification
Algorithm
Language
Synthesis
Code generation
Sequential
C / C++
Behavioral VHDL
RTL VHDL
Matlab
untimed
timed

Text Book & Materials (1)

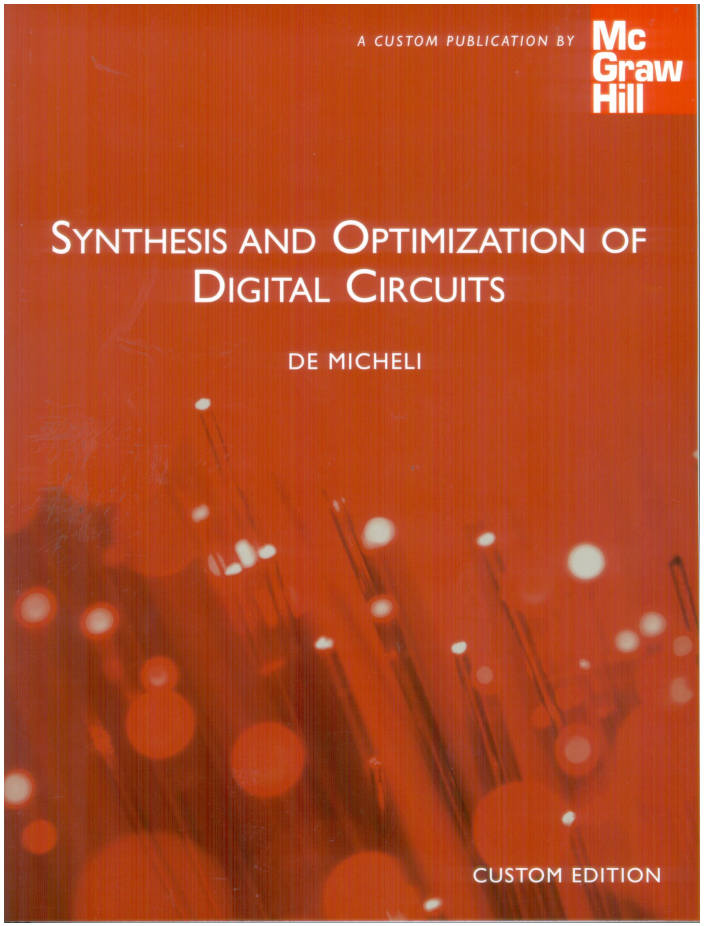
- Course books:
- chapters on High Level Synthesis and Static Timing Analyzes can be found in Electronic Design Automation, chapter 5, 6.5 and 6.6, (chapters can also be downloaded from our library) and
- EDA for IC Implementation, Circuit Design, and Process Technology, chapter 6. (Note: this chapter can also be downloaded from our library, but is an OLDER version)





Text Book & Materials (2)

- Course book: G. De Micheli, Synthesis and Optimization of Digital Circuits (PDF)
- Power Points
- Two chapters from other text books (Eles, Parhi). Can be download from the website.



ET4054 Lab Session Web Site

- The home page for this course is in https://cas.tudelft.nl/Education/courses/et4054

  (Link from Brightspace)
- Additional information about tools:
  https://cas.tudelft.nl/Education/courses/et4351

Text Book Content (1)

Electronic Design Automation: chapter 5, 6.5 and 6.6,
(Chapter 5 optional)

EDA for IC Implementation: Circuit Design, and Process Technology, chapter 6.

Text Book Content (2)

De Micheli, Synthesis and Optimization of Digital Circuits:

Chapt. 3
Chapt. 4: 4.1,2,3,4,5,6,7.
Chapt. 5: 5.1,2,3,4 (excl. 5.3.4, 5.4.5).
Scheduling additional materials: Chapter 3 FDS Petru Eles
Chapt. 6: 6.1,2, Chapt. 6.4,5,6. (excl. 6.2.4,6.2.5, 6.3, 6.5.2)

Chapt. 9: 9.1,2, Chapt. 9.3.1.
Retimimg additional materials.

Topics covered

Pareto points

Scheduling, ASAP, ALAP, list, Force Directed, ILP

Exact methods versus heuristic algorithms

Data & control flowgraph

Control synthesis

Resource & timing optimization

Sharing & binding of resources

Compatibility & conflict graph

Graph coloring, clique partitioning, left edge algorithm

Re-timing

Signals: Timing and delay

Statistical timing analysis

False paths, delay models, crosstalk

Constraints: Setup time, Hold time

Delay in FPGAs: PSM

Corner-based analysis

Clock trees

Practical timing constraints

Content ET4054 Exam 2019/2020

- One question chapter 3,4,5,6,9 de Michelli , or chapter 3 Petru Eles, or chapter 6 EDA books
- Paper presentation: Presentation of the paper you have studied
- Lab session: Bring the printouts and short report of the lab exercise you have done.

- You can bring to the exam any material you want.

ET4054 Paper presentation

- Each student will select/get a recent paper (journal/conference/workshop)
- Read and study the paper
- Present its content at the exam

ET4054 Lab Session

- Goal: Architectural study of some high-level unit, in our case some digital filter.
- Parameter study, implementation aspects
- Scheduling of operations, use of resources.
- Retiming of circuit
- Simulation of a timed realization of the high-level unit.
- Virtual server: et4054.ewi.tudelft.nl

ET4054 Lab Tools

- OS: Linux (!)
- Desktop: KDE
- MATLAB, version > 2014 b, …
- Modelsim, 10.1f
- Synplify_pro
- Xilinx Vivado
- A text editor, e.g. gvim, or kedit
- OpenOffice, or better LaTex
- WebPrinter

ET4054 Lab Location

- Location LB 02.900.
- Open 24/7.
- 12 PC's. There is no reservation list. Come and go.
- First couple of days busy, thereafter quiet.

- But best is to work at home/office with own laptop:
  - Windows: MobaXterm is a 'Enhanced terminal for Windows with X11 server'
  - SSH when using Linux or Mac (XQuartz)
  - XRDP = Remote desktop client

ET4054 Remote Server

- Available on any OS.
- et4054.ewi.tudelft.nl
- Remote access to all software and userspace
- NetID required to login
- 24/7
- User Guide on our website

ET4054 Lab Session Report

- a print-out of the Data Flow Graph, including operations, delays and interconnect (Also print the values of the input and calculated output variables),
- plots of Pareto curves of the Sequencing Graphs, including used scheduling parameters,
- a print-out of the Scheduled Sequencing Graph, and the scheduling parameters involved,
- Timing improvements, the files routed.twr and MODULENAME.bld (both in directory results_xst)
- A print-out of the retime parameters and retimed SG,
- a print-out of the simulation results (wave viewer)
- (optionally) a print-out of the schematic diagram of your design.

Proposed Dates Oral Exam 2019/2020

End Jan / begin Feb 2020;

Week 5/6:

Jan 28 , Jan 30, Jan 31, Feb 4 , Feb 6

Week 5, 2020 (3x2x5 slots)

Week 6, 2020 (2x2x5 slots)