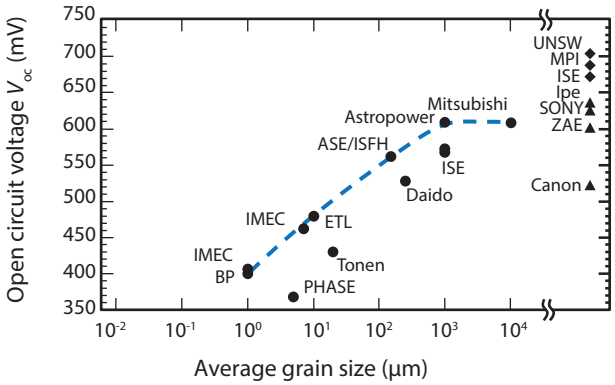

Figure 12.6: The relationship between the open circuit voltage and the average grain size (Reprinted from Thin Solid Films, vol. 403-404, R. Bergmann and J. Werner, The future of crystalline silicon films on foreign substrates, Pages 162-169, Copyright (2002), with permission from Elsevier) [46].

12.2 Production of silicon wafers

After the initial considerations on designing c-Si solar cells, we now will discuss how monocrystalline and multicrystalline silicon wafers can be produced. In Fig. 12.7 we illustrate the production process of monocrystalline silicon wafers.

The lowest quality of silicon is the so-called metallurgical silicon, which is made from *quartzite*. Quartzite is a rock consisting of almost pure silicon dioxide (SiO_2). For producing silicon the quartzite is molten in a submerged-electrode arc furnace by heating it up to around 1900°C, as illustrated in Fig. 12.7. Then, the molten quartzite is mixed with carbon. As a carbon source, a mixture of coal, coke and wood chips is used. The carbon then starts reacting with the SiO_2. Since the reactions are rather complex, we will not discuss them in detail here. The overall reaction how ever can be written as

$$SiO_2 + 2\,C \rightarrow Si + 2\,CO \tag{12.1}$$

As a result, carbon monoxide (CO) is formed, which will leave the furnace in the gas phase. In this way, the quartzite is purified from the silicon. After the reactions are finished, the molten silicon that was created during the process is drawn off the furnace and solidified. The purity of metallurgic silicon, shown as a powder in Fig. 12.7, is around 98% to 99%.

About 70% of the worldwide produced metallurgical silicon is used in the aluminium casting industry for make aluminium silicon alloys, which are used in automotive engine blocks. Around 30% are being used for make a variety of chemical products like silicones. Only around 1% of metallurgical silicon is used as a raw product for making electronic grade silicon.

The silicon material with the next higher level of purity is called polysilicon. It is made from a powder of metallurgical silicon in the *Siemens process*. In the process, the metallurgical silicon is brought into a reactor and exposed hydrogen chloride (HCl) at elevated

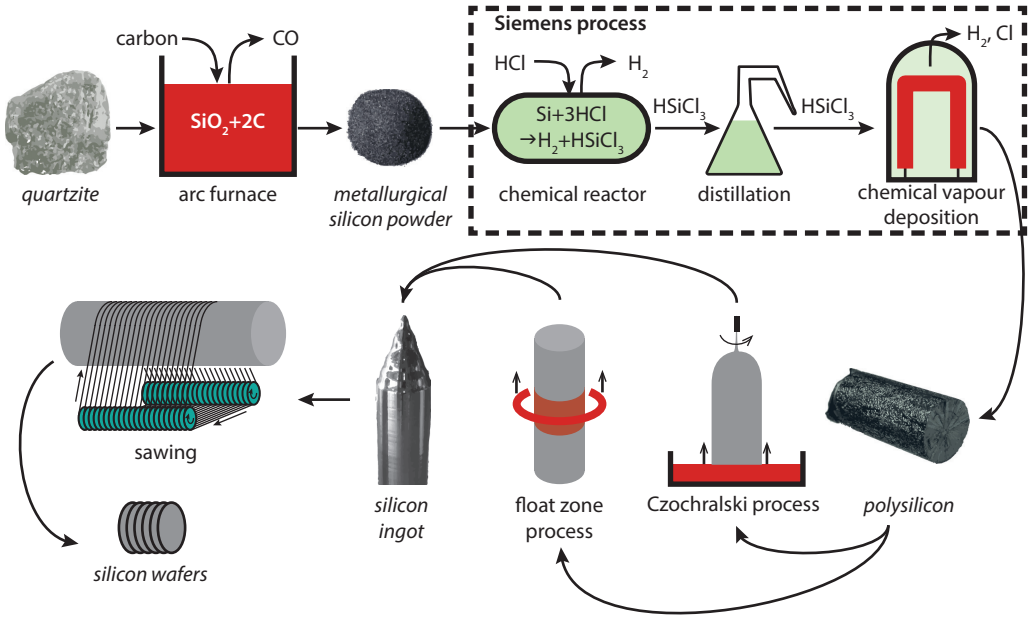

Figure 12.7: Illustrating the production process of monocrystalline silicon wafers.

temperatures in presence of a catalyst. The silicon reacts with the hydrogen chloride,

$$\mathrm{Si} + 3\,\mathrm{HCl} \rightarrow \mathrm{H_2} + \mathrm{HSiCl_3}, \tag{12.2}$$

leading to the creation of trichlorosilane ($HSiCl_3$). This is a molecule that contains one silicon atom, three chlorine atoms and one hydrogen atom. Then, the trichlorosilane gas is cooled and liquified. Using *distillation*, impurities with boiling points higher or lower than $HSiCl_3$ are removed. The purified trichlorosilane is evaporated again in another reactor and mixed with hydrogen gas. There, the trichlorosilane is decomposed at hot rods of highly purified Si, which are at a high temperature in between around 850°C and 1050°C. The Si atoms are deposited on the rod whereas the chlorine and hydrogen atoms are desorbed from the rod surface back in to the gas phase. As a result a pure silicon material is grown. This method of depositing silicon on the rod is one example of *chemical vapour deposition* (CVD). As the exhaust gas still contains chlorosilanes and hydrogen, these gasses are recycled and used again: Chlorosilane is liquified, distilled and reused. The hydrogen is cleaned and thereafter recycled back in to the reactor. The Siemens process consumes a lot of energy.

Polysilicon granules can also be produced using *Fluid Bed Reactors* (not shown in Fig. 12.7). This process is operated at lower temperatures and consumes much less energy. Polycrystalline silicon can have an purity as high as 99.9999%, or in other words only one out of million atoms is an atom different from Si.

The last approach we briefly mention is that of *upgraded metallurgical silicon* (not shown in Fig. 12.7). In this process metallurgical silicon is chemically refined by blowing gasses through the silicon melt removing the impurities. Although processing is cheap, the silicon

purity is lower than that achieved with the Siemens or the Fluid Bed reactor approaches.

Now we introduce two methods that are industrially used for making monocrystalline silicon *ingots*, *i.e.* large cylinders of silicon that consist of one crystal only. This means that inside the ingot no grain boundaries are present. Such a monocrystalline ingot and both the methods are sketched in Fig. 12.7.

The first method we discuss is based on the *Czochralski process* that was discovered by the Polish scientist Jan Czochralski in 1916. In this method, highly purified silicon is melted in a crucible at typical temperature of 1500°c. Intentionally boron or phosphorus can be added for making p-doped or n-doped silicon, respectively. A seed crystal that is mounted on rotating shaft is dipped in to the molten silicon. The orientation of this seed crystal is well defined; it is either 100 or 111 oriented. The melt solidifies at the seed crystal and adopts the orientation of the crystal. The crystal is rotating and pulled upwards slowly, allowing the formation of a large, single-crystal cylindrical column from the melt — the ingot. For successfully conducting the process, temperature gradients, the rate of pulling the shaft upwards and the rotational speed must be well controlled. Due to improved process control throughout the years, nowadays ingots of diameters of 200 mm or even 300 mm with lengths of up to two meters can be fabricated. To prevent the incorporation of impurities, the Czochralski process takes place in an inert atmosphere, like argon gas. The crucible is made from quartz, which partly dissolves in the melt as well. Consequently, monocrystalline silicon made with the Czochralski method has a relatively high oxygen level.

The second method to make monocrystalline silicon is the *float zone* process, which allows fabricating ingots with extremely low densities of impurities like oxygen and carbon. As a source material, a polycrystalline rod made with the Siemens process is used. The end of the rod is heated up and melted using an induction coil operating at radio frequency (RF). The molten part is then brought in contact with the seed crystals, where it solidifies again and adopts the orientation of the seed crystal. Again 100 or 111 orientations are being used. As the molten zone is moved along the polysilicon rod, the single-crystal ingot is growing as well. Many impurities remain in and move along with the molten zone. Nowadays, during the process nitrogen is intentionally added in order to improve the control over microdefects and the mechanical strength of the wafers. One advantage of the float-zone technique is that the molten silicon is not in contact with other materials like quartz, as this is the case when using the Czochralski method. In the float-zone process the molten silicon is only in contact with the inert gas like argon. The silicon can be doped by adding doping gasses like diborane (B_2H_6) and phosphine (PH_3) to the inert gas to get *p*-doped and *n*-doped silicon, respectively. The diameter of float-zone processed ingots generally is not larger than 150 mm, as the size is limited by surface tensions during the growth.

Not only monocrystalline silicon ingots, but also *multicrystalline silicon ingots*, which consist of many small crystalline grains, can be fabricated (not shown in Fig. 12.7). This can be made by melting highly purified silicon in a crucible and pouring the molten silicon in a cubic shaped *growth crucible*. There, the molten silicon solidifies in to multi-crystalline ingot in a process called *silicon casting*. If both melting and solidification is done in the same crucible it is referred to as *directional solidification*. Such multicrystalline ingots can have a front surface area of up to 70×70 cm^2 and a height of up to 25 cm.

Now, as we know how to produce monocrystalline and multicrystalline ingots we will

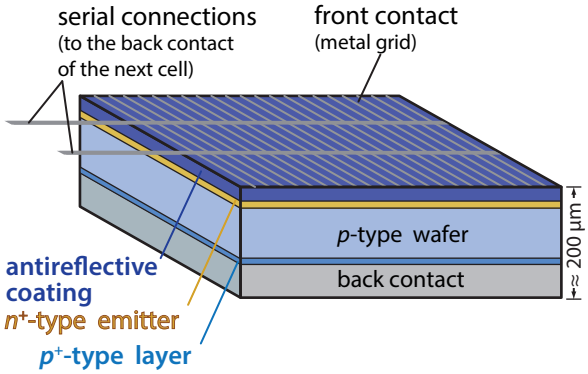

Figure 12.8: Scheme of a modern crystalline silicon cell.

discuss how to make *wafers* out of them. The process that is used to make the wafers is *sawing*, as illustrated in Fig. 12.7. Logically, sawing will damage the surface of the wafers. Therefore, this processing step is followed by a polishing step. The biggest disadvantage of sawing is that a significant fraction of the silicon is lost as *kerf loss*, which usually is determined by the thickness of the wire or saw used for sawing. Usually, it is in the order of 100 µm. As typical wafers used in modern solar cells have thicknesses in the order of 150 µm up to 200 µm, the kerf loss is very significant.

A completely different process for making silicon wafers is the *silicon ribbon* technique (not shown in Fig. 12.7). As this technique does not include any sawing step, no kerf loss occurs. In the silicon ribbon technique a string is used that is resistant agains high temperatures. This string is pulled up from a silicon melt. The silicon solidifies on the string and hence a sheet of crystalline silicon is pulled out of the melt. Then, the ribbon is cut into wafers. Before the wafers can be processed further in order to make solar cells, some surface treatments are required. The electronic quality of ribbon silicon is not as high as that of monocrystalline.

To summarise, we discussed how to make metallurgical silicon out of quartzite and how to fabricate polysilicon. We have seen that monocrystalline ingots are made using either the Czochralski or the float-zone process, while multicrystalline ingots are made using a casting method. Wafers are fabricated by sawing these ingots. A method that does not have any kerf losses in the ribbon silicon approach.

12.3 Designing c-Si solar cells

In this section, we briefly discuss the operating principles of c-Si solar cells. Especially, we discuss several technical aspects that play an important role in the collection of the light, excitation of charge carriers and the reduction of optical losses.

In Chapter 8 we discussed how an illuminated p-n junction can operate as a solar cell. In the illustrations used there, both the p-doped and n-doped regions have the same thickness. This is not the case in real c-Si devices. For example, the most conventional type of c-Si solar cells is built from a p-type silicon wafer, as sketched in Fig. 12.8. However,