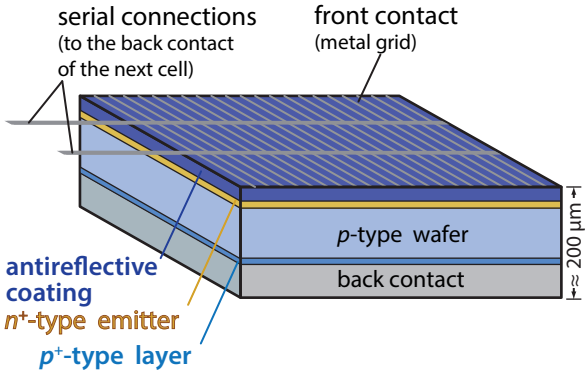

Figure 12.8: Scheme of a modern crystalline silicon cell.

discuss how to make *wafers* out of them. The process that is used to make the wafers is *sawing*, as illustrated in Fig. 12.7. Logically, sawing will damage the surface of the wafers. Therefore, this processing step is followed by a polishing step. The biggest disadvantage of sawing is that a significant fraction of the silicon is lost as *kerf loss*, which usually is determined by the thickness of the wire or saw used for sawing. Usually, it is in the order of 100 µm. As typical wafers used in modern solar cells have thicknesses in the order of 150 µm up to 200 µm, the kerf loss is very significant.

A completely different process for making silicon wafers is the *silicon ribbon* technique (not shown in Fig. 12.7). As this technique does not include any sawing step, no kerf loss occurs. In the silicon ribbon technique a string is used that is resistant agains high temperatures. This string is pulled up from a silicon melt. The silicon solidifies on the string and hence a sheet of crystalline silicon is pulled out of the melt. Then, the ribbon is cut into wafers. Before the wafers can be processed further in order to make solar cells, some surface treatments are required. The electronic quality of ribbon silicon is not as high as that of monocrystalline.

To summarise, we discussed how to make metallurgical silicon out of quartzite and how to fabricate polysilicon. We have seen that monocrystalline ingots are made using either the Czochralski or the float-zone process, while multicrystalline ingots are made using a casting method. Wafers are fabricated by sawing these ingots. A method that does not have any kerf losses in the ribbon silicon approach.

12.3 Designing c-Si solar cells

In this section, we briefly discuss the operating principles of c-Si solar cells. Especially, we discuss several technical aspects that play an important role in the collection of the light, excitation of charge carriers and the reduction of optical losses.

In Chapter 8 we discussed how an illuminated p-n junction can operate as a solar cell. In the illustrations used there, both the p-doped and n-doped regions have the same thickness. This is not the case in real c-Si devices. For example, the most conventional type of c-Si solar cells is built from a p-type silicon wafer, as sketched in Fig. 12.8. However,

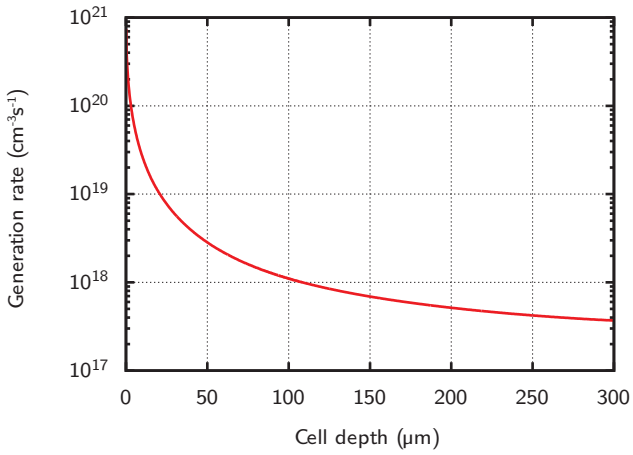

Figure 12.9: The generation profile in crystalline silicon illuminated under AM1.5. Note the logarithmic scale on the y-axis.

the n-type layer on the top of the p-wafer is much thinner than the wafer; it typically has a thickness of around 0.3 µm. Often, this layer is called the *emitter* layer. As mentioned before, the whole wafer has typically thicknesses in between 100 and 300 µm.

For monochromatic light the generation profile shows exponential decay (and hence a straight line on a logarithmic scale as in Fig. 12.9) because of the Lambert-Beer law [Eq. (4.25)]. Figure 12.9 shows the generation profile of silicon that is illuminated under the AM1.5 spectrum. This generation profile does not show such a behaviour because of the wavelength-dependent absorption coefficient [see e.g. Fig. 12.4]. The largest fraction of the light is absorbed close to the front surface of the solar cell. In the first 10 µm by far the most charge carriers are generated. By making the front emitter layer very thin, a large fraction of the light excited charge carriers generated by the incoming light are created within the diffusion length of the p-n junction.

Now we will discuss the collection of charger carriers in a crystalline silicon solar cell. The crucial components that play a role in charge collection are the emitter layer, the metal front contacts and the back contact. First, the emitter layer: At the p-n junction the minority charge carriers, which are excited by the light, are separated at the p-n junction: the minority electrons in the p-layer drift to the n-layer, where they have to be collected. Since the silicon n-emitter is not sufficiently conductive we have to use the much more conductive metal contacts, which are placed on top of the emitter layer. Very often, the metal contacts are made of the cheap metal aluminium.

This means that the electrons have to diffuse laterally through the emitter layer to the electric front contact to be collected. Which factors are important for a good transport of the electrons to the contact? First, the lifetime of the charge carriers needs to be high. A high lifetime guarantees large open circuit voltages, or in other words the optimal utilisation of the band gap energy. For increasing the lifetime, recombination losses must be reduced as much as possible.

Recombination not only reduces the V_{oc}, it also limits the collected current. As men-

tioned earlier, in silicon two recombination mechanisms are present: Shockley-Read-Hall recombination and Auger recombination. First, let us take a look at Shockley-Read-Hall recombination at the surface, that we introduced in Section 7.5. A bare c-Si surface contains many defects, because the surface silicon atoms have some valence electrons that cannot make molecular orbitals due to the absence of neighbouring atoms. These valence orbitals containing only one electron at the surface act like defects. They are also called *dangling bonds*. At the dangling bonds, the charge carriers can recombine through the SRH process. The probability and speed at which charge carriers can recombine is usually expressed in terms of the *surface recombination velocity*. Since a large fraction of the charge carriers are generated close to the front surface, a high surface recombination velocity at the emitter front surface will lead to significant charge carriers losses and consequently lower short-circuit current densities. In high-quality monocrystalline silicon wafers, for example, no defect-rich boundaries are present in the bulk. Thus, the lifetime of charge carriers is limited by the recombination processes at the wafer surface.

In order to reduce the surface recombination two approaches are used. First, the defect concentration on the surface is reduced by depositing a thin layer of a different material on top of the surface. This material partially restores the bonding environment of the silicon atoms. In addition, the material must be an insulator, it must force the electrons to remain in and move through the emitter layer. Typical materials used for this *chemical passivation* layers are silicon oxides (SiO_x) and silicon nitride (Si_xN_y).[1] A silicon oxide layer can be formed by heating up the silicon surface in an oxygen-rich atmosphere, leading to the oxidation of the surface silicon atoms. Si_3N_4 can be deposited using plasma-enhanced chemical vapour deposition (PE-CVD) that we will discuss in more detail in Chapters 13 and 14.

A second approach for reducing the surface recombination velocity is to reduce the minority charge carrier density near the surface. As the surface recombination velocity is limited by the minority charge carriers density, it is beneficial to have the minority charge carrier density at the surface as low as possible. By increasing the doping of the emitter layer, the density of the minority charge carriers can be reduced, which results in lower surface recombination velocities. However, this is in competition with the diffusion length of the minority charge carriers. The blue part of the solar spectrum leads to generation of many charge carriers very close to the surface, *i.e.* in the emitter layer. For utilising these light excited minority charge carriers, the diffusion length of the holes has to be large enough to reach the depletion zone at the *p-n* junction. However, increasing the doping levels leads to a decreasing diffusion length of the minority holes in the emitter. Therefore, too high doping levels or too thick emitter layers would result in a poor blue response or – in other words – low external quantum efficiency (EQE, see Chapter 9) values in the blue part of the spectrum. Such an emitter layer could be called "dead layer" as the light excited minority charge carriers can not be collected.

Next, we take a closer look at the metal-emitter interface. Because electrons must be easily conducted from the emitter to the metal, insulating passivation layers such as SiO_x or Si_xN_y cannot be used. Therefore, the metal-semiconductor interface has more defects and hence an undesirably high interface recombination velocity. Additionally, a metal-semiconductor junction induces a barrier for the majority charge carriers, as we have seen

[1] Stoichiometric silicon oxide and silicon nitride have the chemical formula SiO_2 and Si_3N_4, respectively. As the layers used for passivation are not stoichiometric, we indicate the elementary fractions with x and y.

in Section 8.3. Hence, this barrier will give rise to a higher contact resistance. Again high doping levels can reduce the recombination velocity at the metal-semiconductor interface and also reduce the contact resistance. In order to minimise the recombination at the interface defects as much as possible, the area of the metal-semiconductor interface must be minimised and the emitter directly below the interface should be heavily doped, which is indicated with n^{++}. The sides of the metal contacts are buried in the insulting passivation layer. The area below the contact has been heavily doped. These two approaches reduce the recombination and collection losses at the metal contact.

The solar cell shown in Fig. 12.8 has a classic metal grid pattern on top. We see two high ways for the electrons in the middle of top surface of the solar cell. They are called *busbars*. The small stripes going from the busbars to the edges of the solar cell are called the *fingers*. Let now R be the resistance of such a finger. If L, W, and H are the length, width and height of the fingers, respectively, and ρ is the resistivity of the metal, R is given by

$$R = \rho \frac{L}{WH}. \tag{12.3}$$

This equation shows that the longer the path length for an electron, the larger the resistance the electrons experience. Further, he smaller the cross-section $(W \cdot H)$ of the finger, the larger the resistance will be. Note, that the resistance of the contacts will act as a series resistance in the equivalent electric circuit. Larger series resistance will result in lower fill factors of the solar cell as discussed in Chapter 9. Hence, electrically large cross-sections of the fingers are desirable.

To arrive at a metallic contact, electrons in the emitter have to travel laterally through the emitter. Because of the resistivity of the n-type silicon, the charge carriers in the emitter layer also experience a resistance. It can be shown that the power loss due to the resistivity of the emitter layer scales with the spacing between two fingers to the power 3.

As the metal contacts are at the front surface, they act as unwelcome shading objects, or in other words light incident on the metallic front contact area cannot be absorbed in the PV-active layers. Therefore, the contact area should be kept as small as possible, which is in competition with the fact that the finger cross section should be maximised. So basically, the finger height should be as high as possible while the finger width, you would like to have as small as possible to comply with these requirements.

We can see that several effects compete with other. Fig. 12.10 (a) shows the relationship between power losses and finger spacing. With increasing finger spacing the power losses of the solar cell decreases because of less shading. On the other hand, the losses due to the increased resistivity in the emitter layer increase. Hence, there is an optimal spacing distance at that the power loss is minimal. A similar plot can be made for the power loss in dependence of the finger width; it is shown in Fig. 12.10 (b). The larger W the larger shading losses will be. But with increasing W the resistance decreases. Again, here an optimum exists at which the power losses are minimal. We see that optimising the front contact pattern is a complex interplay between the finger width and spacing.

For designing the back contact we find similar issues. Just as the electrons are to be collected in the front n-type layer, the holes are to be collected at the back contact. Electrons are the only charge carriers that exist in metal. Therefore the holes have to recombine with the electrons at the back semiconductor-metal interface. If the distance between the p-n interface and the back contact is smaller than the typical diffusion length of the minority

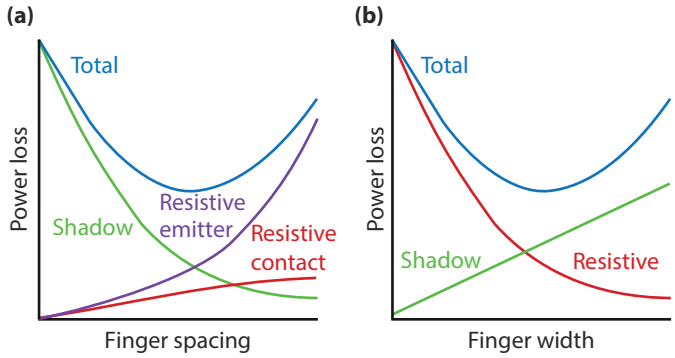

Figure 12.10: Power loss due to (a) spacing and (b) widths of the metallic fingers on top of a c-Si solar cell.

electrons, the minority electrons can be lost at the defects of the back contact interface because of SRH recombination

Several methods can be used to reduce this loss. First, the area between the metal contact and the semiconductor can be reduced, just as for the front contact. To do this, point contacts can be used, while the rest of the rear surface is passivated by an insulating passivation layer, similar as we already discussed for the emitter front surface. The recombination loss of electrons at the back contact can be further reduced by a introducing a *back surface field*. Above the point contacts a highly p-doped region is placed, which is indicated by p^+.

To understand how the back surface field works, we take a look at the band diagram shown in Fig. 12.11. The interface between the normally doped p-region and the highly doped p^+-region acts like an n-p junction. Here, this junctions acts as a barrier that prevents minority electrons in the p-region from diffusing to the back surface. Further, the space charged field behaves like a passivation layer for the defects at the back contact interface and allows to have higher minority carrier densities in the p-doped bulk.

After this thorough discussion on managing the charge carriers, we now take a closer look on managing the photons in a crystalline silicon solar cell. Several optical loss mechanisms must be addressed. These are shading, reflection losses, parasitic absorption losses in the non-PV active layers, and transmission through the back of the solar cell. As already mentioned, *shading losses* are caused by the metallic front contact grid.

Secondly, *reflection* from the front surface is an important loss mechanisms. We briefly mention two approaches to design *anti-reflective coatings* (ARC) for reducing these losses. First, reflection can be minimised based on the *Rayleigh film* principle: by putting a film with a refractive index smaller than that of silicon wafer between the cell and the wafer losses can be reduced. The optimal value for the refractive index of the intermediate layer equals the square root of the product of refractive indexes of the two other media,

$$n_{\text{opt}} = \sqrt{n_{\text{air}} n_{\text{Si}}}. \tag{12.4}$$

At a wavelength of 500 nm, the optimal refractive index for a layer in-between air and silicon is 2.1. Note that in practice a solar cell in encapsulated under a glass or polymer plate,

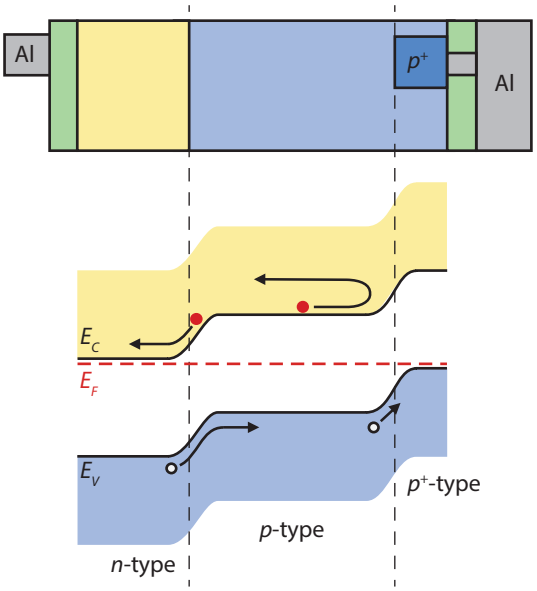

Figure 12.11: Effect of the back surface field illustrated in a band diagram.

which will have a beneficial effect on the refractive index grading as well, reducing the reflection losses further. Secondly, using the concept of destructive interference, the thickness and refractive index of an antireflection coating can be chosen such that in a certain wavelength range the reflection is minimised. This happens when the light reflected from the air-ARC interface is in anti-phase with the light reflected from the ARC-Si interface, as discussed in Chapter 4. We find that the thickness of such a layer should be *a quarter of the* wavelength in the layer,

$$d_{\mathrm{ARC}} = \frac{\lambda_0}{4n}, \tag{12.5}$$

where λ_0 denotes the wavelength *in vacuo* and n is the refractive index of the antireflective layer. For a refractive index of 2.1, a layer thickness of 60 nm would lead to destructive interference at 500 nm. As mentioned earlier, a typical material for passivation is silicon nitride. we have discussed earlier, one of the typical passivation layers of standard crystalline silicon is silicon nitride. Fig. 12.12 (a) shows a multicrystalline wafer without any ARC. It appears silverish, which means that it is highly reflective. In Fig. 12.12 (b) a similar wafer is shown after it was passivated with Si_xN_y. We see that it has a dark-blue appearance, hence its reflection is much lower. Interestingly enough, the refractive index of Si_xN_y at 500 nm is in the range of 2 to 2.2, close to the optimum mentioned earlier. The blue appearance indicates that reflection in the blue is stronger than at other wavelengths.

The reflection losses also can be minimised by texturing the wafer surface. Light that is reflected at the textured surface can be reflected at angles in which the trajectory of the light ray is incident somewhere else on the surface, where it still can be coupled into the silicon. Additionally, the scattering at textured surfaces will couple the light under angles different from the interface normal to the wafer. Therefore, the average path length of the light in

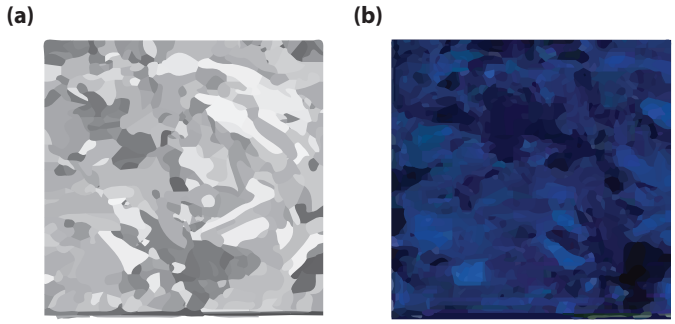

Figure 12.12: A multicrystalline silicon wafer (a) without and (b) with an antireflective coating from silicon nitride.

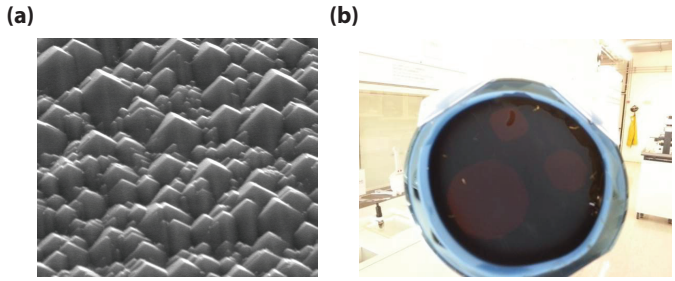

Figure 12.13: (a) A *textured* multicrystalline Si wafer and (b) a wafer with a *black silicon* surface.

the absorber will be increased, which leads to stronger absorption of the light. An example of a typical pyramid-textured c-Si wafer that was processed in the DIMES Research Center in Delft is shown in Fig. 12.13 (a). The process to create such textures is discussed in the Section 12.4. With a different etching approach, it is even possible to make silicon to appear completely black, as shown in Fig. 12.13 (b). This is called *black silicon*.

12.4 Fabricating c-Si solar cells

After this discussion on the different aspects that are important when designing c-Si solar cells, we now will discuss how such solar cells actually can be fabricated. Figure 12.14 shows a schematic flowchart for the fabrication of c-Si solar cells.

The first step of fabricating a solar cell is to clean a silicon wafer, which is fabricated as discussed in Section 12.2. This cleaning happens in an acidic or alkaline wet etch process and is also important to remove damage in the wafer due to the sawing process, with which wafers are cut out of an ingot. As we have seen in the Section 12.3, most c-Si solar cells are textured in order to increase the absorption of the incident light and to reduce reflection losses. The textures usually are created during a wet etching process using a mixture of *potassium hydroxide* (KOH) and *2-propanol* (isopropanol, C_3H_7OH). Interestingly enough, 100 surfaces are etched much faster than the 111 surfaces. Such a behaviour is

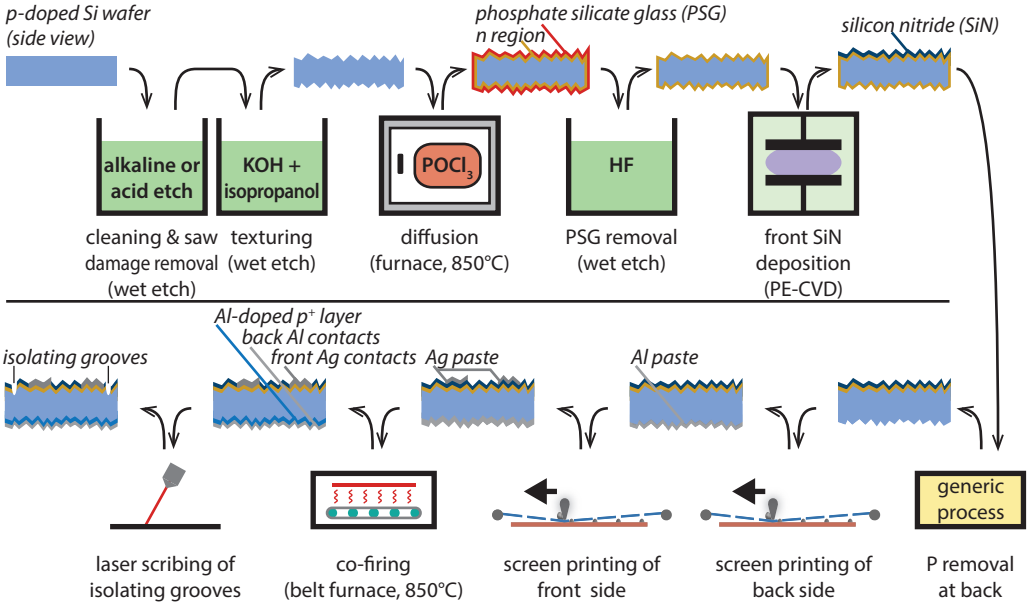

Figure 12.14: Schematic flowchart for making crystalline silicon solar cells.

called *anisotropic etching*. Thus, when a 100 wafer is etched, the 100 surface will be etched away, while the (*slanted*) 111 surface facets will remain. Therefore, we obtain a wafer with a pyramid structure consisting of 111 facets only.

Next, the emitter layer has to be created, for example during a *solid state diffusion* process. In this process, the wafers are placed in a furnace at around 850°C. In the furnace, a phosphorus-containing chemical is present, which acts as a source for the P atoms that are used as n-dopants. Often, *phosphoryl chloride* ($POCl_3$) is used as a P source. At these high temperatures, the P atoms react with the surface, and they are mobile in the silicon crystal. According to Fick's law, they can diffuse into the wafer,

$$J(x) = -D\frac{\mathrm{d}n}{\mathrm{d}x}, \tag{12.6}$$

where the particle flux J (in $\mathrm{cm}^{-2}\mathrm{s}^{-1}$) is proportional to the negative gradient of the particle density n (in cm^{-3}). D (in $\mathrm{cm}^2\mathrm{s}^{-1}$) is the diffusion constant. The diffusion process has to be controlled such that the dopants penetrate into the solid to establish the desired emitter thickness. During the diffusion process not only the emitter is created, but also a thin layer of *phosphosilicate glass* (PSG) – a mixture of P_2O_5 and SiO_2. This PSG layer has to be removed, which usually happens in a wet etching process using *hydrofluoric acid* (HF).

Now, a *silicon nitride* layer is deposited onto the emitter, which acts as antireflective coating and passivating layer, as we have seen in Section 12.3. Different processes can be used for the deposition of this layer, such as *plasma-enhances chemical vapour deposition* (PE-CVD) that we discuss in more detail in Chapter 14.

During the diffusion process an n-doped layer was not only created at the front side,

but also on the back side. This layer at the back has to be removed, as otherwise we would have an *n*-*p*-*n* device that would not be a working solar cell. The removal can happy with many different processes, for example wet etching. Alternatively, also sometimes a protective layer is deposited onto the back side prior to the emitter diffusion. This layer would prevent the creation of an *n*-doped layer at the back.

Now the *p*-*n* junction in principle is finished; we only need to make the electrical contacts at the front and the rear that allow us to connect the solar cell with an electric circuit or with other solar cells in a PV module. In industry these contacts are usually fabricated using screen printing processes followed by firing. These processes are explained in detail in Chapter 14. Different screen printing pastes are used, which are usually based on aluminium or silver as a metal. For the front contact commonly Ag paste is printed on top of the passivation layer. As we have seen in Section 12.3, the design of the front metal grid needs a careful optimisation between resistive and shading losses. In contrast the rear side is totally covered with Al.

To make real contacts out of the screen-printing pastes, the cell is put in a belt furnace at 850°C. This process is called *firing*; if both the top and front contacts are fired at the same time, we call it *co-firing*. As a result of the co-firing process the front side Ag paste etches away the underlying SiN layer, forming a direct contact with the emitter.

During the co-firing process Al atoms diffuse into the wafer at the rear side and act as a *p*-type dopant, forming a p^+ layer at the rear of the device. Because of this layer, a back surface field (BSF) is created, which enhances the performance of the solar cell as we have seen in Section 12.3. However, during this process also an eutectic layer is created at the rear side, which leads to high parasitic absorption and hence low internal reflection of light that penetrates through the entire solar cell to the back. Usually, also Ag busbars are screen-printed on the back side for the interconnections with other cells.

The last step is to create isolating grooves at the border of the solar cells. This for example can be done with laser scribing. Isolating grooves are very important to prevent leakage currents along the sides of the solar cells. Such leaking currents can be very detrimental to the solar cell performance, hence it is important to prevent leakage currents.

12.5 High-efficiency concepts

In the last section of this chapter we discuss three examples of high-efficiency concepts based on crystalline silicon technology. As already discussed earlier, different types of silicon wafers with different qualities can be used. Naturally, for achieving the highest efficiencies, the bulk recombination must be as small as possible. Therefore the high efficiency concepts are based on monocrystalline wafers.

12.5.1 The PERL concept

The first high efficiency concept was developed in the late 1980s and the early 1990s at the *University of New South Wales* in the group of Martin Green. Figure 12.15 shows an illustration of the PERL concept, which uses a *p*-type float zone silicon wafer. With this concept, conversion efficiencies of 25% were achieved [47]. The abbreviation PERL cell stands for