but also on the back side. This layer at the back has to be removed, as otherwise we would have an *n*-*p*-*n* device that would not be a working solar cell. The removal can happy with many different processes, for example wet etching. Alternatively, also sometimes a protective layer is deposited onto the back side prior to the emitter diffusion. This layer would prevent the creation of an *n*-doped layer at the back.

Now the *p*-*n* junction in principle is finished; we only need to make the electrical contacts at the front and the rear that allow us to connect the solar cell with an electric circuit or with other solar cells in a PV module. In industry these contacts are usually fabricated using screen printing processes followed by firing. These processes are explained in detail in Chapter 14. Different screen printing pastes are used, which are usually based on aluminium or silver as a metal. For the front contact commonly Ag paste is printed on top of the passivation layer. As we have seen in Section 12.3, the design of the front metal grid needs a careful optimisation between resistive and shading losses. In contrast the rear side is totally covered with Al.

To make real contacts out of the screen-printing pastes, the cell is put in a belt furnace at 850°C. This process is called *firing*; if both the top and front contacts are fired at the same time, we call it *co-firing*. As a result of the co-firing process the front side Ag paste etches away the underlying SiN layer, forming a direct contact with the emitter.

During the co-firing process Al atoms diffuse into the wafer at the rear side and act as a *p*-type dopant, forming a p^+ layer at the rear of the device. Because of this layer, a back surface field (BSF) is created, which enhances the performance of the solar cell as we have seen in Section 12.3. However, during this process also an eutectic layer is created at the rear side, which leads to high parasitic absorption and hence low internal reflection of light that penetrates through the entire solar cell to the back. Usually, also Ag busbars are screen-printed on the back side for the interconnections with other cells.

The last step is to create isolating grooves at the border of the solar cells. This for example can be done with laser scribing. Isolating grooves are very important to prevent leakage currents along the sides of the solar cells. Such leaking currents can be very detrimental to the solar cell performance, hence it is important to prevent leakage currents.

12.5 High-efficiency concepts

In the last section of this chapter we discuss three examples of high-efficiency concepts based on crystalline silicon technology. As already discussed earlier, different types of silicon wafers with different qualities can be used. Naturally, for achieving the highest efficiencies, the bulk recombination must be as small as possible. Therefore the high efficiency concepts are based on monocrystalline wafers.

12.5.1 The PERL concept

The first high efficiency concept was developed in the late 1980s and the early 1990s at the *University of New South Wales* in the group of Martin Green. Figure 12.15 shows an illustration of the PERL concept, which uses a *p*-type float zone silicon wafer. With this concept, conversion efficiencies of 25% were achieved [47]. The abbreviation PERL cell stands for

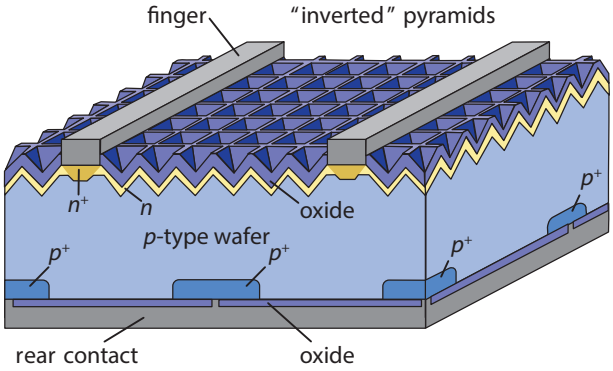

Figure 12.15: Illustrating the structure of a PERL solar cell.

Passivated Emitter Rear Locally diffused cell. This abbreviation indicates two important concepts that have been integrated in this technology: First, the optical losses of the PERL solar cell at the front side are minimised using three techniques:

1. The top surface of the solar cell is textured with inverted-pyramid structures. This microscopic texture allows a fraction of the reflected light to be incident on the front surface for a second time, which enhances the total amount of light coupled in to the solar cell.
2. The inverted pyramid structure is covered with a double-layer anti-reflection coating (ARC), which results in an extremely low top surface reflection. Often a double layer coating of magnesium fluoride (MgF_2) and zinc sulfide (ZnS) is used as an antireflection coating.
3. The contact area at the front side has to be as small as possible, to reduce the shading losses. In the PERL concept the very thin and fine metal fingers are processed using photolithography technology.

Secondly, the emitter layer is well-designed. As discussed in the previous sections, the emitter should be highly doped underneath the contacts, which in the PERL concept is achieved by heavily phosphorus diffused regions. The rest of the emitter is moderately doped, or in other words lightly diffused, to preserve an excellent blue response. The emitter is passivated with a silicon oxide layer on top of the emitter to suppress surface recombination as much as possible. With the PERL concept, the surface recombination velocity could be reduced so far that open circuit voltages with values of above 700 mV could be obtained.

At the rear surface of the solar cell, point contacts have been used in combination with thermal oxide passivation layers, which passivates the non-contacted area, and hence reduces the undesirable surface recombination. A highly doped boron region, created by local Boron diffusion, operates as a local back surface field, to limit the recombination of the minority electrons at the metal back contact.

The PERL concept includes some expensive processing steps. Therefore, the Chinese company *Suntech* developed in collaboration with University of New South Wales a more

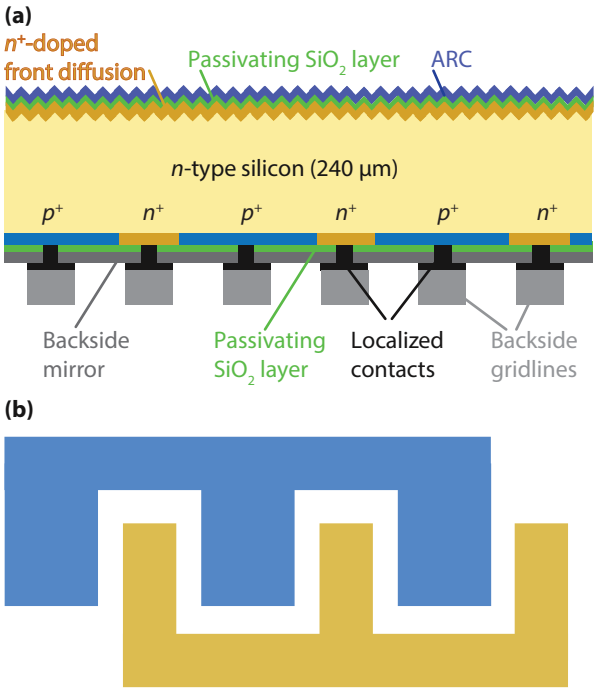

Figure 12.16: (a) Illustrating the structure of an IBC solar cell and (b) the contacts on its back.

commercially viable crystalline silicon cell technology, which is inspired by the PERL design.

12.5.2 The interdigitated back contact (IBC) solar cell

A second successful cell concept is the *interdigitated back contact* (IBC) solar cell. The main idea of the IBC concept is to have no shading losses at the front metal contact grid at all. All the contacts responsible for collecting of charge carriers at the n- and p-side are positioned at the back of the crystalline wafer solar cell. A sketch of such a solar cell is shown in Fig. 12.16 (a).

An advantage of the IBC concept is that monocrystalline float-zone n-type wafers can be used. This is interesting because n-type wafers have some interesting advantages with respect to p-type wafers. First, the n-type wafers do not suffer from light induced degradation. In p-type wafers both boron and oxygen are present, which under light exposure start to make complexes that act like defects. This light induced degradation causes a reduction of the power output with 2-3% after the first weeks of installation. No such effect is present in n-type wafers. The second advantage is that n-type silicon is not that sensitive for impurities like for example iron impurities. As a result, less efforts have to be made to fabricate high quality n-type silicon, and thus high quality n-type silicon can be processed cheaper than p-type silicon. On the other hand, p-doped wafers have the advantage that

the boron doping is more homogeneously distributed across the wafer as this is possible for n-type wafers. This means that within one n-type wafer the electronic properties can vary, which lowers the yield of solar cell production based on n-type monocrystalline wafers.

Besides that IBC cells are made from n-type wafers, they lack one large p-n junction. Instead, IBC cells have many localised junctions. The holes are separated at a junction between the p^+ silicon and the n-type silicon, whereas the electrons are collected using n^+-type silicon. The semiconductor-metal interfaces are kept as small as possible in order to reduce the undesired recombination at this defect-rich interface. Another advantage is that the cross section of the metal fingers can be made much larger, because they are at the back and therefore do not cause any shading losses. Thus, resistive losses at the metallic contacts can be reduced. Since both electric contacts are on the back side, it contains two metal grids, as illustrated in Fig. 12.16 (b). The passivation layer should made from a low-refractive-index material such that it operates like a backside mirror. It will reflect the light above 900 nm, which is not absorbed during the first pass back in to the absorber layer. Thus, this layer enhances the absorption path length.

At the front side of the IBC cell losses of light-excited charge carriers due to surface recombination is suppressed by a *front surface field* similar to the back surface field discussed earlier. This field is created with a highly doped n^+ region at the front of the surface. Thus, a n^+-n junction is created that acts like a n-p junction. It will act as a barrier that prevents the light-excited minority holes in the n-region from diffusing towards the front surface. The front surface field behaves like a passivation for the defects at the front interface and allows to have higher levels for the hole minority density in the n-doped bulk.

Reflective losses at the front side are reduced in a similar way as for PERL solar cells: Deposition of double layered antireflection coatings and texturing of the front surface.

The IBC concept is commercialised by the U.S. company *SunPower Corp.*, who have achieved high solar cell efficiencies of 24.2%.

12.5.3 Hetero junction (HIT) solar cells

The third high-efficiency concept are *heterojunction with intrinsic thin layer* (HIT) solar cells. Before we discuss the technological details, we briefly recall the principles of heterojunctions, that already were discussed in Section 8.2.

Homojunctions, which are present in all the c-Si solar cell types discussed so far in this chapter, are fabricated by different doping types within the same semiconductor material. Hence, the band gap in the p- and n-regions is the same. A junction consisting of a p-doped semiconductor material and an n-doped semiconductor made from another material is called a *heterojunction*. In HIT cells, the heterojunction is formed in-between two different silicon-based semiconductor materials: On the one hand, we use a n-type float zone monocrystalline silicon wafer. The other material is hydrogenated amorphous silicon (a-Si:H), which we will discussed in more detail in Section 13.3. a-Si:H is a silicon material in which the atoms are not ordered in a crystalline lattice but in a disordered lattice. For the moment we only must keep in mind that a-Si:H has a band gap of around 1.7 eV which is considerably higher than that of c-Si (1.12 eV).

In Fig. 12.17 a band diagram of a heterojunction between n-doped crystalline silicon and p-doped amorphous silicon in the dark and thermal equilibrium is sketched. We see that next to the induced field because of the space charge region, some local energy steps

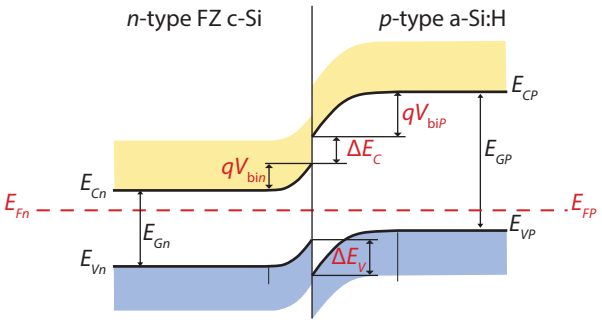

Figure 12.17: Illustrating the band diagram of a heterojunction.

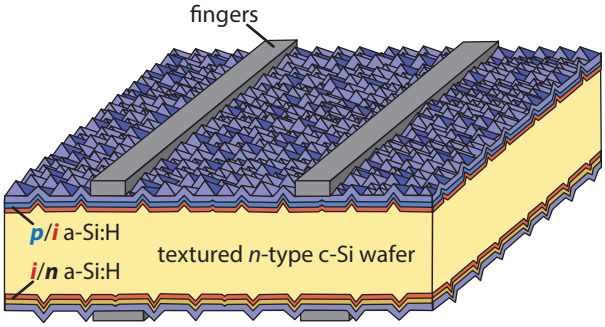

Figure 12.18: Illustrating the structure of a HIT solar cell.

are introduced. These steps are caused by the two different bandgaps for the p and n regions. The valence band is higher positioned in the p-type amorphous silicon than in the n-type crystalline silicon. This will allow the minority charge carriers in the n-type c-Si, the holes, to drift to the p-type silicon. However, the holes experience a small barrier. While they could not travel across such a barrier in classical mechanics, quantum mechanics allows them to *tunnel* across this barrier.

Let us now take a closer look to HIT solar cells. The HIT concept was developed by the Japanese company Sanyo, that is currently a part of the Japanese *Panasonic Corp.* As we can see in Fig. 12.18, the HIT cell configuration has two junctions: The junction at the front side is formed using a thin layer of only 5 nanometers of intrinsic amorphous silicon which is indicated by the color red. A thin layer of p-doped amorphous silicon is deposited on top and here indicated with the color blue. The heterojunction forces the holes to drift to the p-layer. At the rear surface a similar junction is made: First, a thin layer of intrinsic amorphous silicon is deposited on the wafer surface, indicated by red. On top of the intrinsic layer an n-doped amorphous silicon is deposited indicated, which is indicated by the yellow color.

As discussed earlier, for high quality wafers, like this n-type float zone monocrystalline silicon wafer, the recombination of charge carriers at the surface determines the charge carrier lifetime. The advantage of the HIT concept is that the amorphous silicon acts as a very

good passivation layer. With this approach the highest possible charge carrier lifetimes are accomplished. Thus, c-Si wafer based heterojunction solar cells have the highest achieved open circuit voltage among the different crystalline silicon technologies. The current record cell[2] has an open circuit voltage of 0.74 V and en efficiency of 25.6%.

How do the charge carriers travel to the contacts? The conductive properties of the *p*-doped amorphous silicon are relatively poor. While in the homojunction solar cells the lateral diffusion to the contacts takes place in the emitter layer, in a HIT solar cell this occurs through a transparent conducting oxide (TCO) material, like indium tin oxide (ITO), which is deposited on top of the *p*-doped layer. TCOs are discussed in more detail in Section 13.1.

The same contacting scheme is applied at the *n*-type back side. This means that this solar cell can be used in a bifacial configuration: it can collect light from the front, and scattered and diffuse light falling on the back-side of the solar cell. Another important advantage of the HIT technology is that the amorphous silicon layers are deposited using the cheap plasma enhanced chemical vapour deposition (PE-CVD) technology at low temperatures, not higher than 200°C. Therefore, making the front surface and back surface fields in HIT solar cells is very cheap.

In this chapter we discussed many aspects of crystalline silicon solar cell technology. Before the solar cells can be installed, they must be packed as a *PV module*. How such modules are made is discussed in Chapter 15.

12.6 Exercises

12.1 Which of the following statements is true about mono- and multicrystalline silicon?

(a) SRH recombinations are more important in multicrystalline than in monocrystalline silicon.

(b) Higher open-circuit voltages are obtained with multicrystalline than with monocrystalline silicon.

(c) The open-circuit voltage increases as the grain size of the multicrystalline silicon absorber layer decreases.

(d) The lifetime of minority charge carriers is higher in multicrystalline than in monocrystalline silicon.

12.2 What is the proper order, from lower purity to higher purity, of the following types of silicon?

(a) Metallurgical silicon / monocrystalline silicon / polysilicon

(b) Monocrystalline silicon / polysilicon / metallurgical silicon

(c) Metallurgical silicon / polysilicon / monocrystalline silicon

(d) Polysilicon / metallurgical silicon / monocrystalline silicon

12.3 Which of the following processes is used in order to fabricate monocrystalline silicon? (More than one correct answer possible.)

(a) The Czochralski process.

[2] As of May 2014.